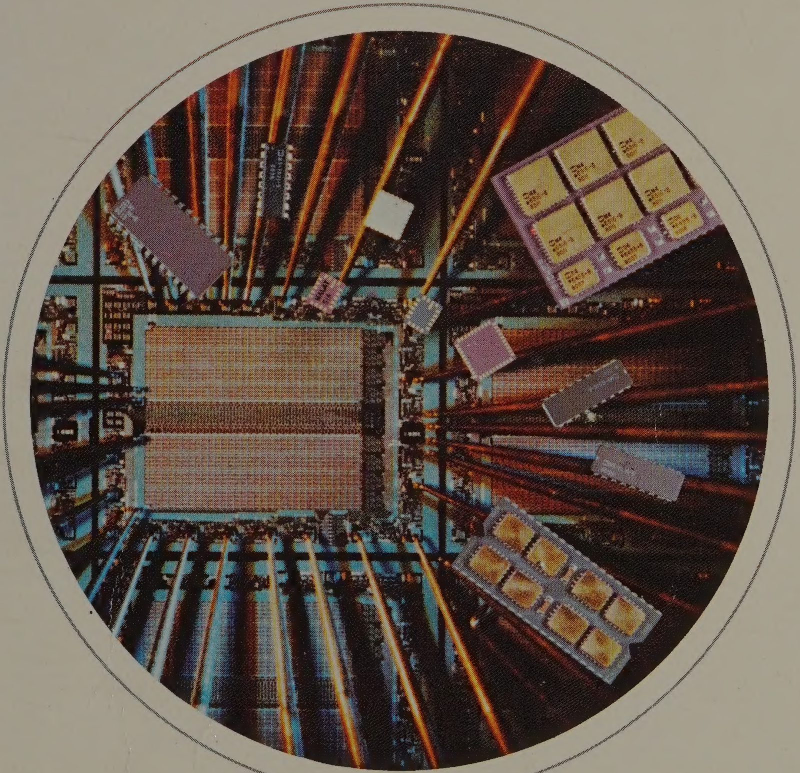
DIGITAL

BIPOLAR

CMOS



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

Volume 2
1981

Volume 2
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HARRIS
Digital Data Book

Harris Semiconductor Digital Products represent state-of-the-art in density and high speed performance. HARRIS expertise in design and processing offers the user the most reliable product available in a wide choice of formats, options, and package types. With continuing research and development and the introduction of new products, Harris will provide its customers with the most advanced technology.

This book describes Harris Semiconductor Products Division's complete line of digital products and includes a complete set of product specifications and data sheets. Also included are sections on reliability, programming, and packaging.

Please fill out the registration card at the back of this book and return it to us so we may keep you informed of our latest new product developments over the next year.

If you need more information on these and other HARRIS products, please contact the nearest HARRIS sales office listed in the back of this data book.

Harris Semiconductor's products are sold by description only. HARRIS reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Information contained in application notes is intended soley for general guidance; use of the information for user's specific application is at user's risk. Reference to products of other manufacurers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

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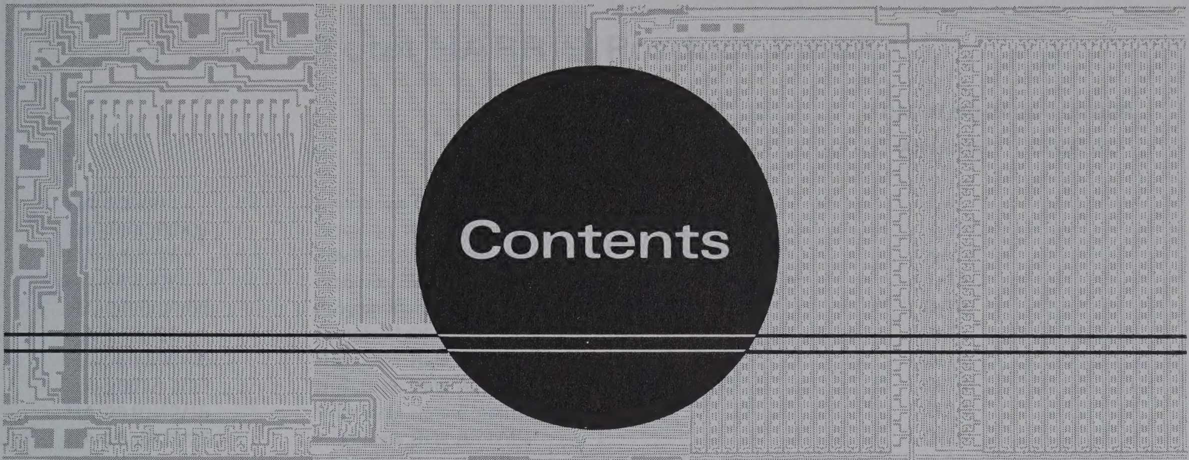

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Data Sheet Classifications

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview DATA SHEET	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information DATA SHEET	Sampling or Pre-Production	This is advanced information, and specifications are subject to change without notice.
Preliminary DATA SHEET	First Production	Supplementary data may be published at a later date. Harris reserves the right to make changes at any-time without notice, in order to improve design and supply the best product possible.

I. C. Handling Procedures

Harris I.C. processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common I.C. internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance I.C. inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existance in the industry. In addition most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10KV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1-M ohm to ground. The 1-M ohm resistor will prevent electroshock injury to personnel.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid, in the generation of a static change. Where they cannot be eliminated natural materials such as cotton etc. should be used to minimize charge generation capacity.
- Control relative humidity to as high as a level as practical. (RH 50%).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting material. If this is not possible, ionized air blowers may be a good alternative.

---

* Supplier 3M Company "Velostat"

HARRIS Memory Selection Guide

NUMBER WORDS	1	2	4	8	12
32	**32**	**64**	**128**	PROM 7602 7603 **256**	**512**
64	**64**				RAM 6512 **1024**
128	**128**				**2048**
256	**256**		RAM 6501 6551 6561 6562 PROM 6611 6661 7610(A) 7611(A)		**4096**
512	**512**		RAM 6513 PROM 7620(A) 7621(A)	PROM 6641 7640(A) 7641(A) 7647R 7648 7649	**8192**
1024	RAM 6508 6518 **1024**		RAM 6514 PROM 7642(A)(P) 7643(A)(P) 7644(A)	PROM 7608 7680(R)(P)(RP) 7681(R)(P)(RP) RAM 6515	ROM 6322 **16,384**
2048	RAM 6503 **2048**		PROM 7684(P) 7685(P)	PROM 7616 76160 76161 RAM 6516	**32,768**
4096	RAM 6504 6505 **4096**				**65,536**
8192	**8192**			RAM 6564	**131,072**
16,384	**16,384**	**32,768**	RAM 6564 **65,536**	**131,072**	**262,144**

BYTE SIZE

Bipolar PROM Cross Reference

AMD	HARRIS
AM 27LS08 AM 27S08 AM 29750 AM 27S18	7602
AM 27LS09 AM 27S09 AM 29751 AM 27S19	7603
AM 27LS100 AM 27S10 AM 29760 AM 27LS20	7610/10A
AM 27LS11 AM 27S11 AM 29761 AM 27LS21	7611/11A
AM 27S12 AM 29770	7620/20A
AM 27S13 AM 29771	7621/21A

INTEL	HARRIS
3601	7610/10A
3621	7611/11A
3602/02A	7620/20A
3622/22A	7621/21A
3604/04A 3604L	7640/41A
3624/24A	7641/41A
3605	7642
3625	7643
3608	7680
3628	7681

MOTOROLA	HARRIS
MCM5303A	JAN 0512
MCM7640	7640/40A
MCM7641	7641/41A
MCM7642	7642
MCM7643	7643
MCM2708	7608

RAYTHEON	HARRIS
29660 29662	7610/10A
29661 29663	7611/11A
29611 29613	7620/20A
29620 29622	7648
29624 29625	7640/40A
29621 29623	7649
29625 29627	7641/41A
29630 29632	7680
29631 29633	7681
29634 29635 29636 29637	7608

FAIRCHILD	HARRIS
93417	7610/10A
93427	7611/11A
93436	7620/20A
93446	7620/21A
93438	7640/40A
93448	7641/41A
93452	7642
93453	7643
93450	7680
93451	7681

INTERSIL	HARRIS
5600	7602
5610	7603
5603	7610/10A
5623	7611/11A
5604	7620/20A
5624	7621/21A
5605	7640/40A
5625	7641/41A
56506	7642
56526	7643

NATIONAL	HARRIS
DM8577 DM74S188	7602
DM8578 DM74S288	7603
DM74S387	7610/10A
DM74S287	7611/11A
DM74S473	7648
DM87S295	7640/40A
DM74S472	7649
DM87S296	7641/41A
DM74S572	7642
DM74S573	7643
DM87S229	7680
DM87S228	7681
DM74S672	7684
DM74S673	7685
DM27LS08	7608

SIGNETICS	HARRIS
82S23	7602
82S123	7603
82S27 82S126	7610/10A
82S129	7611/11A
82S130	7620/20A
82S131	7621/21A
82S146	7648
82S140	7640/40A
82S147	7649
82S141	7641/41A
82S136	7642
82S137	7643
82S180	7680
82S181	7681
82S2708	7608
82S184	7684
82S185	7685
82S190	76160
82S191	76161

FUJITSU	HARRIS
MB7056	7602
MB7051	7603
MB7057	7610/10A
MB7052	7611/11A
MB7058	7620/20A
MB7053	7620/21A
MB7059	7642
MB7054	7643
MB7060	7680
MB7055	7681

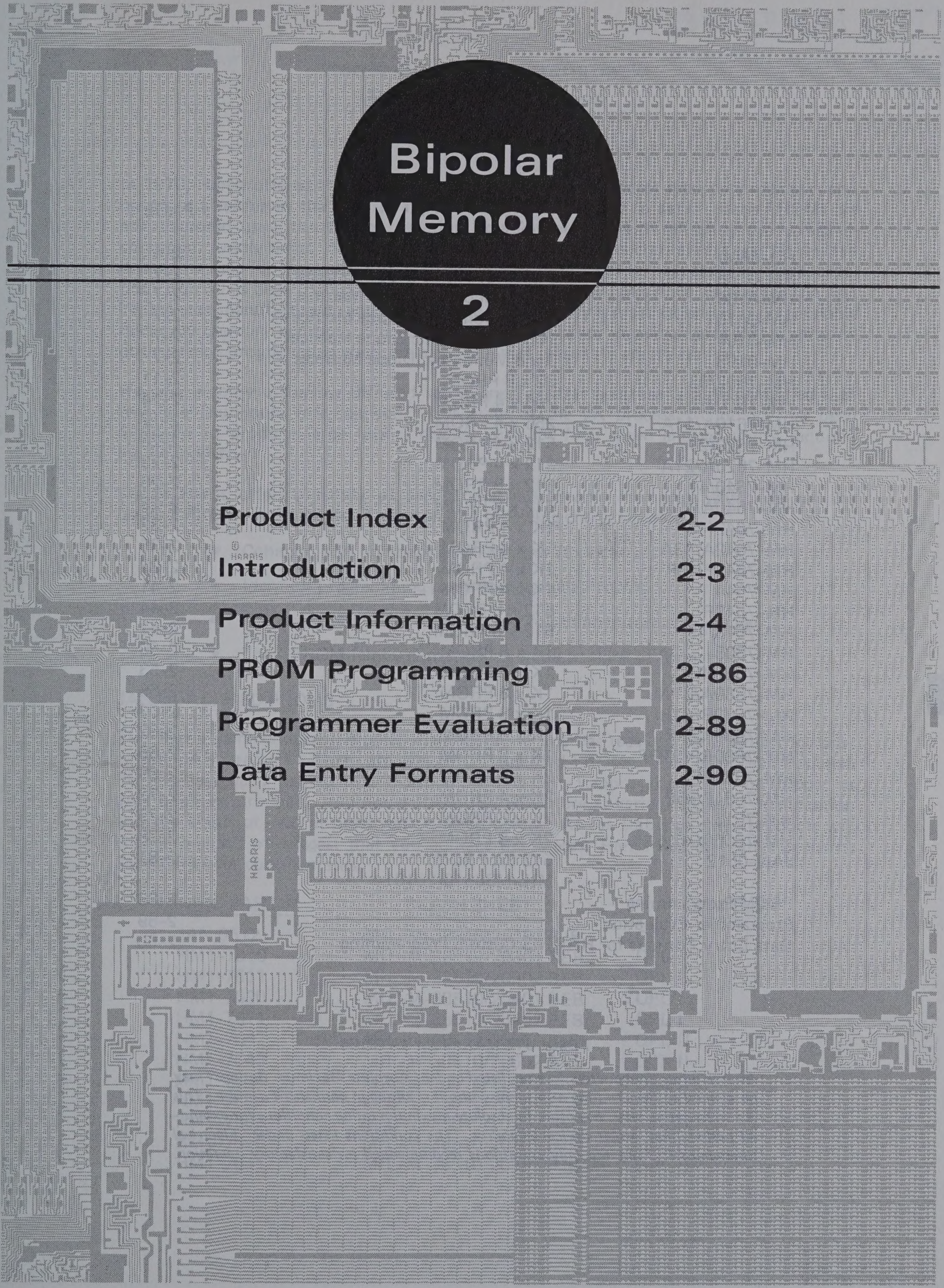
NMI	HARRIS
6330	7602
6331	7603
6300	7610/10A
6301	7611/11A
6305	7620/20A
6306	7621/21A
6348	7648
6340	7640/40A
6349	7649
6341	7641/41A
6352	7642
6353	7643
6380	7680
6381	7681
6385	7608
63100	7684
63101	7685

NEC	HARRIS
μPB403	7610/10A
μPB405	7640/40A
μPB425	7641/41A
μPB406	7642
μPB426	7643
μPB408	7680
μPB428	7681
μPB427	7608

TEXAS INST.	HARRIS
74S188/188A	7602
74S288	7603
74186	JAN 0512
74S387	7610/10A
74S287	7611/11A
74S473	7648
74S475	7640/40A
74S472	7649
74S474	7641/41A
74S477	7642
74S476	7643

Users' Guide to MOS Static RAMs

SIZE & ORGAN-IZATION	TYPE	PINS	HARRIS	AMD	AMI	EA	FUJITSU	GI	GTE	HITACHI	INTEL	INTERSIL	MICRO POWER SYSTEMS	MITEL	MITSUBISHI	MOSTEK	MOTOROLA	NATIONAL	NEC	OKI	RCA	SIGNETICS	SOLID STATE SCIENTIFIC	SYNERTEK	TI	TOSHIBA	ZILOG
64 x 12	CMOS	18	6512									6512															
1K	CMOS	16	6508		6508		8401					6508	6508	1902			7001 6508	6508 74C929	443		6508 5001 1821		5102	5102	6508	5508	
		18	6518		6518							6518	6518				6518	6518 74C930									
1K x 1	NMOS	16		9102	4015 4025						2102 2125					4102	2125 2115	2102	2102 2125			2102 2125		2102	2102 4033		
1K	CMOS	16	6562																								
		18	6561									6561						74C921 6552									
		22	6501		5101					435101	5101						145101		5101 510L		5040 5101			5101	5101	5007 5501	
		22 22	6551									6551						T4C920 6551			1822					5101	
256 x 4	NMOS	16		9112		2112					2112							2112			4112	2112 2606		2112	4043		
		18		2112 9111		2111					2111							2111	2111		4111	2111		2111 2112	4042		
		22		2101 9101		2101		4256			2101							2101	2101		4101	2101		2101	4039		
2K	CMOS	18	6503																								
2K x 1	NMOS	18																									
2K	CMOS	18	6513																								
512 x 4	NMOS	18									2113																
4K	CMOS	18	6504 6505				8404			4315 6147		6504 6505	6504				6504	6504 6847		5104						5504	
		20																									
4K x 1	NMOS	18		9145 9147	4017 2147		2147		4104 4200	6147 4847	2141 2147	2147				4104 2147	2147	2141 2147	4104 2147			2613		2147	2147 4044 4045	315D	4104 6104
		22		9140				4200																			
4K	CMOS	18	6514				8414			6148 4334		6514	6514	21C14	58981		6514	6514 6848	444	5114 5115	5114					5514	
		20																	445							5047	
1K x 4	NMOS	18		9124 9135 9114	2114				2114 4804	472114 6148	2114 2148	2148				2148	2114 2148	2148 2114	2114	2114		2614		2114	2114 4045 4047	314A	
		20		9148							2142							2141 2142						2142			
		22		9130 9131																							
8K	CMOS	24	6515																								
1K x 8	NMOS	24							8118							4118 4801			µPD 421-3								
16K	CMOS	24	6516							6116									µPD 446							5516	
2K x 8	NMOS	24														4802				2128					4016	2016	



Bipolar Memory

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HM-7640/41	512 x 8 PROM	2-26
HM-7640A/41A	512 x 8 PROM	2-29
HM-7642/43	1K x 4 PROM	2-32
HM-7642A/43A	1K x 4 PROM	2-35
HM-7642P/43P	1K x 4 PROM	2-38
HM-7644	1K x 4 PROM	2-41
HM-7647R	512 x 8 PROM	2-44
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HM-7608	1K x 8 PROM	2-50
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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Harris Generic Programmable Read Only Memories

In 1970, Harris offered the industry's first Bipolar programmable read only memory, and has been a leader in the field of Bipolar PROMs from 1970 to date. Harris PROMs are manufactured using the Bipolar Junction Isolation process with reliability proven nickel-chromium fusible links. Harris has had experience with nickel chromium since 1964 when it was first used for high reliability military circuits because of its high stability characteristics. Harris has been manufacturing nickel-chromium fuse links since 1970 when the first PROM was manufactured, and has become the industry's most extensive programmable read only memory concept. This history has been a factor in giving Harris PROMs the industry's high programming yield and a proven level of quality and reliability.

We now employ a shallow diffused self-aligned emitter aperture process combined with two-level aluminum interconnect. This state of the art process technology has been deployed to produce large format devices with the high speed and versatility required by the industry.

Today Harris offers a family of programmable read only memories which we call the Generic PROMs or GPROMs. They have the following characteristics:

- Coherent part numbering scheme, the 76xxx series.
- Identical programming procedure for all GPROMs.
- All parameters are guaranteed over full temperature and voltage.
- The GPROM family comprises a complete range of formats.

JAN QUALIFIED PROMS

The Harris Semiconductor Bipolar manufacturing line has received certification for processing JAN product. There are five QPL I qualified PROMs. Five additional HARRIS PROMs have been granted QPL II listing pending QPL I approval and may be shipped as JAN qualified product. Additional HARRIS PROMs are at various stages of qualification and the status of each at press time is listed below. As the status of these products will change rapidly, we suggest that you contact the nearest Harris Representative or Harris Sales Office for current status.

HARRIS PART #	SLASH SHEET	STATUS
JAN 0512	MIL-M-38510/20101 BJB	QPL I
HM1-7610	MIL-M-38510/20301 BEB	QPL I
HM1-7611	MIL-M-38510/20302 BEB	QPL I
HM1-7620	MIL-M-38510/20401 BEB	QPL I
HM1-7621	MIL-M-38510/20402 BEB	QPL I
HM1-7642	MIL-M-38510/20601 BVB	QPL II
HM1-7643	MIL-M-38510/20602 BVB	QPL II
HM1-7644	MIL-M-38510/20603 BEB	QPL II
HM1-7602	MIL-M-38510/20701 BEB	QPL II
HM1-7603	MIL-M-38510/20702 BEB	QPL II
HM1-7640	MIL-M-38510/20801 BJB	QPL II
HM1-7641	MIL-M-38510/20802 BJB	QPL II

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

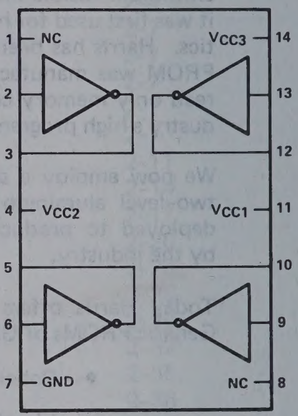
HD-6600
QUAD POWER STROBE

FEBRUARY 1978

Features

- HIGH DRIVE CURRENT—200mA
- HIGH SPEED 50ns TYPICAL
- TTL COMPATIBLE INPUTS
- DIELECTRIC ISOLATION
- QUAD MONOLITHIC CONSTRUCTION
- POWER SUPPLY FLEXIBILITY
- LOW POWER:
  - STANDBY—30mW/CIRCUIT
  - ACTIVE—95mW/CIRCUIT

Logic Diagram

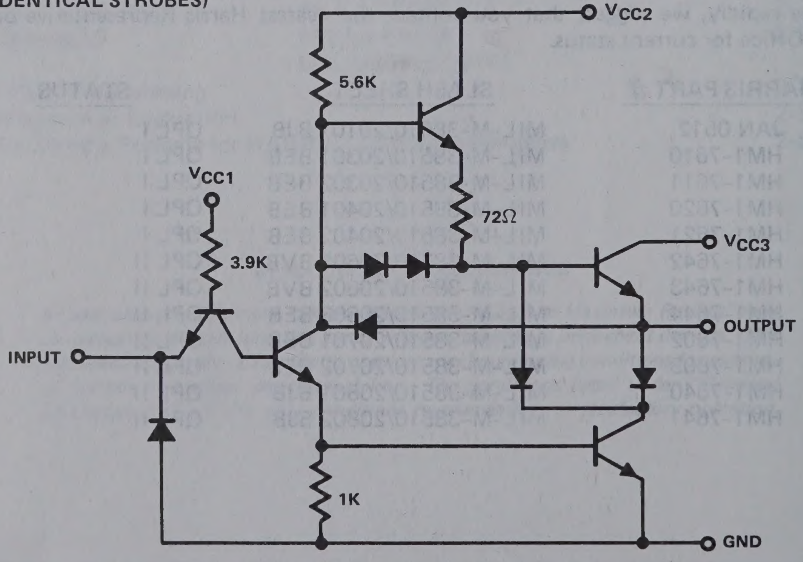

1
NC
2
3
4
VCC2
5
6
7
GND
14
VCC3
13
12
11
VCC1
10
9
8
NC

Description

The HD-6600 Quad Power Strobe is constructed with Harris Dielectric Isolation Bipolar Monolithic Process. The design incorporates power supply flexibility with TTL compatible inputs and high current outputs. This circuit is intended for use in power switched PROM arrays.

Circuit Diagram

(ONE OF FOUR IDENTICAL STROBES)


VCC2
5.6K
VCC1
72Ω
3.9K
VCC3
OUTPUT
INPUT
1K
GND

Specifications HD-6600

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{CC1}	+8 VDC
	V_{CC2}	+18 VDC
	V_{CC3}	+18 VDC
Input Voltage V_{IN}		-0.5 VDC to +5.5 VDC
Storage Temperature T_{STG}		-65°C to +150°C
Output Current I_L		-200mA
Power Dissipation at 25°C		1000mW (Derate 9mW/°C Above 60°C)

RECOMMENDED OPERATING CONDITIONS

Power Supplies:	V_{CC1}	5 VDC ± 10%
	V_{CC2}	12 VDC ± 15%
	V_{CC3}	5 VDC ± 20%

ELECTRICAL CHARACTERISTICS

T_A = -55°C to +125°C HD1-6600-2 V_{CC2} = 12.0 VDC
T_A = 0°C to +75°C HD1-6600-5 V_{CC3} = 5.0 VDC

D.C.

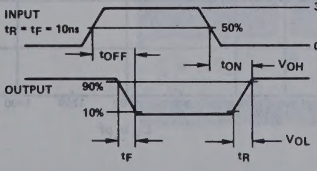
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
I_{IR}	Input Current			60	µA	V_{IN} = 2.4 VDC	V_{CC1} = 5.5 VDC
I_{IF}				-1.6	mA	V_{IN} = 0.4 VDC	
V_{IH}	Input Threshold Voltage	2.0			V	V_{CC1} = 4.5 VDC	
V_{IL}				0.8	V		
V_{OH}	Output Voltage (Note 1)	4.75	4.85		V	V_{CC1} = 5.0 VDC V_{IN} = 0.4 VDC	I_L = -150mA DC
V_{OL}				1.0	V	V_{CC1} = 5.0 VDC	I_L = 500µA DC
I_{CC1}	Supply Current (Note 2)		4	6.0	mA	V_{CC1} = 5.5 VDC	V_{IN} = 2.4 VDC
I_{CC2}			40	70	mA	V_{CC1} = 5.5 VDC V_{IN} = 0.4 VDC	I_L = -150mA DC
I_{CC2}			8	15	mA	V_{CC1} = 5.5 VDC V_{IN} = 2.4 VDC	I_L = 0

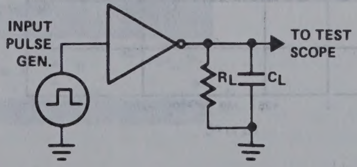
A.C.

SYMBOL	PARAMETER	TYP.	MAX.	UNITS	CONDITIONS T_A = 25°C
t_{ON}	Turn On Delay	50	75	ns	V_{CC1} = 5.0 VDC
t_{OFF}	Turn Off Delay	50	75	ns	V_{CC2} = 12 VDC
					V_{CC3} = 5.0 VDC
t_R	Rise Time	40	65	ns	R_L = 33Ω
t_F	Fall Time	40	65	ns	C_L = 620 pF

NOTES (1) One strobe enabled. (2) All strobes enabled.

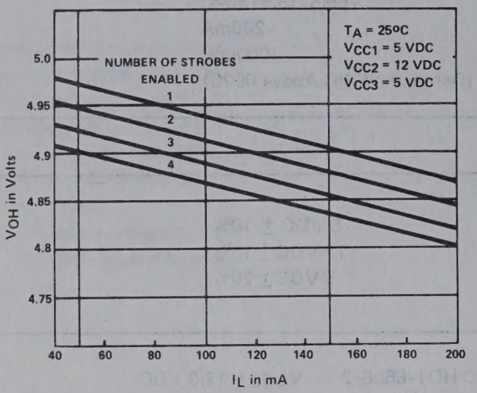
Switching Time Definitions



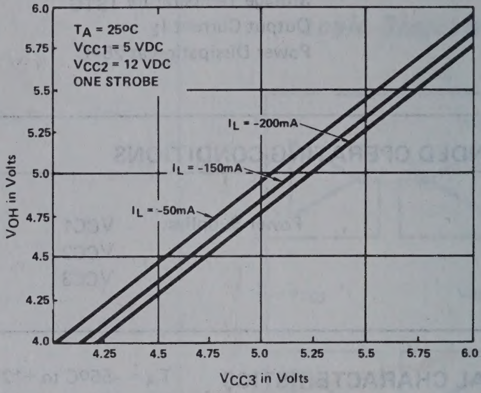


Typical Characteristics

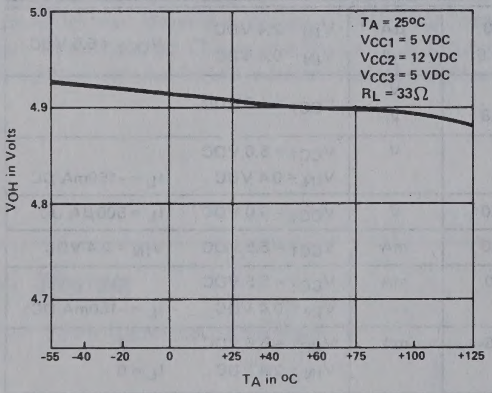
TYPICAL OUTPUT VOLTAGE vs.
LOAD CURRENT AND NUMBER OF STROBES ENABLED



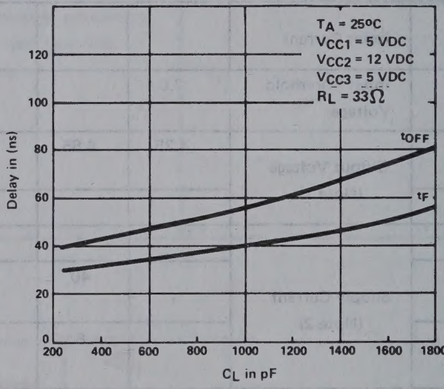
TYPICAL OUTPUT VOLTAGE vs.
V_{CC3} SUPPLY VOLTAGE



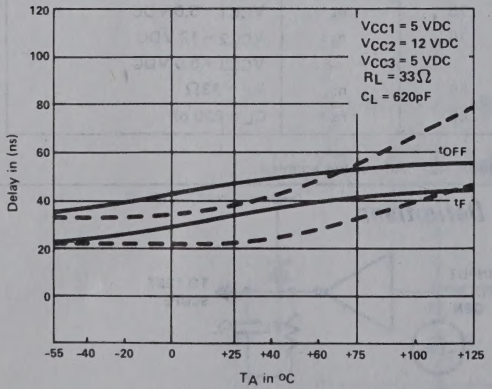
TYPICAL OUTPUT VOLTAGE vs.
AMBIENT TEMPERATURE



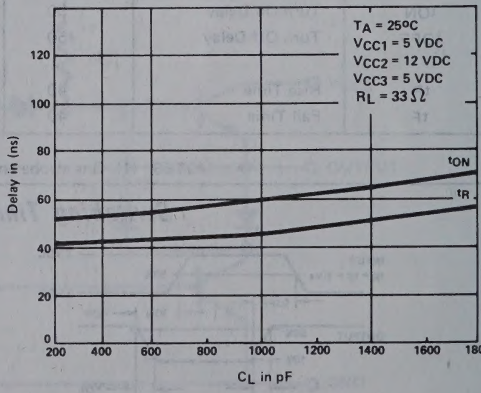
TYPICAL DELAY t_{OFF} AND t_F vs.
LOAD CAPACITANCE



TYPICAL DELAY vs.
AMBIENT TEMPERATURE



TYPICAL DELAY t_{ON} AND t_R vs.
LOAD CAPACITANCE



HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

MONOLITHIC DIODE MATRICES

Features

- FIELD PROGRAMMABLE
- CMOS COMPATIBLE
- ZERO POWER DISSIPATION
- FAST SWITCHING
- FIVE POPULAR ORGANIZATIONS

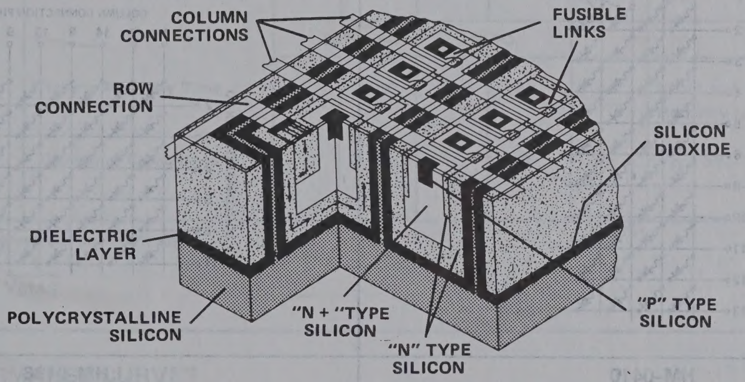
Description

Designed with the CMOS circuit engineer in mind, these versatile diode matrices allow the application of logically powerful programmable solutions to low power CMOS system applications.

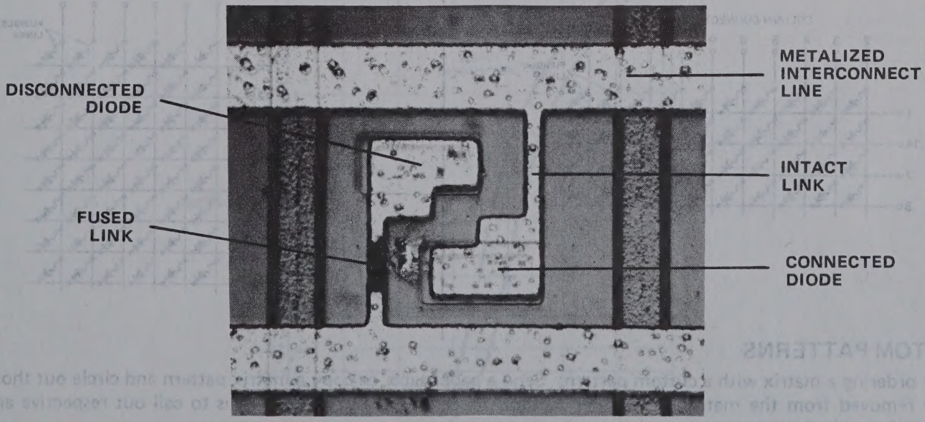
These devices incorporate an advanced dielectric isolation process to eliminate the need for power supply pins and allow parasitic free operation.

Programming is accomplished by cleanly vaporizing a fusible link by application of a brief high voltage pulse to a selected array element. This operation open circuits a row to column orring diode eliminating their former interaction.

Monolithic Structure


COLUMN CONNECTIONS
FUSIBLE LINKS
ROW CONNECTION
SILICON DIOXIDE
DIELECTRIC LAYER
POLYCRYSTALLINE SILICON
"N + "TYPE SILICON
"N" TYPE SILICON
"P" TYPE SILICON

Fusible Link System


METALIZED INTERCONNECT LINE
DISCONNECTED DIODE
INTACT LINK
FUSED LINK
CONNECTED DIODE

Monolithic Diode Matrices

HM-0168 6 x 8 DIODE MATRICES

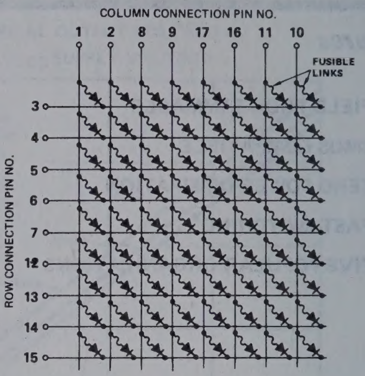
HM-0186 8 x 6 DIODE MATRICES

HM-0410 4 x 10 DIODE MATRICES

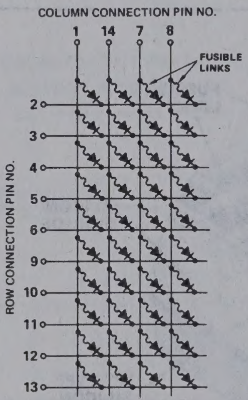
HM-0104 10 x 4 DIODE MATRICES

HM-0198 9 x 8 DIODE MATRICES

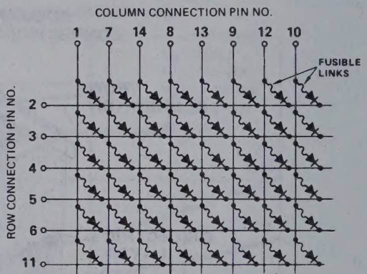
HM-0198


COLUMN CONNECTION PIN NO.
1 2 8 9 17 16 11 10
FUSIBLE LINKS
ROW CONNECTION PIN NO.
3
4
5
6
7
12
13
14
15

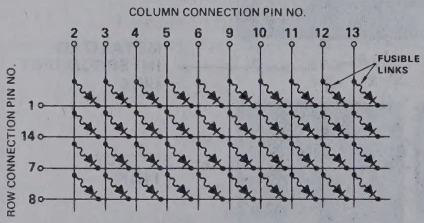
HM-0104


COLUMN CONNECTION PIN NO.
1 14 7 8
FUSIBLE LINKS
ROW CONNECTION PIN NO.
2
3
4
5
6
9
10
11
12
13

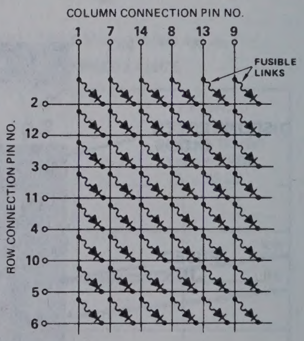
HM-0168


COLUMN CONNECTION PIN NO.
1 7 14 8 13 9 12 10
FUSIBLE LINKS
ROW CONNECTION PIN NO.
2
3
4
5
6
11

HM-0410


COLUMN CONNECTION PIN NO.
2 3 4 5 6 9 10 11 12 13
FUSIBLE LINKS
ROW CONNECTION PIN NO.
1
14
7
8

HM-0186


COLUMN CONNECTION PIN NO.
1 7 14 8 13 9
FUSIBLE LINKS
ROW CONNECTION PIN NO.
2
12
3
11
4
10
5
6

CUSTOM PATTERNS

When ordering a matrix with a custom pattern: Send a paper tape, or copy a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify a pattern is to call out respective anode and cathode for each diode to be removed, by package pin number.

Specifications Diode Matrices

ABSOLUTE MAXIMUM RATINGS

Forward Current	100mA
Surge Current (100 μs Max.)	200mA
Total Ckt. Dissipation (Still Air)	450mW
Storage Temperature (Ambient)	-65°C to +150°C

Maximum Ratings are limiting values above which permanent damage may occur.

ELECTRICAL CHARACTERISTICS

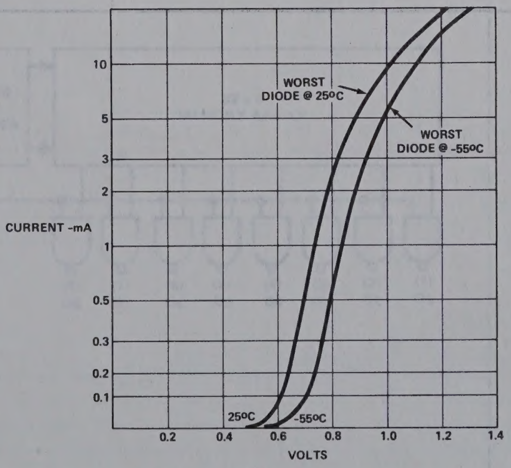
		HM-0XXX-5		HM-0XXX-2 HM-0XXX-8			
	T_A	0°C to +75°C		-55°C to +125°C			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
V_F	Forward Voltage		1.5 0.9		1.5 .9	V V	$I_F = 20mA$ $I_F = 1mA$
BV_R	Reverse Breakdown Voltage	20		30		V	$I_{BV} = 100\mu A$
		25°C		25°C			
t_{rr}	Reverse Recovery Time		100		50	ns	$I_F = 10mA$ to $I_R = 10mA$ Recovery to 1mA
C_C	Crosspoint Capacitance (1)				8	pF	$V_R = 5V$; f = 1MHz (2)

(1) Guaranteed but not 100% tested.

(2) $C_C \propto \frac{1}{V_{BIAS}}$

TYPICAL PERFORMANCE CURVES

VOLTAGE V_f

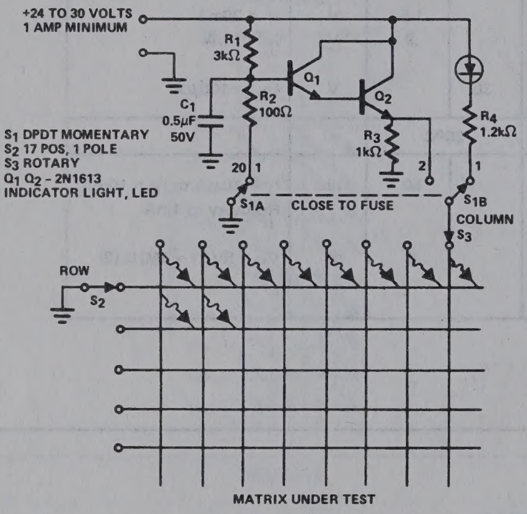


Programming

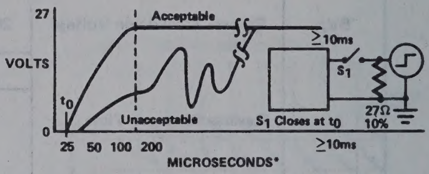
Use a simple supply capable of driving a 27 ohm resistor (carbon) with a clean transition from 0 to 24–30 volts in less than 500μs, for at least 10ms. The diode to be disconnected is selected by setting the row and column switches S2 and S3 respectively as required. When switch S1 is depressed, programming current is provided to column contacts in the matrix. This current opens the fusible link, in series with the selected diode. The peak fusing current required to open a fusible link is approximately 750 milliamperes. As the temperature of the fuse is raised, the aluminum begins to melt. This melting continues until the fuse link separates. The cohesive forces of the melting aluminum retracts the remaining portions of the metal, thereby preventing formation of loose aluminum residues. The melting temperature of aluminum (approximately 650°C) will not affect the passivating layer of silicon dioxide, whose melting temperature is about 1350°C. Test verification is obtained by an indicator lamp or LED placed in series with the column and row switches through the verify contacts of S1 to give electrical indication of the condition of each diode in the matrix before and after fusing.

Caution: Programming is limited to one fuse at a time.

SIMPLE PROGRAMMER


+24 TO 30 VOLTS
1 AMP MINIMUM
R1
3kΩ
Q1
Q2
C1
0.5μF
50V
R2
100Ω
R3
1kΩ
R4
1.2kΩ
S1 DPDT MOMENTARY
S2 17 POS, 1 POLE
S3 ROTARY
Q1 Q2 - 2N1613
INDICATOR LIGHT, LED
20
1
2
1
S1A
CLOSE TO FUSE
S1B
COLUMN
S3
ROW
S2
MATRIX UNDER TEST

PROGRAMMER TEST CONFIGURATION


27
VOLTS
0
Acceptable
Unacceptable
t0
25 50 100 200
MICROSECONDS*
≥10ms
S1
27Ω
10%
S1 Closes at t0
≥10ms

*Max T_{RISE} = 500μsec

NOTE: The 27 ohm resistor is only used for oscilloscope measurements of the Power Supply Characteristics becaues it represents a typical unprogrammed fuse/diode.

HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7602/03

32 x 8 PROM

HM-7602 — Open Collector Outputs
HM-7603 — "Three State" Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7602/03 is a fully decoded high speed Schottky TTL 256/Bit Field Programmable ROM in a 32 word by 8 bit/word format with open collector (HM-7602) or "Three State" (HM-7603) outputs. These PROMs are available in a 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

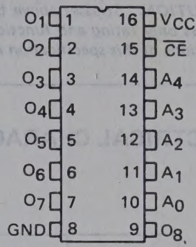
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7602/03 contains test rows which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows are blown prior to shipment.

There is one chip enable input on the HM-7602/03. $\overline{CE}$ low enables the chip.

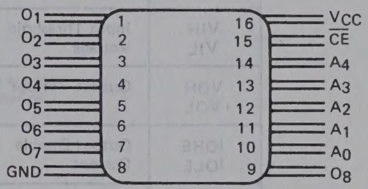
Pinouts

TOP VIEW – DIP



O1 1
O2 2
O3 3
O4 4
O5 5
O6 6
O7 7
GND 8
16 VCC
15 CE
14 A4
13 A3
12 A2
11 A1
10 A0
9 O8

TOP VIEW – FLATPACK

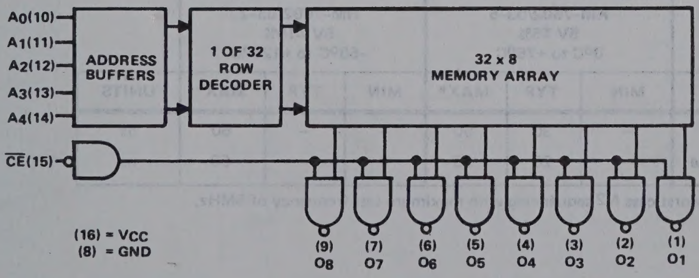


O1 1
O2 2
O3 3
O4 4
O5 5
O6 6
O7 7
GND 8
16 VCC
15 CE
14 A4
13 A3
12 A2
11 A1
10 A0
9 O8

PIN NAMES

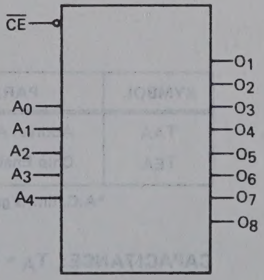
A0 – A4	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}$	Chip Enable Inputs

Functional Diagram



A0(10)
A1(11)
A2(12)
A3(13)
A4(14)
ADDRESS BUFFERS
1 OF 32 ROW DECODER
32 x 8 MEMORY ARRAY
CE(15)
(16) = VCC
(8) = GND
(9) O8
(7) O7
(6) O6
(5) O5
(4) O4
(3) O3
(2) O2
(1) O1

Logic Symbol



CE
A0
A1
A2
A3
A4
O1
O2
O3
O4
O5
O6
O7
O8

Specifications HM-7602/03

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7602/03-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7602/03-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	— —	— -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 —	1.5 1.5	— 0.8	V V	V_{CC} = V_{CC} Min V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output Voltage "1" "0"	2.4* —	3.2* 0.35	— 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	— —	— —	+100 -100	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	—	—	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	—	-100*	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	—	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

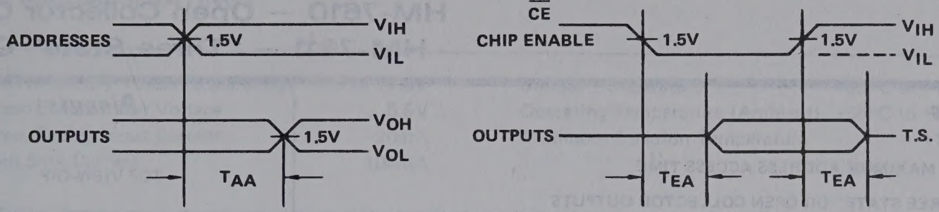
		HM-7602/03-5 5V ±5% 0°C to +75°C			HM-7602/03-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS
T_{AA}	Address Access Time	—	30	50	—	—	60	ns
T_{EA}	Chip Enable Access Time	—	20	35	—	—	50	ns

*A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

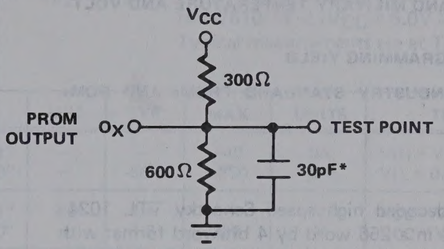
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE
CHIP ENABLE
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

A. C. TEST LOAD


VCC
300Ω
PROM OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

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PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7610/11

256 x 4 PROM

HM-7610 — Open Collector Outputs
HM-7611 — "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- INPUTS AND OUTPUT TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROMs AND ROMs

Description

The HM-7610/11 are fully decoded high speed Schottky TTL 1024-Bit Field Programmable ROMs in a 256 word by 4 bit/word format with open collector (HM-7610) or "three state" (HM-7611) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

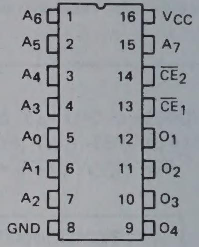
The HM-7610/11 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

2

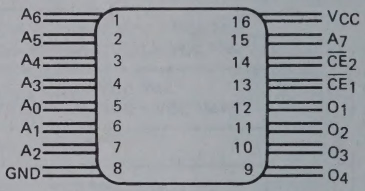
Pinouts

TOP VIEW–DIP



A_6 1
A_5 2
A_4 3
A_3 4
A_0 5
A_1 6
A_2 7
GND 8
16 V_{CC}
15 A_7
14 $\overline{CE}_2$
13 $\overline{CE}_1$
12 O_1
11 O_2
10 O_3
9 O_4

TOP VIEW–FLATPACK

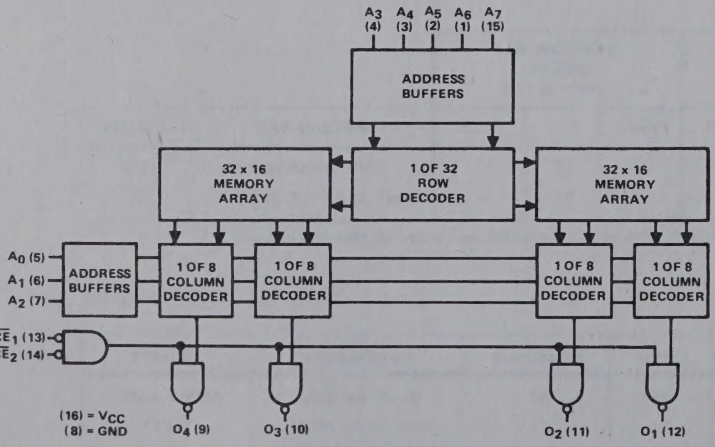


A_6 1
A_5 2
A_4 3
A_3 4
A_0 5
A_1 6
A_2 7
GND 8
16 V_{CC}
15 A_7
14 $\overline{CE}_2$
13 $\overline{CE}_1$
12 O_1
11 O_2
10 O_3
9 O_4

PIN NAMES

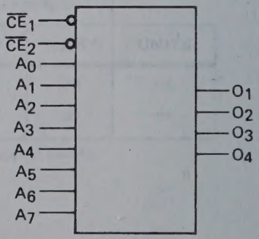
$A_0 - A_7$	Address Inputs
$\overline{CE}_1 - \overline{CE}_2$	Chip Enable Inputs
$O_1 - O_4$	Data Outputs

Functional Diagram



A_3 (4) A_4 (3) A_5 (2) A_6 (1) A_7 (15)
ADDRESS BUFFERS
32 x 16 MEMORY ARRAY
1 OF 32 ROW DECODER
32 x 16 MEMORY ARRAY
A_0 (5)
A_1 (6)
A_2 (7)
ADDRESS BUFFERS
1 OF 8 COLUMN DECODER
1 OF 8 COLUMN DECODER
1 OF 8 COLUMN DECODER
1 OF 8 COLUMN DECODER
$\overline{CE}_1$ (13)
$\overline{CE}_2$ (14)
(16) = V_{CC}
(8) = GND
O_4 (9)
O_3 (10)
O_2 (11)
O_1 (12)

Logic Symbol



$\overline{CE}_1$
$\overline{CE}_2$
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
O_1
O_2
O_3
O_4

Specifications HM-7610/11

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7610/11-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7610/11-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	"0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+100	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-100	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals
*Not applicable to open collector.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

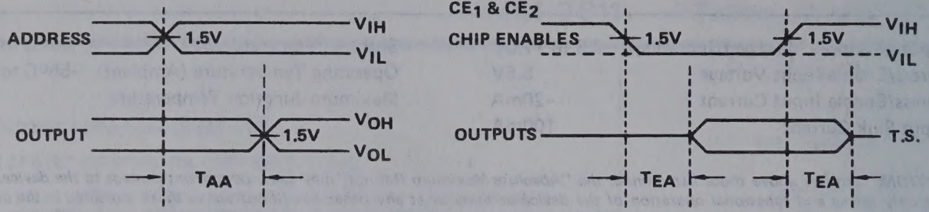
		HM-7610/11-5 5V ±5% 0°C to +75°C			HM-7610/11-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS
T_{AA}	Address Access Time	–	40	60	–	–	75	ns
T_{EA}	Chip Enable Access Time	–	15	25	–	–	30	ns

*A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

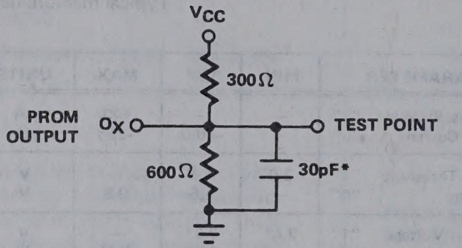
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESS
1.5V
V_{IH}
V_{IL}
OUTPUT
1.5V
V_{OH}
V_{OL}
T_{AA}
$\overline{CE}_1$ & $\overline{CE}_2$
CHIP ENABLES
1.5V
V_{IH}
1.5V
V_{IL}
OUTPUTS
T.S.
T_{EA}
T_{EA}

A. C. TEST LOAD


V_{CC}
300Ω
PROM OUTPUT
O_X
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

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HM-7610A/11A
HIGH SPEED 256 x 4 PROM
HM-7610A - Open Collector Outputs
HM-7611A - "Three State" Outputs

Features

- 45ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CAST N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's

Description

The HM-7610A/11A are fully decoded high speed Schottky TTL 1024-Bit Field Programmable ROMs in a 256 word by 4 bit/word format with open collector (HM-7610A) or "three state" (HM-7611A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

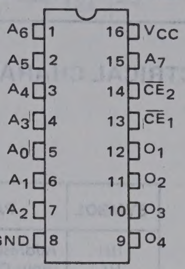
The HM-7610A/11A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art high speed logic systems.

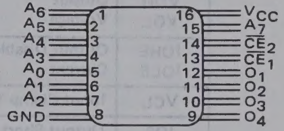
Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

Pinouts

TOP VIEW—DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 CE2
13 CE1
12 O1
11 O2
10 O3
9 O4

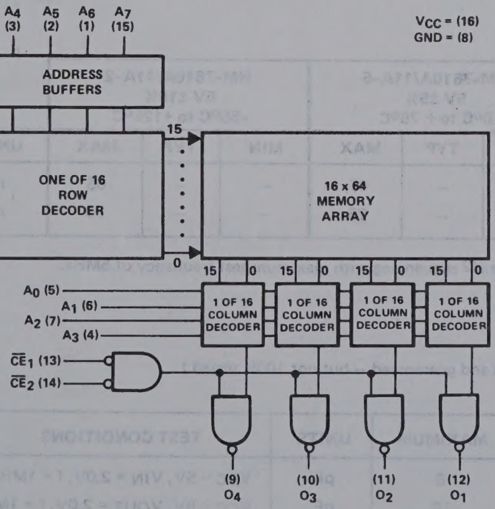
TOP VIEW—FLAT PACK


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 CE2
13 CE1
12 O1
11 O2
10 O3
9 O4

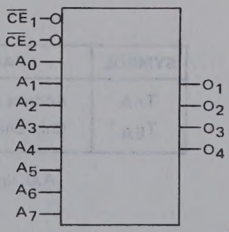
PIN NAMES

$A_0 - A_7$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}_1, \overline{CE}_2$	Chip Enable Inputs

Functional Diagram


A4 (3)
A5 (2)
A6 (1)
A7 (15)
VCC = (16)
GND = (8)
ADDRESS BUFFERS
ONE OF 16 ROW DECODER
15
0
16 x 64 MEMORY ARRAY
15 0 15 0 15 0 15 0
A0 (5)
A1 (6)
A2 (7)
A3 (4)
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
CE1 (13)
CE2 (14)
(9) O4
(10) O3
(11) O2
(12) O1

Logic Symbol


CE1
CE2
A0
A1
A2
A3
A4
A5
A6
A7
O1
O2
O3
O4

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7610A/11A-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7610A/11A-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable Input Current	"1" "0"	— —	— -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold Voltage	"1" "0"	2.0 —	1.5 1.5	— 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output Voltage	"1" "0"	2.4* —	3.2* 0.35	— 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable Current	"1" "0"	— —	— —	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage		—	—	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current *		-15*	—	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current		—	—	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*Not applicable to open collector.
NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

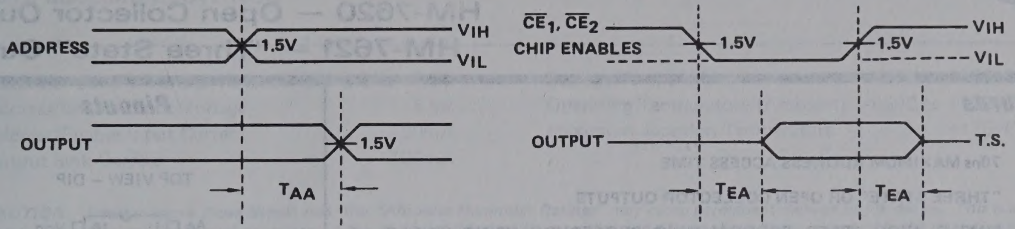
		HM-7610A/11A-5 5V ±5% 0°C to + 75°C			HM-7610A/11A-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	—	—	45	—	—	65	ns
T_{EA}	Chip Enable Access Time	—	—	25	—	—	30	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

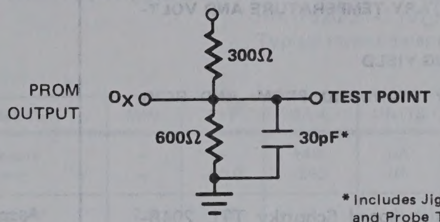
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed — but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESS
1.5V
VIH
VIL
OUTPUT
1.5V
TAA
CE1, CE2
CHIP ENABLES
1.5V
1.5V
VIH
VIL
OUTPUT
T.S.
TEA
TEA

A.C. TEST LOAD


300Ω
PROM
OUTPUT
Ox
TEST POINT
600Ω
30pF*

*Includes Jig
and Probe Total
Capacitance

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HM-7620/21

512 x 4 PROM

HM-7620 — Open Collector Outputs
HM-7621 — "Three State" Outputs

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- INPUTS AND OUTPUT TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROMs AND ROMs

Description

The HM-7620/21 are fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROMs in a 512 word by 4 bit/word format with open collector (HM-7620) or "three state" (HM-7621) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

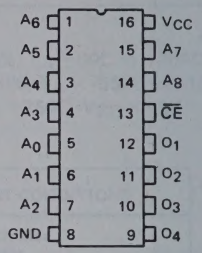
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

The HM-7620/21 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

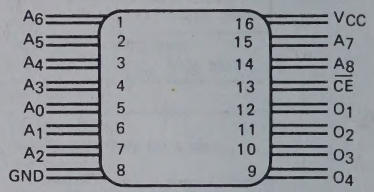
Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

Pinouts

TOP VIEW – DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 A8
13 CE
12 O1
11 O2
10 O3
9 O4

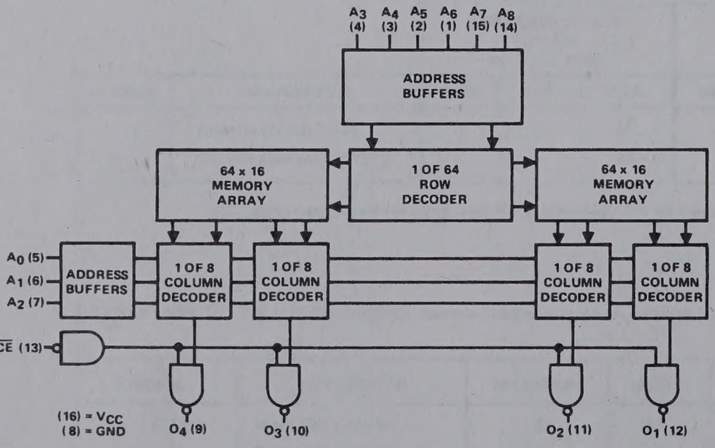
TOP VIEW – FLATPACK


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 A8
13 CE
12 O1
11 O2
10 O3
9 O4

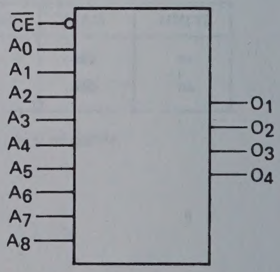
PIN NAMES

A0 – A8	Address Inputs
$\overline{CE}$	Chip Enable Input
O1 – O4	Data Outputs

Functional Diagram


A3 (4)
A4 (3)
A5 (2)
A6 (1)
A7 (15)
A8 (14)
ADDRESS BUFFERS
64 x 16 MEMORY ARRAY
1 OF 64 ROW DECODER
64 x 16 MEMORY ARRAY
A0 (5)
A1 (6)
A2 (7)
ADDRESS BUFFERS
1 OF 8 COLUMN DECODER
1 OF 8 COLUMN DECODER
1 OF 8 COLUMN DECODER
1 OF 8 COLUMN DECODER
CE (13)
(16) = VCC
(8) = GND
O4 (9)
O3 (10)
O2 (11)
O1 (12)

Logic Symbol


CE
A0
A1
A2
A3
A4
A5
A6
A7
A8
O1
O2
O3
O4

Specifications HM-7620/21

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7620/21-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7620/21-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	"0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+100	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-100	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

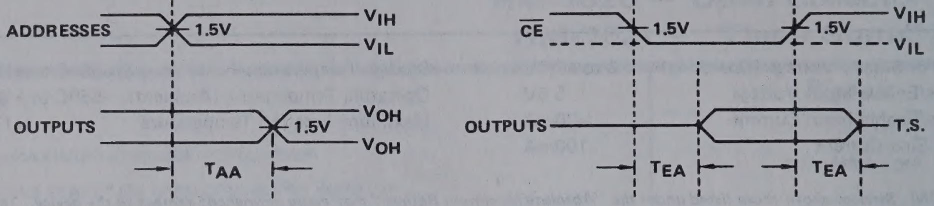
		HM-7620/21-5 5V ±5% 0°C to +75°C			HM-7620/21-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS
T_{AA}	Address Access Time	–	45	70	–	–	85	ns
T_{EA}	Chip Enable Access Time	–	15	25	–	–	30	ns

*A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

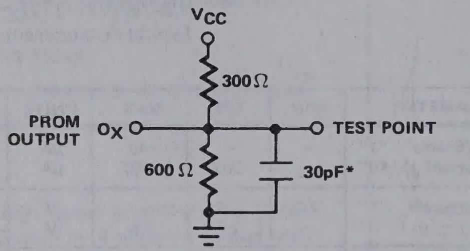
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOH
TAA
CE
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

A. C. TEST LOAD


VCC
300 Ω
PROM OUTPUT
OX
TEST POINT
600 Ω
30pF*

* Includes jig & probe total capacitance

HM-7620A/21A

HIGH SPEED 512 x 4 PROM

HM-7620A - Open Collector Outputs
HM-7621A - "Three State" Outputs

Features

- **50ns** MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's.

Description

The HM-7620A/21A are fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM's in a 512 word by 4 bit/word format with open collector (HM-7620A) or "three state" (HM-7621A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

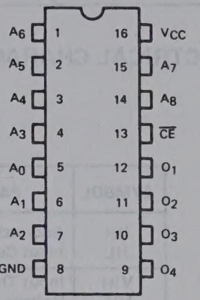
The HM-7620A/21A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art high speed logic systems.

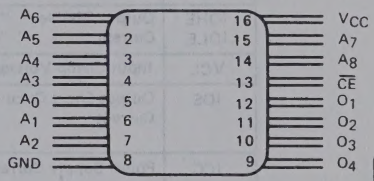
Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

Pinouts

TOP VIEW - DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 A8
13 CE
12 O1
11 O2
10 O3
9 O4

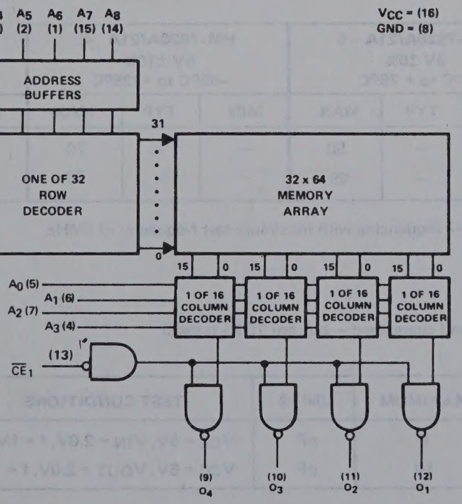
TOP VIEW – FLATPACK


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 A8
13 CE
12 O1
11 O2
10 O3
9 O4

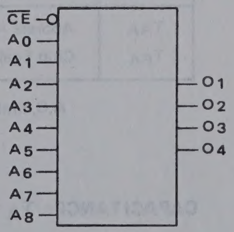
PIN NAMES

A0 – A8	Address Inputs
$\overline{CE}$	Chip Enable Input
O1 – O4	Data Outputs

Functional Diagram


A4 (3)
A5 (2)
A6 (1)
A7 (15)
A8 (14)
VCC = (16)
GND = (8)
ADDRESS BUFFERS
31
ONE OF 32 ROW DECODER
0
32 x 64 MEMORY ARRAY
15
0
A0 (5)
A1 (6)
A2 (7)
A3 (4)
1 OF 16 COLUMN DECODER
(13)
CE1
(9) O4
(10) O3
(11) O2
(12) O1

Logic Symbol


CE
A0
A1
A2
A3
A4
A5
A6
A7
A8
O1
O2
O3
O4

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7620A/21A-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7620A/21A-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*"Three State" only

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

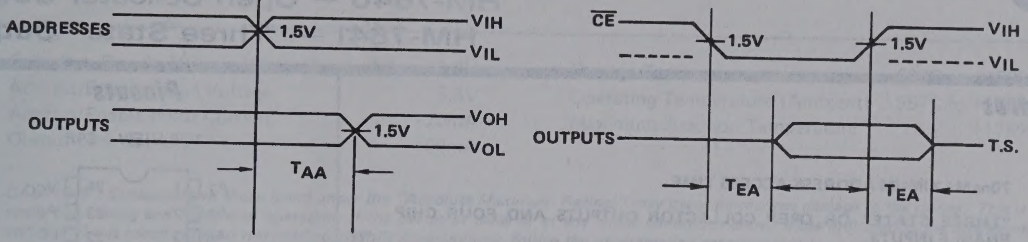
		HM-7620A/21A - 5 5V ±5% 0°C to + 75°C			HM-7620A/21A -2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	–	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	–	25	–	–	30	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

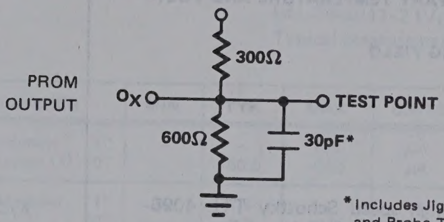
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

A.C. TEST LOAD


300Ω
PROM
OUTPUT
OX
TEST POINT
600Ω
30pF*

*Includes Jig and Probe Total Capacitance

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PRODUCTS DIVISION
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HM-7640/41

512 x 8 PROM

HM-7640 — Open Collector Outputs
HM-7641 — "Three State" Outputs

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME — GUARANTEED FOR WORST CASE N² SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7640/41 are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

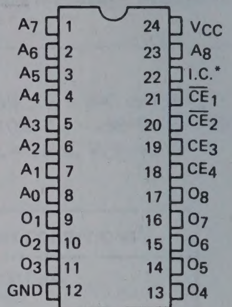
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7640/41 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

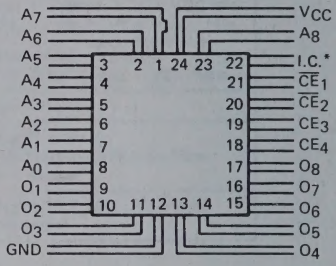
There are four chip enable inputs on the HM-7640/41 where $\overline{CE}_1$, and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Pinouts

TOP VIEW – DIP


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 I.C.*
21 CE1
20 CE2
19 CE3
18 CE4
17 O8
16 O7
15 O6
14 O5
13 O4

TOP VIEW – FLATPACK

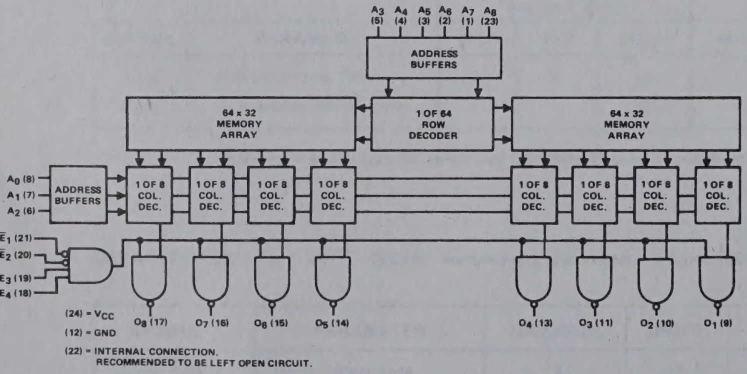

A7
A6
A5
A4
A3
A2
A1
A0
O1
O2
O3
GND
VCC
A8
I.C.*
CE1
CE2
CE3
CE4
O8
O7
O6
O5
O4
3 2 1 24 23 22
4 21
5 20
6 19
7 18
8 17
9 16
10 11 12 13 14 15

PIN NAMES

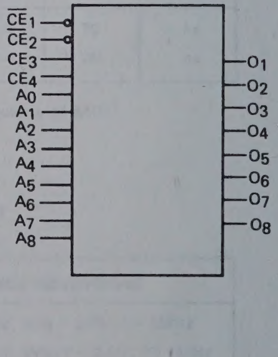
$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Inputs

*Internal connection. Recommended to be left open circuit.

Functional Diagram


A3 (5)
A4 (4)
A5 (3)
A6 (2)
A7 (1)
A8 (23)
ADDRESS BUFFERS
64 x 32 MEMORY ARRAY
1 OF 64 ROW DECODER
64 x 32 MEMORY ARRAY
A0 (8)
A1 (7)
A2 (6)
ADDRESS BUFFERS
1 OF 8 COL. DEC.
CE1 (21)
CE2 (20)
CE3 (19)
CE4 (18)
O8 (17)
O7 (16)
O6 (15)
O5 (14)
O4 (13)
O3 (11)
O2 (10)
O1 (9)
(24) = VCC
(12) = GND
(22) = INTERNAL CONNECTION. RECOMMENDED TO BE LEFT OPEN CIRCUIT.

Logic Symbol


CE1
CE2
CE3
CE4
A0
A1
A2
A3
A4
A5
A6
A7
A8
O1
O2
O3
O4
O5
O6
O7
O8

Specifications HM-7640/41

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640/41-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7640/41-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable Input Current (1) "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	"0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold Voltage "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min
V_{IL}	"0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	2.4 (2)	3.2 (2)	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	"0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable Current "1"	–	–	+100	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	"0"	–	–	-100	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals
(1) Enable Current measured using only one enable input to disable the device.
(2) "Three State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

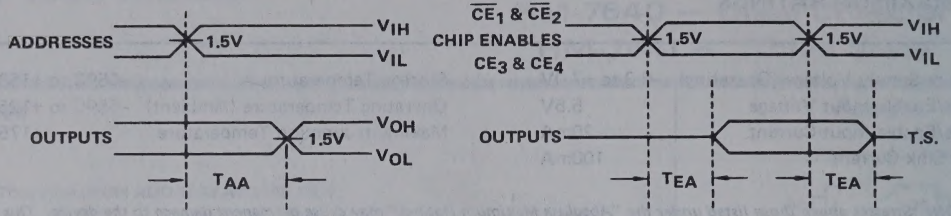
		HM-7640/41 5V ±5% 0°C to +75°C			HM-7640/41 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	70	–	–	85	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C

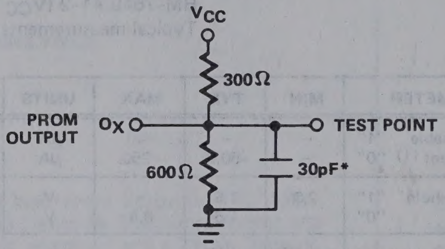
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS



ADDRESSES
1.5V
V_{IH}
V_{IL}
OUTPUTS
1.5V
V_{OH}
V_{OL}
T_{AA}
$\overline{CE_1}$ & $\overline{CE_2}$
CHIP ENABLES
CE_3 & CE_4
1.5V
1.5V
V_{IH}
V_{IL}
OUTPUTS
T.S.
T_{EA}
T_{EA}

A. C. TEST LOAD



V_{CC}
300Ω
PROM OUTPUT
O_X
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

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HM-7640A/41A
HIGH SPEED 512 x 8 PROM
HM-7640A - Open Collector Outputs
HM-7641A - "Three State" Outputs

Preliminary

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIPS ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME — GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW INPUT LOADING

Description

The HM-7640A/41A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

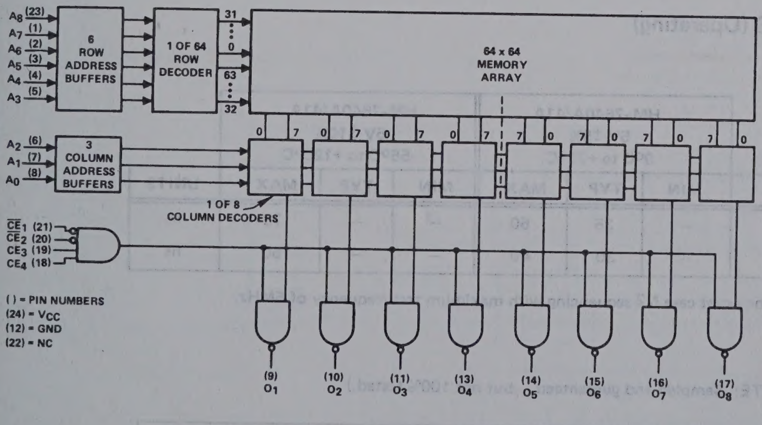
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7640A/41A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

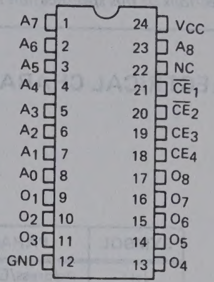
There are four chip enable inputs on the HM-7640A/41A where $\overline{CE}_1$, and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Functional Diagram

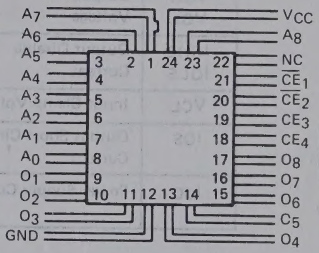

A8 (23)
A7 (1)
A6 (2)
A5 (3)
A4 (4)
A3 (5)
6 ROW ADDRESS BUFFERS
1 OF 64 ROW DECODER
31
0
63
32
64 x 64 MEMORY ARRAY
0 7 0 7 0 7 0 7 7 0 7 0 7 0 7 0
A2 (6)
A1 (7)
A0 (8)
3 COLUMN ADDRESS BUFFERS
1 OF 8 COLUMN DECODERS
CE1 (21)
CE2 (20)
CE3 (19)
CE4 (18)
( ) = PIN NUMBERS
(24) = VCC
(12) = GND
(22) = NC
(9) O1
(10) O2
(11) O3
(13) O4
(14) O5
(15) O6
(16) O7
(17) O8

Pinouts

TOP VIEW — DIP


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 NC
21 CE1
20 CE2
19 CE3
18 CE4
17 O8
16 O7
15 O6
14 O5
13 O4

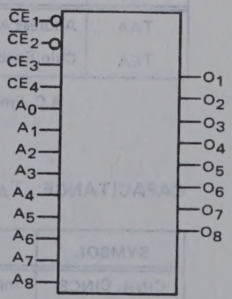
TOP VIEW — FLATPACK


A7
A6
A5
A4
A3
A2
A1
A0
O1
O2
O3
GND
3 2 1 24 23 22
4
5
6
7
8
9
10 11 12 13 14 15
21
20
19
18
17
16
VCC
A8
NC
CE1
CE2
CE3
CE4
O8
O7
O6
C5
O4

PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, CE_3, CE_4$	Chip Enable Inputs

Logic Symbol


CE1
CE2
CE3
CE4
A0
A1
A2
A3
A4
A5
A6
A7
A8
O1
O2
O3
O4
O5
O6
O7
O8

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640A/41A-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7640A/41A-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

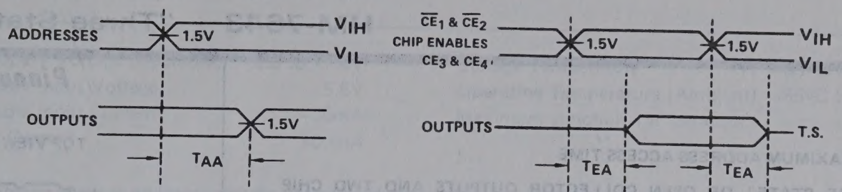
		HM-7640A/41A 5V ±5% 0°C to +75°C			HM-7640A/41A 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

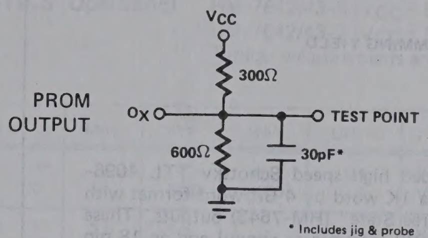
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
V_IH
V_IL
1.5V
OUTPUTS
1.5V
T_AA
CE̅1 & CE̅2
CHIP ENABLES
CE3 & CE4
1.5V
1.5V
V_IH
V_IL
OUTPUTS
T.S.
T_EA
T_EA

A.C. TEST LOAD


VCC
300Ω
PROM
OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

2

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7642/43

1K x 4 PROM

HM-7642 — Open Collector Outputs
HM-7643 — "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7642/43 are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 1K word by 4 Bit/word format with open collector (HM-7642) or "Three State" (HM-7643) outputs. These PROMs are avaliable in an 18 pin DIP (ceramic or epoxy) and an 18 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

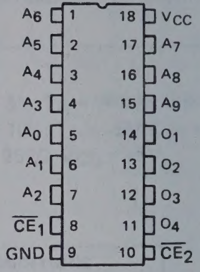
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7642/43 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

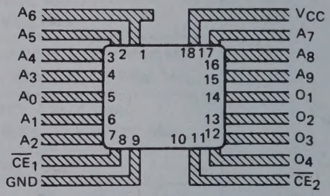
There are two chip enable inputs on the HM-7642/43. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinouts

TOP VIEW – DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CE1 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 O1
13 O2
12 O3
11 O4
10 CE2

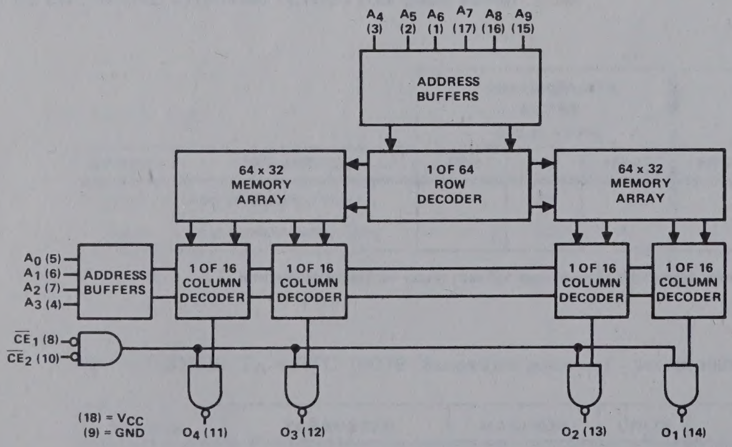
TOP VIEW – FLATPACK


A6
A5
A4
A3
A0
A1
A2
CE1
GND
VCC
A7
A8
A9
O1
O2
O3
O4
CE2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18

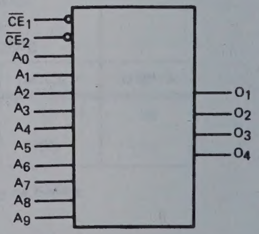
PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}_1, \overline{CE}_2$	Chip Enable Inputs

Functional Diagram


A4 (3)
A5 (2)
A6 (1)
A7 (17)
A8 (16)
A9 (15)
ADDRESS BUFFERS
64 x 32 MEMORY ARRAY
1 OF 64 ROW DECODER
64 x 32 MEMORY ARRAY
A0 (5)
A1 (6)
A2 (7)
A3 (4)
ADDRESS BUFFERS
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
CE1 (8)
CE2 (10)
(18) = VCC
(9) = GND
O4 (11)
O3 (12)
O2 (13)
O1 (14)

Logic Symbol


CE1
CE2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

*CAUTION: Stresses above those listed under the "**Absolute** Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)*

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642/43-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642/43-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output Voltage "1" "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+100 -100	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

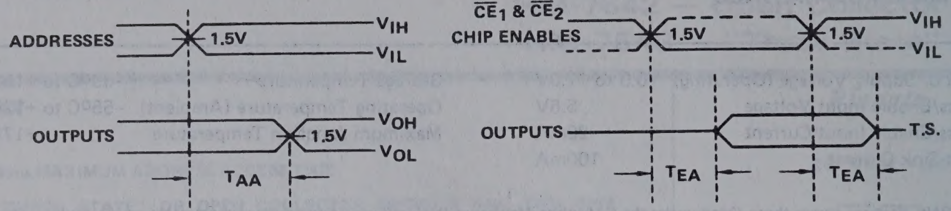
		HM-7642/43 5V ±5% 0°C to +75°C			HM-7642/43 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	85	ns
T_{EA}	Chip Enable Access Time	–	15	25	–	–	30	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

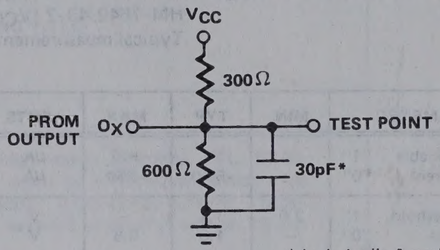
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE1 & CE2
CHIP ENABLES
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

A. C. TEST LOAD


VCC
300Ω
PROM
OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7642A/43A
HIGH SPEED 1K x 4 PROM
HM-7642A - Open Collector Outputs
HM-7643A - "Three State" Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642A/43A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 1K words by 4 Bit/word format with open collector(HM-7642A) or "Three State" (HM-7643A) outputs. These PROM's are available in an 18–pin DIP (ceramic or epoxy) and an 18–pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

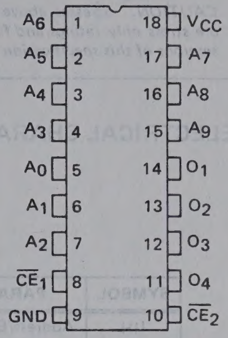
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7642A/43A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7642A/43A. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

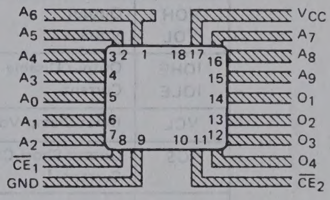
Pinout

TOP VIEW—DIP



A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
$\overline{CE}_1$ 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 O1
13 O2
12 O3
11 O4
10 $\overline{CE}_2$

TOP VIEW—FLAT PACK

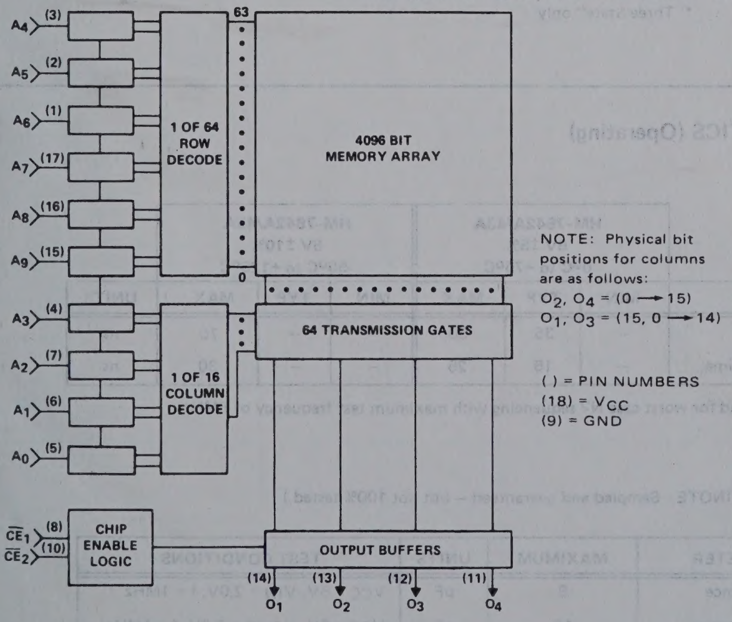


A6
A5
A4
A3
A0
A1
A2
$\overline{CE}_1$
GND
3 2 1 18 17 16
4 15
5 14
6 13
7 8 9 10 11 12
VCC
A7
A8
A9
O1
O2
O3
O4
$\overline{CE}_2$

PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1, \overline{CE}_2$	CHIP ENABLE INPUTS

Functional Diagram

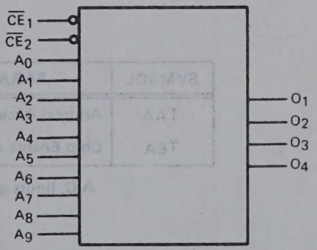


A4 (3)
A5 (2)
A6 (1)
A7 (17)
A8 (16)
A9 (15)
A3 (4)
A2 (7)
A1 (6)
A0 (5)
$\overline{CE}_1$ (8)
$\overline{CE}_2$ (10)
1 OF 64 ROW DECODE
63
0
4096 BIT MEMORY ARRAY
64 TRANSMISSION GATES
1 OF 16 COLUMN DECODE
CHIP ENABLE LOGIC
OUTPUT BUFFERS
(14) O1
(13) O2
(12) O3
(11) O4

NOTE: Physical bit positions for columns are as follows:
$O_2, O_4 = (0 \longrightarrow 15)$
$O_1, O_3 = (15, 0 \longrightarrow 14)$

( ) = PIN NUMBERS
(18) = V_{CC}
(9) = GND

Logic Symbol



$\overline{CE}_1$
$\overline{CE}_2$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4

Specifications HM-7642A/43A

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642A/43A-5 V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642A/43A-2 V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

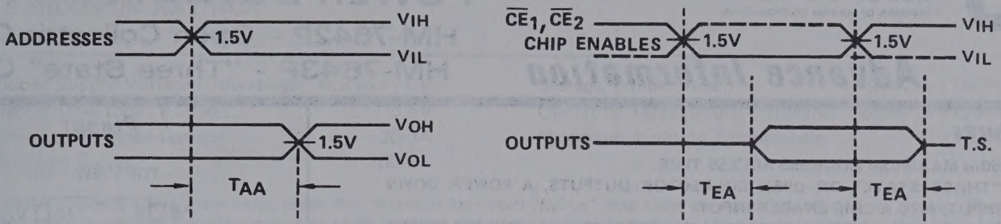
		HM-7642A/43A 5V ±5% 0°C to +75°C			HM-7642A/43A 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TAA	Address Access Time	–	35	50	–	–	70	ns
TEA	Chip Enable Access Time	–	15	25	–	–	30	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

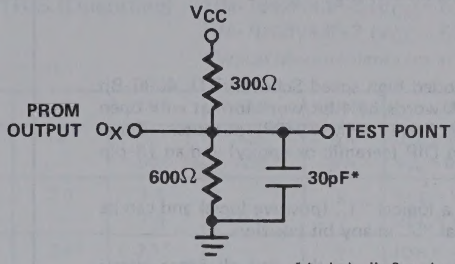
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed — but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE1, CE2
CHIP ENABLES
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

A.C. TEST LOAD


VCC
300Ω
PROM
OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes jig & probe
total capacitance

HARRIS
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PRODUCTS DIVISION
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HM-7642P/43P

POWER DOWN 1K x 4 PROM

HM-7642P - Open Collector Outputs
HM-7643P - "Three State" Outputs

Advance Information

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS, A POWER DOWN INPUT, AND A CHIP ENABLE INPUT.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642P/43P are fully decoded high speed SchottkyTTL 4096-Bit Field Programmable ROMs in a 1K words by 4 bit/word format with open collector (HM-7642P) or "Three State" (HM-7643P) outputs. These PROM s are available in an 18-pin DIP (ceramic or epoxy) and an 18-pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

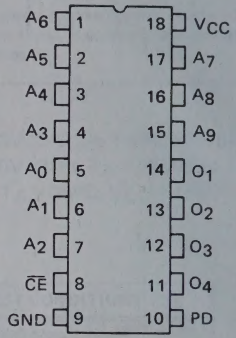
The HM-7642P/43P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a power down input on the HM-7642P/43P which is similar to a chip enable. The chip can be enabled or disabled using the power down input where a powered down chip dissipates 25% of nominal power and the outputs go to a high impedance state. The chip is powered up when PD_1 is low.

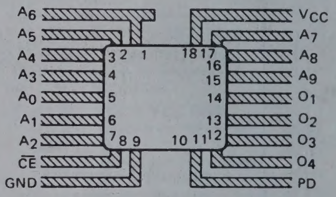
There is also the conventional chip enable input on this device, $\overline{CE}$ low and PD_1 low enables the device.

Pinout

TOP VIEW – DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
CE 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 O1
13 O2
12 O3
11 O4
10 PD

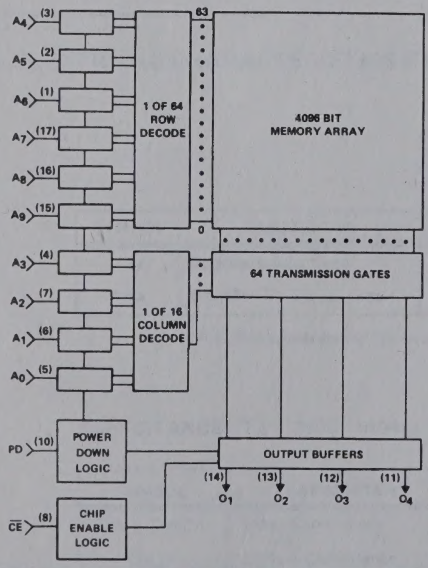
TOP VIEW – FLAT PACK


A6
A5
A4
A3
A0
A1
A2
CE
GND
VCC
A7
A8
A9
O1
O2
O3
O4
PD
3 2 1
18 17
16
15
4
5
14
6
13
7 8 9
10 11 12

PIN NAMES

A_0 - A_9	ADDRESS INPUTS
O_1 - O_4	DATA OUTPUTS
PD	POWER DOWN INPUT
$\overline{CE}$	CHIP ENABLE INPUT

Functional Diagram

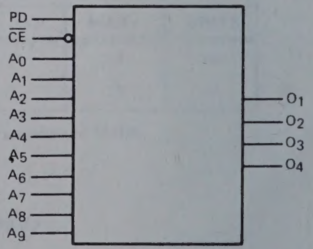

A4 (3)
A5 (2)
A6 (1)
A7 (17)
A8 (16)
A9 (15)
63
0
1 OF 64 ROW DECODE
4096 BIT MEMORY ARRAY
A3 (4)
A2 (7)
A1 (6)
A0 (5)
1 OF 16 COLUMN DECODE
64 TRANSMISSION GATES
PD (10)
POWER DOWN LOGIC
OUTPUT BUFFERS
(14) (13) (12) (11)
O1 O2 O3 O4
CE (8)
CHIP ENABLE LOGIC

NOTE: Physical bit positions for columns are as follows:

O_1, O_3 = (15, 0 $\longrightarrow$ 14)
O_2, O_4 = (0 $\longrightarrow$ 15)

( ) = Pin Numbers
(18) = V_{CC}
(9) = GND

Logic Symbol


PD
CE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4

Specifications HM-7642P/43P

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642P/43P-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642P/43P-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.
I_{CCPD}	Power Supply Current During Power Down	–	–	40	mA	V_{CC} = V_{CC} Max., All Inputs Ground Except Pin 10.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

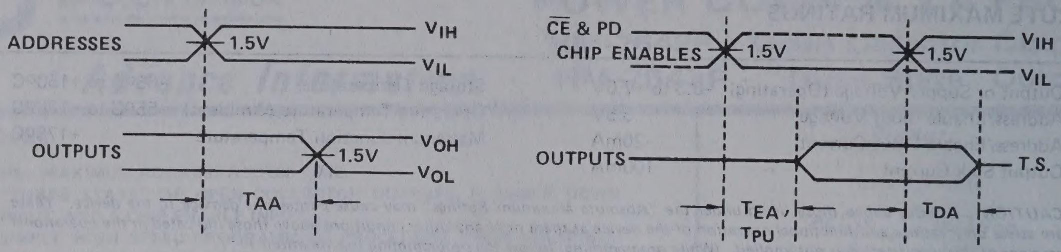
		HM-7642P/43P-5 5V ± 5% 0°C to +75°C			HM-7642P/43P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	35	50	-	-	70	ns
T_{DA}	Chip Disable Access Time	-	15	25	-	-	30	ns
T_{PU}	Chip Power-Up Access Time	-	100	150	-	-	200	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

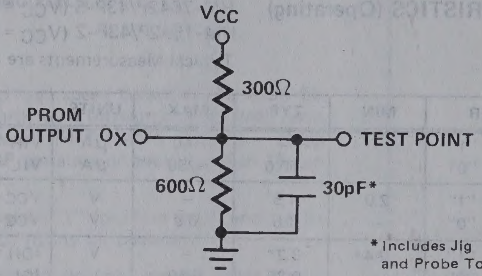
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
V_{IH}
V_{IL}
OUTPUTS
1.5V
V_{OH}
V_{OL}
T_{AA}
$\overline{CE}$ & PD
CHIP ENABLES
1.5V
1.5V
V_{IH}
V_{IL}
OUTPUTS
T.S.
T_{EA} /
T_{PU}
T_{DA}

A.C. TEST LOAD


V_{CC}
300Ω
PROM
OUTPUT O_X
TEST POINT
600Ω
30pF*

* Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7644

1K x 4 PROM

Active Pull-up Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- ACTIVE PULL-UP OUTPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME — GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW PIN COUNT FOR MAXIMUM DENSITY

Description

The HM-7644 is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 1K word by 4 bit/word format with active pull-up outputs. This PROM is available in a 16 pin DIP (ceramic or epoxy) and a 16 pin flatpack.

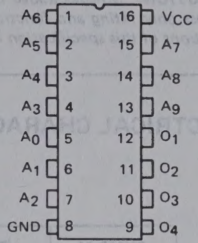
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

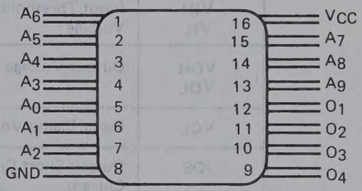
The HM-7644 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

Pinouts

TOP VIEW — DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 A8
13 A9
12 O1
11 O2
10 O3
9 O4

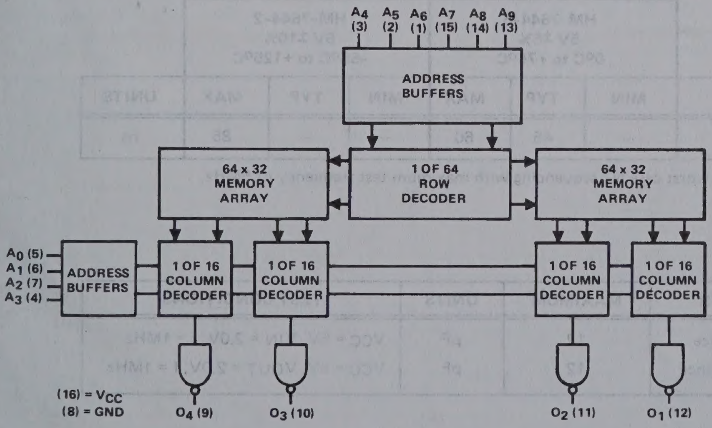
TOP VIEW — FLATPACK


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
GND 8
16 VCC
15 A7
14 A8
13 A9
12 O1
11 O2
10 O3
9 O4

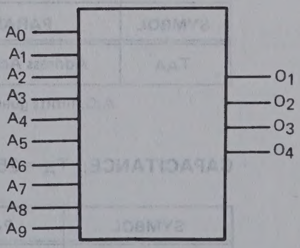
PIN NAMES

A0 – A9	Address Inputs
O1 – O4	Data Outputs

Functional Diagram


A4 (3)
A5 (2)
A6 (1)
A7 (15)
A8 (14)
A9 (13)
ADDRESS BUFFERS
64 x 32 MEMORY ARRAY
1 OF 64 ROW DECODER
64 x 32 MEMORY ARRAY
A0 (5)
A1 (6)
A2 (7)
A3 (4)
ADDRESS BUFFERS
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
1 OF 16 COLUMN DECODER
(16) = VCC
(8) = GND
O4 (9)
O3 (10)
O2 (11)
O1 (12)

Logic Symbol


A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7644-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7644-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	"0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals

A.C. ELECTRICAL CHARACTERISTICS (Operating)

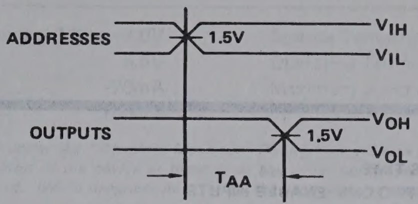
		HM-7644-5 5V ±5% 0°C to +75°C			HM-7644-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	85	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

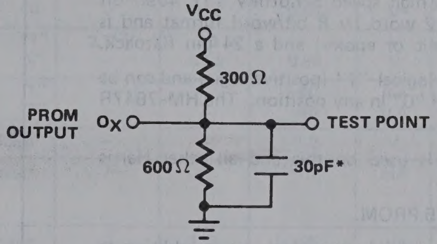
CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA

A. C. TEST LOAD


VCC
300Ω
PROM OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7647R
LATCHED OUTPUT
512 x 8 PROM

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 82S115
- LATCHED OUTPUTS
- INPUT LOADING IS – 100 μA MAXIMUM

Description

The HM-7647R is a fully decoded high speed Schottlky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any position. The HM-7647R has "Three State" outputs.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The pinout is identical to the 82S115 PROM.

The HM-7647R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

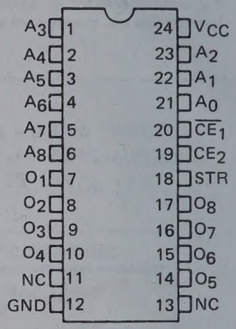
There are two chip enable inputs on the HM-7647R. $\overline{CE}_1$ low and CE_2 high enables the chip.

HM-7647R is operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the two chip enable inputs will control the outputs.

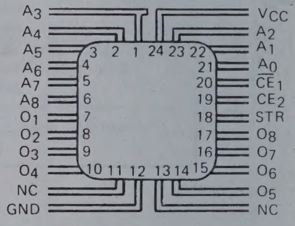
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes low the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinout

TOP VIEW – D.I.P.


A3 1
A4 2
A5 3
A6 4
A7 5
A8 6
O1 7
O2 8
O3 9
O4 10
NC 11
GND 12
24 VCC
23 A2
22 A1
21 A0
20 CE1
19 CE2
18 STR
17 O8
16 O7
15 O6
14 O5
13 NC

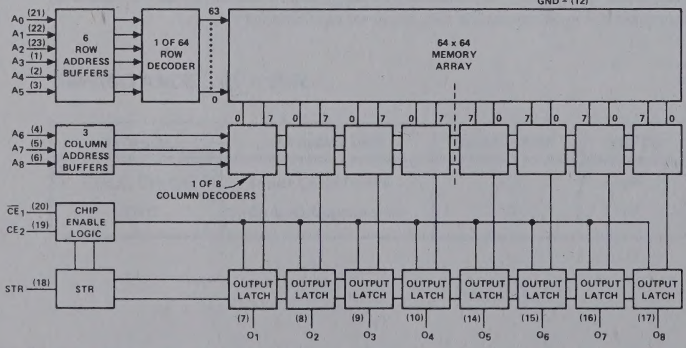
TOP VIEW – FLATPACK


A3
A4
A5
A6
A7
A8
O1
O2
O3
O4
NC
GND
VCC
A2
A1
A0
CE1
CE2
STR
O8
O7
O6
O5
NC
3 2 1 24 23 22
4 5 6 7 8 9
21 20 19 18 17 16
10 11 12 13 14 15

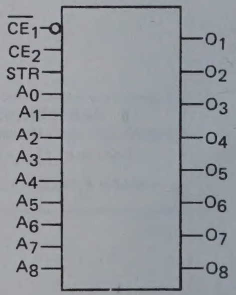
PIN NAMES

A0 – A8	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}$1 – CE2	Chip Enable Inputs
STR	Latch Input

Functional Diagram


VCC = (24)
GND = (12)
A0 (21)
A1 (22)
A2 (23)
A3 (1)
A4 (2)
A5 (3)
6 ROW ADDRESS BUFFERS
1 OF 64 ROW DECODER
63
0
64 x 64 MEMORY ARRAY
0 7
A6 (4)
A7 (5)
A8 (6)
3 COLUMN ADDRESS BUFFERS
1 OF 8 COLUMN DECODERS
CE1 (20)
CE2 (19)
CHIP ENABLE LOGIC
STR (18)
STR
OUTPUT LATCH
(7) O1
(8) O2
(9) O3
(10) O4
(14) O5
(15) O6
(16) O7
(17) O8

Logic Symbol


CE1
CE2
STR
A0
A1
A2
A3
A4
A5
A6
A7
A8
O1
O2
O3
O4
O5
O6
O7
O8

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7647R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7647R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125° C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50	+25 -100(1)	μA μA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0" "0"	2.0 –	1.5 1.5	– 0.85	V V	VCC = VCC Min. VCC = VCC Max.
VOH VOL	Output "1" "1" Voltage "0" "0"	2.7(2) –	3.3 0.35	– 0.50	V V	IOH = -2.0mA, V_{CC} = VCC Min. IOL = +16mA, V_{CC} = VCC Min.
IOHE IOLE	Output Disable "1" Current "0" "0"	– –	– –	+40 -40	μA μA	VOH, VCC = VCC Max. VOL = 0.3V, VCC = VCC Max.
VCL	Input Clamp Voltage	–	–	-1.2	V	IIN = -18mA
IOS	Output Short Circuit Current	-20	–	-70	mA	VOUT = 0.0V One Output Only for a Max. of 1 Second
ICC	Power Supply Current	–	135	185	mA	VCC = VCC Max. All Inputs Grounded

*Positive current defined as into device terminals.

NOTE(1): I_{IL} = -150 μA for -2

NOTE(2): V_{OH} = 2.4V for -2

A.C. ELECTRICAL CHARACTERISTICS (Operating)

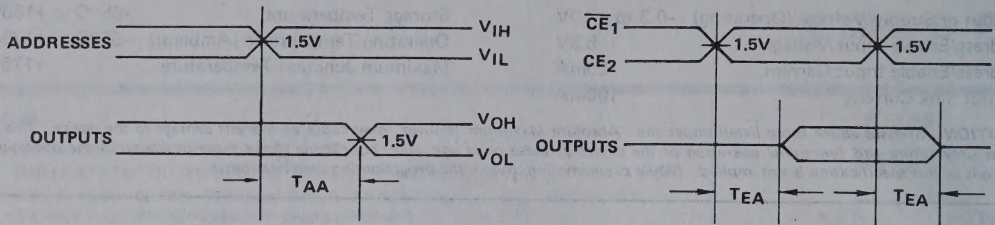
		HM-7647R-5 5V ± 5% 0°C to +75°C			HM-7647R-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
TAA TEA	Address Access Time Chip Enable Access Time	– –	40 30	60 40	– –	50 40	80 50	ns ns	Transparent
TADH	Address Hold Time	0	-10	–	0	-10	–	ns	Latched
TCDH	Chip Enable Hold Time	10	0	–	10	0	–	ns	
TSW	Strobe Pulse Width	30	15	–	40	15	–	ns	
TSL	Strobe Latch Time	60	35	–	80	45	–	ns	
TDL	Strobe Delatch Time	–	–	40	–	–	50	ns	
TCDS	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

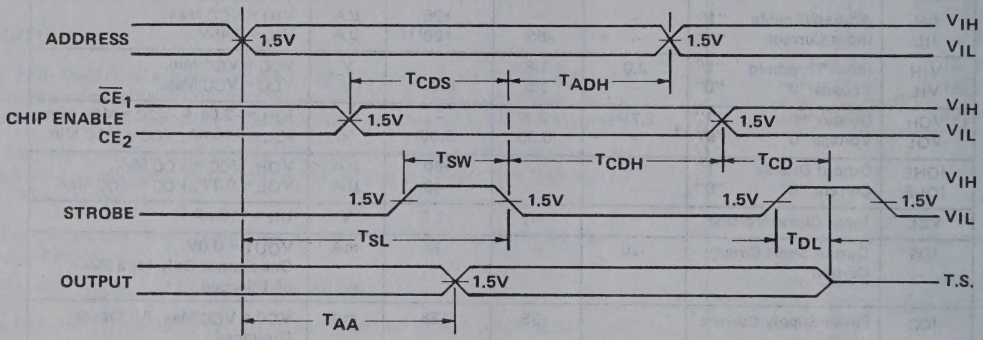
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	VCC = 5V, VIN = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	VCC = 5V, VOUT = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (TRANSPARENT MODE)

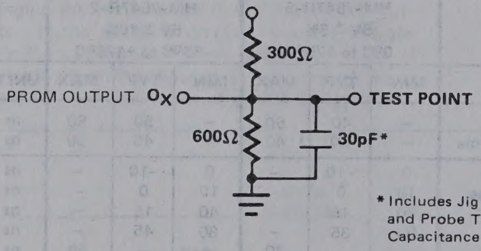

ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE1
CE2
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (LATCHED MODE)


ADDRESS
1.5V
1.5V
VIH
VIL
TCDS
TADH
CE1
CHIP ENABLE
CE2
1.5V
1.5V
VIH
VIL
TSW
TCDH
TCD
VIH
1.5V
1.5V
1.5V
1.5V
VIL
STROBE
TSL
TDL
OUTPUT
1.5V
T.S.
TAA

A.C. TEST LOAD


300Ω
PROM OUTPUT OX
TEST POINT
600Ω
30pF*
* Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7648/49

512 x 8 PROM

HM-7648 - Open Collector Outputs
HM-7649 - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 74S472/73
- LOW INPUT LOADING

Description

The HM-7648/49 is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format with open collector (HM-7648) or "Three State" (HM-7649) outputs. These PROMs are available in a 20 pin D.I.P. (ceramic or epoxy) and a 20 pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

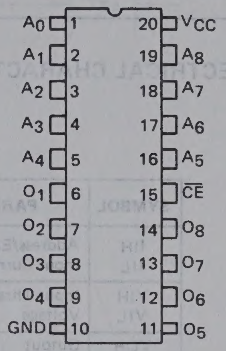
The pinout is identical to the 74S472/73 PROM.

The HM-7648/49 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametic and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

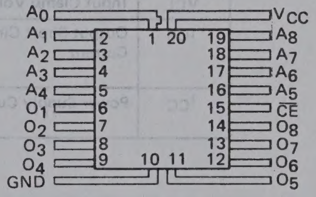
There is a chip enable input on the HM-7648/49 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW - D.I.P.


A_0 1
A_1 2
A_2 3
A_3 4
A_4 5
O_1 6
O_2 7
O_3 8
O_4 9
GND 10
20 V_{CC}
19 A_8
18 A_7
17 A_6
16 A_5
15 $\overline{CE}$
14 O_8
13 O_7
12 O_6
11 O_5

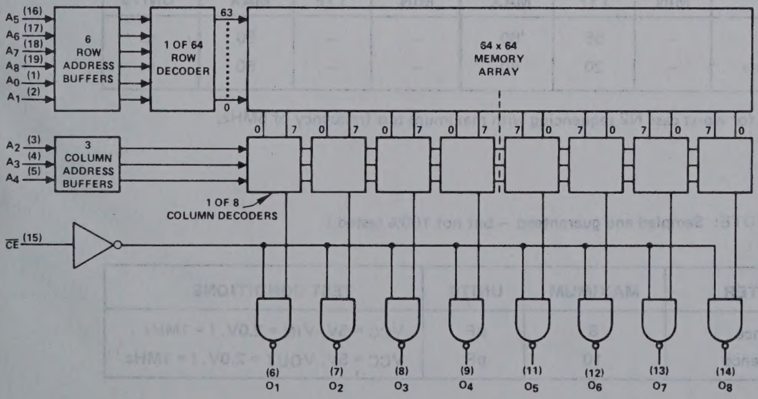
TOP VIEW - FLATPACK


A_0
A_1
A_2
A_3
A_4
O_1
O_2
O_3
O_4
GND
2
3
4
5
6
7
8
9
1 20
10 11
19
18
17
16
15
14
13
12
V_{CC}
A_8
A_7
A_6
A_5
$\overline{CE}$
O_8
O_7
O_6
O_5

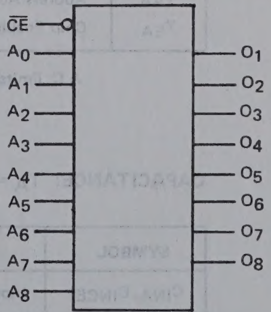
PIN NAMES

A_0 - A_8	Address Inputs
O_1 - O_8	Data Outputs
$\overline{CE}$	Chip Enable Input

Functional Diagram


A_5 (16)
A_6 (17)
A_7 (18)
A_8 (19)
A_0 (1)
A_1 (2)
6 ROW ADDRESS BUFFERS
1 OF 64 ROW DECODER
63
0
64 x 64 MEMORY ARRAY
0 7
A_2 (3)
A_3 (4)
A_4 (5)
3 COLUMN ADDRESS BUFFERS
1 OF 8 COLUMN DECODERS
$\overline{CE}$ (15)
(6) O_1
(7) O_2
(8) O_3
(9) O_4
(11) O_5
(12) O_6
(13) O_7
(14) O_8

Logic Symbol


$\overline{CE}$
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
O_1
O_2
O_3
O_4
O_5
O_6
O_7
O_8

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	$-65^{o}C$ to $+150^{o}C$
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	$-55^{o}C$ to $+125^{o}C$
Address/Enable Input Current	-20mA	Maximum Junction Temperature	$+175^{o}C$
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7648/49-5 ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{o}C$ to $+75^{o}C$)
HM-7648/49-2 ($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^{o}C$ to $+125^{o}C$)
Typical measurements are at $T_A = 25^{o}C$, $V_{CC} = +5V$

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable Input Current	"1" "0"	– –	– -50	+25 -250	µA µA	$V_{IH} = V_{CC}$ Max. $V_{IL} = 0.45V$
V_{IH} V_{IL}	Input Threshold Voltage	"1" "0"	2.0 –	1.5 1.5	– 0.80	V V	$V_{CC} = V_{CC}$ Min. $V_{CC} = V_{CC}$ Max.
V_{OH} V_{OL}	Output Voltage	"1" "0"	2.4 * –	3.2* 0.35	– 0.50	V V	$I_{OH} = -2.0mA$, $V_{CC} = V_{CC}$ Min. $I_{OL} = +16mA$, $V_{CC} = V_{CC}$ Min.
I_{OHE} I_{OLE}	Output Disable Current	"1" "0"	– –	– –	+50 -50 *	µA µA	V_{OH}, $V_{CC} = V_{CC}$ Max. $V_{OL} = 0.3V$, $V_{CC} = V_{CC}$ Max.
V_{CL}	Input Clamp Voltage		–	–	-1.2	V	$I_{IN} = -18mA$
I_{OS}	Output Short Circuit Current		-20*	–	-100*	mA	$V_{OUT} = 0.0V$ One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current		–	120	170	mA	$V_{CC} = V_{CC}$ Max. All Inputs Grounded

* "Three State" only

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

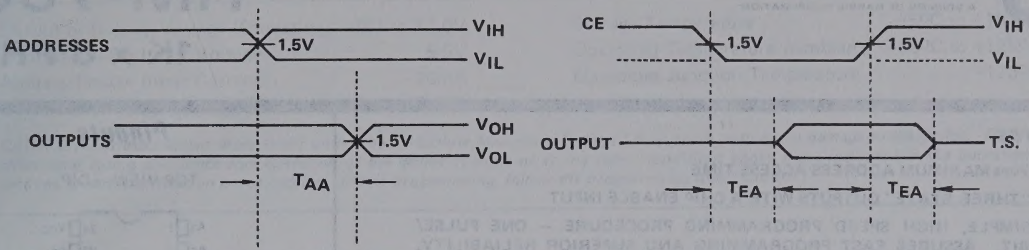
		HM-7648/49-5 5V ±5% $0^{o}C$ to $+ 75^{o}C$			HM-7648/49-2 5V ±10% $-55^{o}C$ to $+125^{o}C$			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	55	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	20	40	–	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

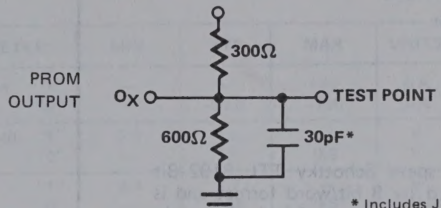
CAPACITANCE: $T_A = 25^{o}C$ (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	$V_{CC} = 5V$, $V_{IN} = 2.0V$, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	$V_{CC} = 5V$, $V_{OUT} = 2.0V$, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
V_{IH}
V_{IL}
OUTPUTS
1.5V
V_{OH}
V_{OL}
T_{AA}
CE
1.5V
1.5V
V_{IH}
V_{IL}
OUTPUT
T.S.
T_{EA}
T_{EA}

A.C. TEST LOAD


300Ω
PROM OUTPUT
O_X
TEST POINT
600Ω
30pF*

* Includes Jig and Probe Total Capacitance

HM-7608

1K x 8 PROM

Features

- **70ns MAXIMUM ADDRESS ACCESS TIME**
- **"THREE STATE" OUTPUTS WITH A CHIP ENABLE INPUT**
- **SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.**
- **FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.**
- **INDUSTRY'S HIGHEST PROGRAMMING YIELD**
- **PIN COMPATIBLE WITH THE 2708 WITH:**
  - **ONLY ONE 5 VOLT SUPPLY**
  - **SUPERIOR ACCESS TIME**
  - **FASTER PROGRAMMING TIME**

Description

The HM-7608 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position, the HM-7608 has "Three State" outputs.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

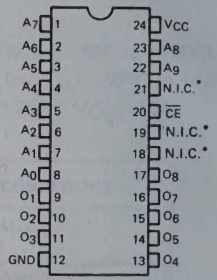
The HM-7608 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is a plug in replacement for the 2708 where the V_{SS} pin on the 2708 becomes GND on the HM-7608. The V_{BB}, V_{DD}, and program pins on the 2708 are all N.C. on the HM-7608.

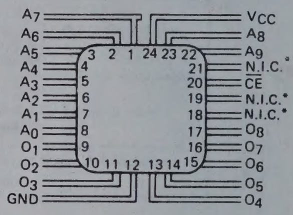
There is a chip enable input on the HM-7608 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW – DIP


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 N.I.C.*
20 CE
19 N.I.C.*
18 N.I.C.*
17 O8
16 O7
15 O6
14 O5
13 O4

TOP VIEW – FLATPACK

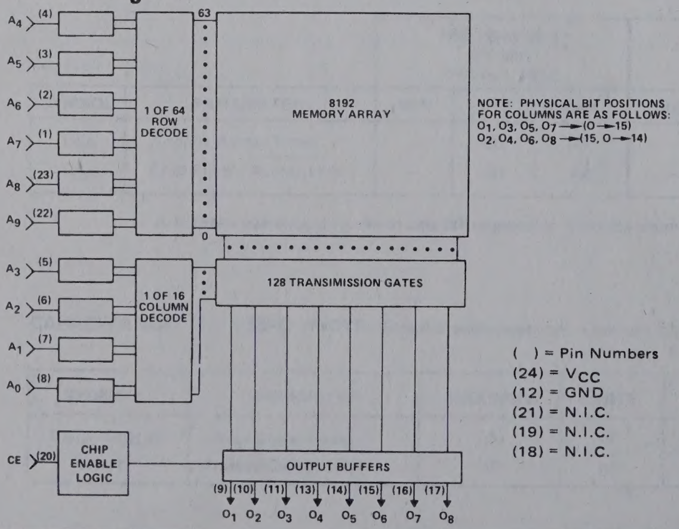

A7
A6
A5
A4
A3
A2
A1
A0
O1
O2
O3
GND
VCC
A8
A9
N.I.C.*
CE
N.I.C.*
N.I.C.*
O8
O7
O6
O5
O4
3 2 1 24 23 22
4 5 6 7 8 9
21 20 19 18 17 16
10 11 12 13 14 15

PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

*No Internal Connect

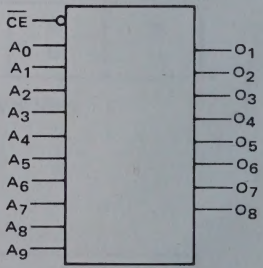
Functional Diagram


A4 (4)
A5 (3)
A6 (2)
A7 (1)
A8 (23)
A9 (22)
63
0
1 OF 64 ROW DECODE
8192 MEMORY ARRAY
A3 (5)
A2 (6)
A1 (7)
A0 (8)
1 OF 16 COLUMN DECODE
128 TRANSIMISSION GATES
CE (20)
CHIP ENABLE LOGIC
OUTPUT BUFFERS
(9) (10) (11) (13) (14) (15) (16) (17)
O1 O2 O3 O4 O5 O6 O7 O8

NOTE: PHYSICAL BIT POSITIONS FOR COLUMNS ARE AS FOLLOWS:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND
(21) = N.I.C.
(19) = N.I.C.
(18) = N.I.C.

Logic Symbol


CE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4
O5
O6
O7
O8

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7608-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7608-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– -50.0	+40 -100	μA μA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	VCC = VCC Min. VCC = VCC Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.5	V V	I_{OH} = -2.0mA, VCC = VCC Min. I_{OL} = +16mA, VCC = VCC Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	μA μA	V_{OH}, VCC = VCC Max. V_{OL} = 0.3V, VCC = VCC Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	-25	-100	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	VCC = VCC Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

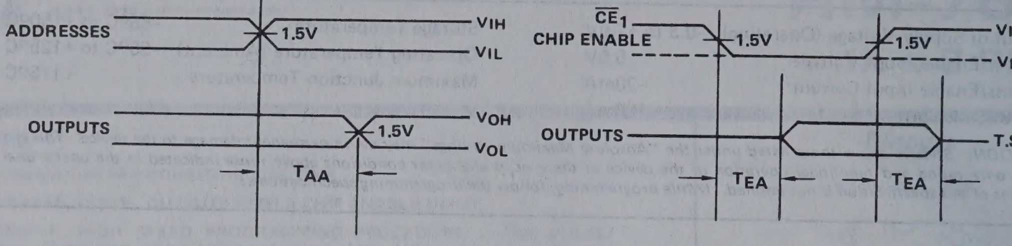
		HM-7608-5 5V ±5% 0°C to + 75°C			HM-7608-2 5V ±10% -55°C to +125°C			
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
T_{AA}	Address Access Time	–	45	70	–	–	90	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

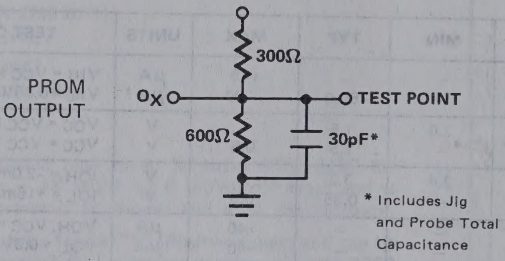
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	VCC = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	VCC = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
$\overline{CE}_1$
CHIP ENABLE
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

A.C. TEST LOAD


300Ω
PROM
OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680/81
1K x 8 PROM
HM-7680 - Open Collector Outputs
HM-7681 - "Three State" Outputs

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7680/81 is a fully decoded high speed Schottky TTL 8192/Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680) or "Three State" (HM-7681) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

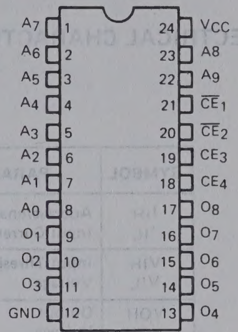
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7680/81 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

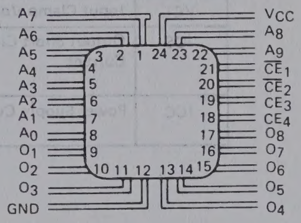
There are four chip enable inputs on the HM-7680/81. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Pinouts

TOP VIEW—DIP


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 CE1
20 CE2
19 CE3
18 CE4
17 O8
16 O7
15 O6
14 O5
13 O4

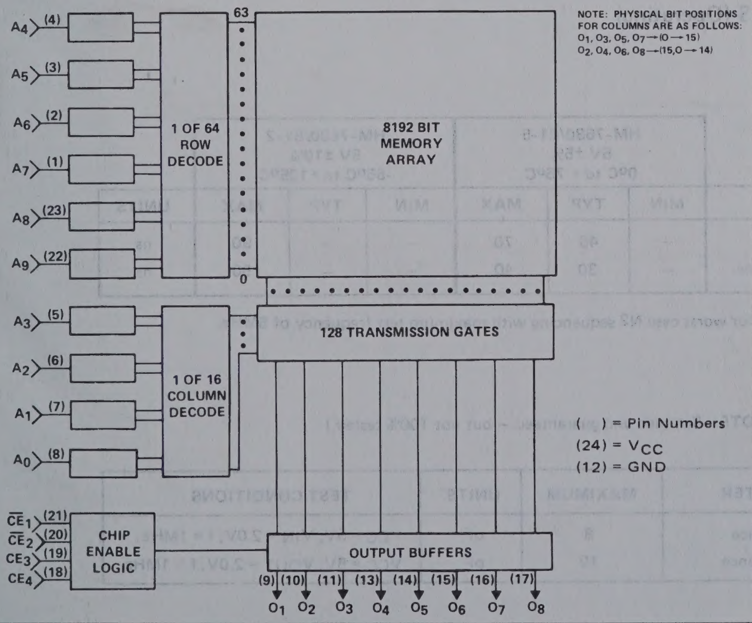
TOP VIEW – FLATPACK


A7
A6
A5
A4
A3
A2
A1
A0
O1
O2
O3
GND
VCC
A8
A9
CE1
CE2
CE3
CE4
O8
O7
O6
O5
O4
3 2 1 24 23 22
4 5 6 7 8 9
21 20 19 18 17 16
10 11 12 13 14 15

PIN NAMES

A0 – A9	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Inputs

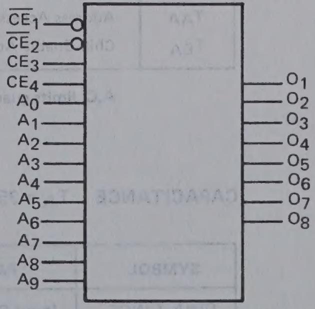
Functional Diagram


A4 (4)
A5 (3)
A6 (2)
A7 (1)
A8 (23)
A9 (22)
1 OF 64 ROW DECODE
63
0
8192 BIT MEMORY ARRAY
128 TRANSMISSION GATES
A3 (5)
A2 (6)
A1 (7)
A0 (8)
1 OF 16 COLUMN DECODE
CE1 (21)
CE2 (20)
CE3 (19)
CE4 (18)
CHIP ENABLE LOGIC
OUTPUT BUFFERS
(9) (10) (11) (13) (14) (15) (16) (17)
O1 O2 O3 O4 O5 O6 O7 O8

NOTE: PHYSICAL BIT POSITIONS FOR COLUMNS ARE AS FOLLOWS:
O1, O3, O5, O7 → (0 → 15)
O2, O4, O6, O8 → (15,0 → 14)

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Logic Symbol


CE1
CE2
CE3
CE4
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4
O5
O6
O7
O8

Specifications HM-7680/81

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65^oC to $+150^oC$
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55^oC to $+125^oC$
Address/Enable Input Current	-20mA	Maximum Junction Temperature	$+175^oC$
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680/81-5 (V_{CC} = 5.0V ±5%, T_A = 0^oC to $+75^oC$)
HM-7680/81-2 (V_{CC} = 5.0V ±10%, T_A = -55^oC to $+125^oC$)
Typical measurements are at T_A = 25^oC, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 * –	3.2 * 0.35	 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40 *	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

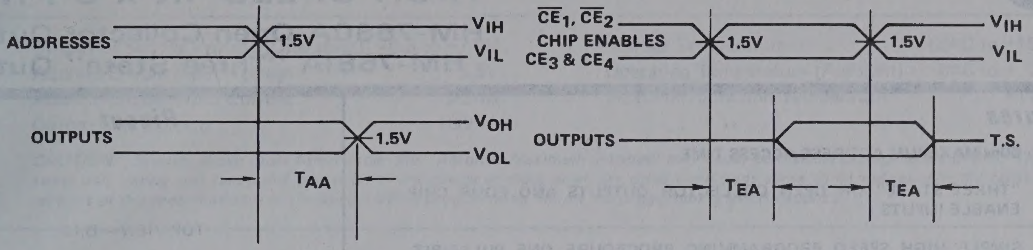
		HM-7680/81-5 5V ±5% 0^oC to + 75^oC			HM-7680/81-2 5V ±10% -55^oC to $+125^oC$			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	70	–	–	90	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

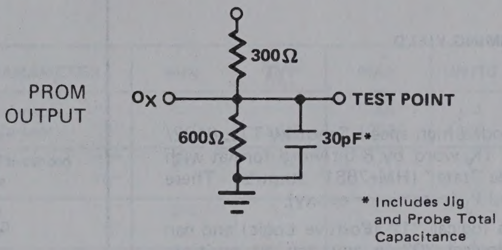
CAPACITANCE : T_A = 25^oC (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
V_{IH}
V_{IL}
OUTPUTS
1.5V
V_{OH}
V_{OL}
T_{AA}
$\overline{CE}_1, \overline{CE}_2$
CHIP ENABLES
CE_3 & CE_4
1.5V
1.5V
V_{IH}
V_{IL}
OUTPUTS
T.S.
T_{EA}
T_{EA}

A.C. TEST LOAD


300Ω
PROM OUTPUT
O_X
TEST POINT
600Ω
30pF*

* Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680A/81A

HIGH SPEED 1K x 8 PROM

HM-7680A Open Collector Outputs
HM-7681A "Three State" Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- ULTRA FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7680A/81A is a fully decoded high speed Schottky TTL 8192/Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680) or "Three State" (HM-7681) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

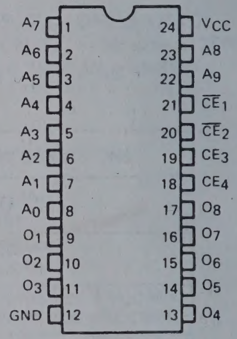
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7680A/81A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7680A/81A. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Pinout

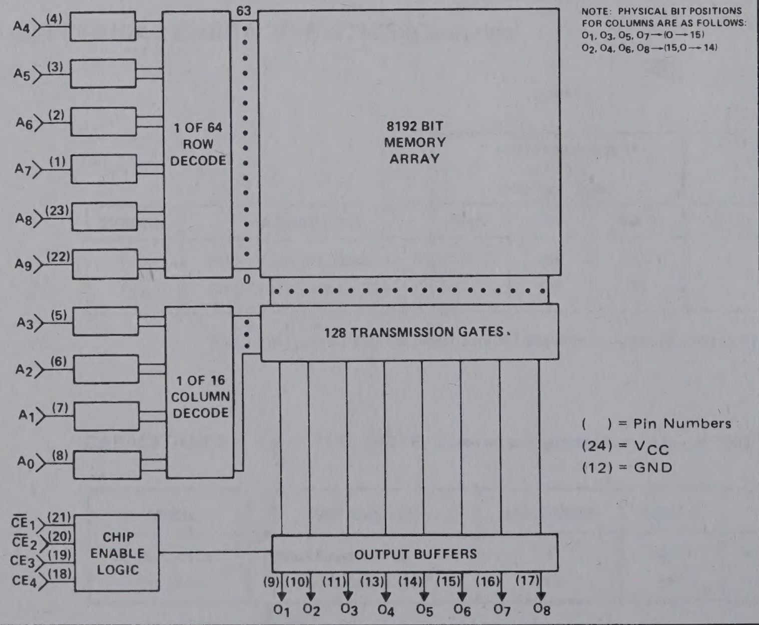
TOP VIEW – D.I.P.


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 $\overline{CE}_1$
20 $\overline{CE}_2$
19 CE3
18 CE4
17 O8
16 O7
15 O6
14 O5
13 O4

PIN NAMES

A0 – A9	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Inputs

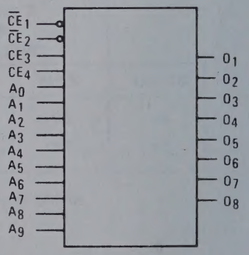
Functional Diagram


A4 (4)
A5 (3)
A6 (2)
A7 (1)
A8 (23)
A9 (22)
63
0
1 OF 64 ROW DECODE
8192 BIT MEMORY ARRAY
A3 (5)
A2 (6)
A1 (7)
A0 (8)
1 OF 16 COLUMN DECODE
128 TRANSMISSION GATES
$\overline{CE}_1$ (21)
$\overline{CE}_2$ (20)
CE3 (19)
CE4 (18)
CHIP ENABLE LOGIC
OUTPUT BUFFERS
(9) (10) (11) (13) (14) (15) (16) (17)
O1 O2 O3 O4 O5 O6 O7 O8

NOTE: PHYSICAL BIT POSITIONS FOR COLUMNS ARE AS FOLLOWS:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Logic Symbol


$\overline{CE}_1$
$\overline{CE}_2$
CE3
CE4
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4
O5
O6
O7
O8

Specifications HM-7680A/81A

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	0°C to + 75°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680A/81A-5 (V_{CC} = 5.0V ±5%, T_A = 0° to +75°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

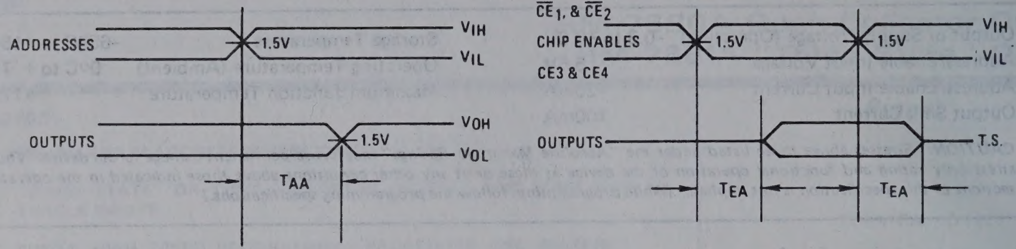
		HM-7680A/81A 5V ±5% 0°C to +75°C			
SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM*	UNITS
T_{AA}	Address Access Time	–	40	50	ns
T_{EA}	Chip Enable Access Time	–	30	40	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

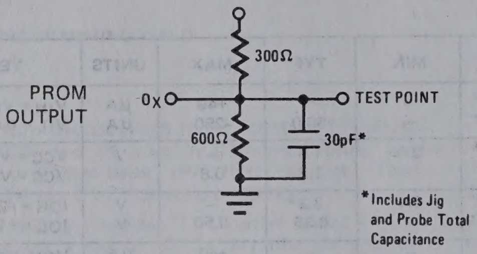
CAPACITANCE : T_A = 25°C (NOTE: Sampled and guaranteed — but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
V_{IH}
V_{IL}
OUTPUTS
1.5V
V_{OH}
V_{OL}
T_{AA}
$\overline{CE}_1$, & $\overline{CE}_2$
CHIP ENABLES
CE3 & CE4
1.5V
1.5V
V_{IH}
V_{IL}
OUTPUTS
T.S.
T_{EA}
T_{EA}

A.C. TEST LOAD


300Ω
PROM
OUTPUT
0_X
TEST POINT
600Ω
30pF*
*Includes Jig and Probe Total Capacitance

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A DIVISION OF HARRIS CORPORATION

HM-7680R/81R
LATCHED OUTPUT 1K x 8 PROM
HM-7680R - Open Collector Outputs
HM-7681R - "Three State" Outputs

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURES AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS

Description

The HM-7680R/81R is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680R) or "Three State" (HM-7681R) outputs. These PROMs are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7680R/81R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

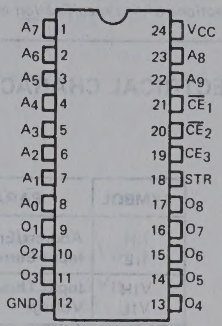
There are three chip enable inputs on the HM-7680R/81R. $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

The HM-7680R/81R is operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

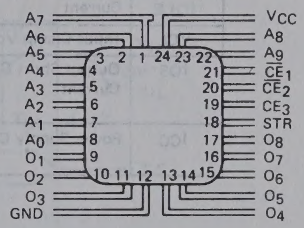
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW—DIP


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 $\overline{CE}_1$
20 $\overline{CE}_2$
19 CE3
18 STR
17 O8
16 O7
15 O6
14 O5
13 O4

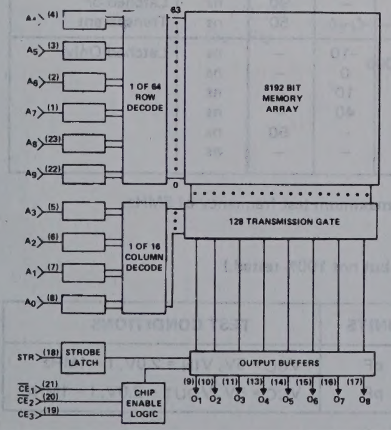
TOP VIEW — FLATPACK


A7
A6
A5
A4
A3
A2
A1
A0
O1
O2
O3
GND
VCC
A8
A9
$\overline{CE}_1$
$\overline{CE}_2$
CE3
STR
O8
O7
O6
O5
O4
3 2 1 24 23 22
4
5
6
7
8
9
10 11 12 13 14 15
21
20
19
18
17
16

PIN NAMES

A0 – A9	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE3	Chip Enable Inputs
STR	Strobe

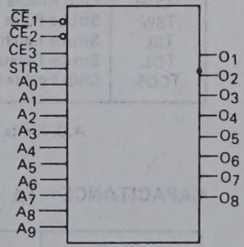
Functional Diagram


A4 (4)
A5 (3)
A6 (2)
A7 (1)
A8 (23)
A9 (22)
1 OF 64 ROW DECODE
63
0
8192 BIT MEMORY ARRAY
A3 (5)
A2 (6)
A1 (7)
A0 (8)
1 OF 16 COLUMN DECODE
128 TRANSMISSION GATE
STR (18)
STROBE LATCH
$\overline{CE}_1$ (21)
$\overline{CE}_2$ (20)
CE3 (19)
CHIP ENABLE LOGIC
OUTPUT BUFFERS
(9) (10) (11) (13) (14) (15) (16) (17)
O1 O2 O3 O4 O5 O6 O7 O8

NOTE: Physical bit positions for columns are as follows:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Logic Symbol


$\overline{CE}_1$
$\overline{CE}_2$
CE3
STR
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4
O5
O6
O7
O8

Specifications HM-7680R/81R

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680R/81R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680R/81R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-25	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

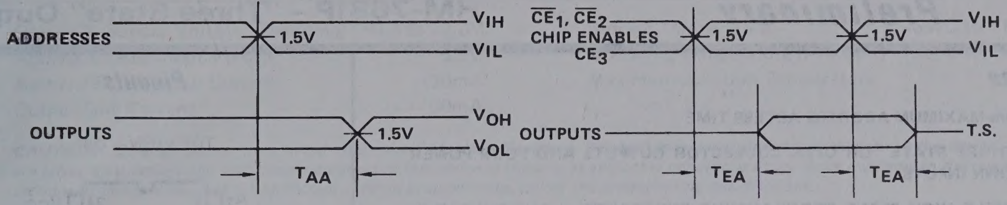
		HM-7680R/81R-5 5V ±5% 0°C to +75°C			HM-7680R/81R-2 5V ±10% -55°C to +125°C				
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDIT.**
T_{AA}	Address Access Time	–	45	70	–	–	90	ns	Latched or Transparent
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	70	40	–	90	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE : T_A = 25°C (NOTE: Sampled and guaranteed — but not 100% tested.)

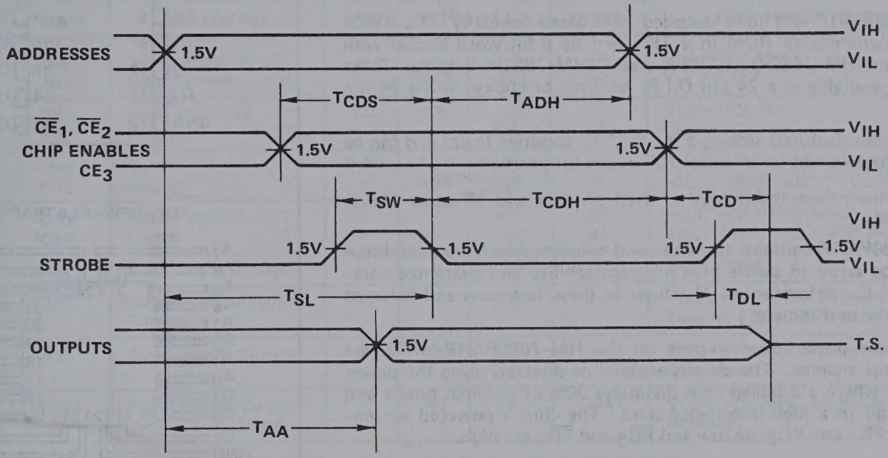
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

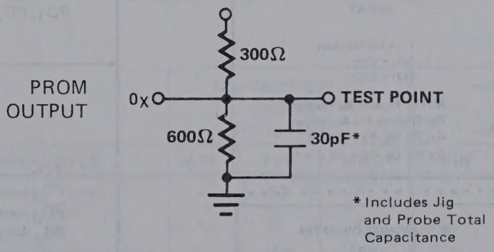

ADDRESSES
1.5V
V_{IH}
V_{IL}
OUTPUTS
1.5V
V_{OH}
V_{OL}
T_{AA}
$\overline{CE}_1$, $\overline{CE}_2$ CHIP ENABLES CE_3
1.5V
1.5V
V_{IH}
V_{IL}
OUTPUTS
T.S.
T_{EA}
T_{EA}

NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)


ADDRESSES
1.5V
1.5V
V_{IH}
V_{IL}
T_{CDS}
T_{ADH}
$\overline{CE}_1$, $\overline{CE}_2$ CHIP ENABLES CE_3
1.5V
1.5V
V_{IH}
V_{IL}
T_{SW}
T_{CDH}
T_{CD}
V_{IH}
STROBE
1.5V
1.5V
1.5V
1.5V
V_{IL}
T_{SL}
T_{DL}
OUTPUTS
1.5V
T.S.
T_{AA}

A.C. TEST LOAD


300Ω
PROM OUTPUT
0x
TEST POINT
600Ω
30pF*
* Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680P/81P

POWER DOWN 1K x 8 PROM

HM-7680P - Open Collector Outputs
HM-7681P - "Three State" Outputs

Preliminary

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR POWER DOWN INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7680P/81P is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680P) or "three state" (HM-7681P) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

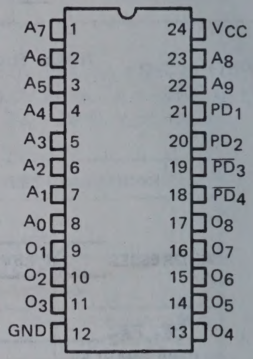
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7680P/81P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

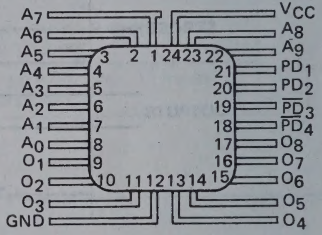
There are four power down inputs on the HM-7680P/81P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1 and PD_2 are low and $\overline{PD}_3$ and $\overline{PD}_4$ are high.

Pinouts

TOP VIEW – DIP


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 PD1
20 PD2
19 $\overline{PD}_3$
18 $\overline{PD}_4$
17 O8
16 O7
15 O6
14 O5
13 O4

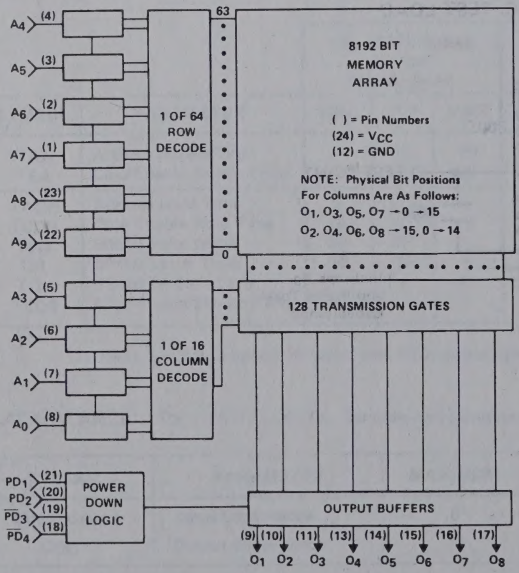
TOP VIEW–FLATPACK


A7
A6
A5
A4
A3
A2
A1
A0
O1
O2
O3
GND
VCC
A8
A9
PD1
PD2
$\overline{PD}_3$
$\overline{PD}_4$
O8
O7
O6
O5
O4
3 2 1 24 23 22
4 5 6 7 8 9
21 20 19 18 17 16 15
10 11 12 13 14

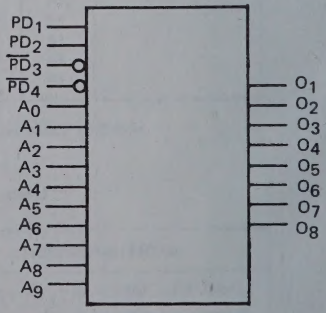
PIN NAMES

A_0 - A_9	Address Inputs
O_1 - O_8	Address Outputs
PD_1, PD_2, $\overline{PD}_3$, $\overline{PD}_4$	Power Down Inputs

Functional Diagram


A4 (4)
A5 (3)
A6 (2)
A7 (1)
A8 (23)
A9 (22)
A3 (5)
A2 (6)
A1 (7)
A0 (8)
1 OF 64 ROW DECODE
63
0
8192 BIT MEMORY ARRAY
( ) = Pin Numbers
(24) = VCC
(12) = GND
NOTE: Physical Bit Positions For Columns Are As Follows:
O1, O3, O5, O7 → 0 → 15
O2, O4, O6, O8 → 15, 0 → 14
128 TRANSMISSION GATES
1 OF 16 COLUMN DECODE
PD1 (21)
PD2 (20)
$\overline{PD}_3$ (19)
$\overline{PD}_4$ (18)
POWER DOWN LOGIC
OUTPUT BUFFERS
(9) (10) (11) (13) (14) (15) (16) (17)
O1 O2 O3 O4 O5 O6 O7 O8

Logic Symbol


PD1
PD2
$\overline{PD}_3$
$\overline{PD}_4$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
O1
O2
O3
O4
O5
O6
O7
O8

Specifications 7680P/81P

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680P/81P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7680P/81P-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*		-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.
I_{CCPD}	Power Supply Current During Power Down	–	40	55	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

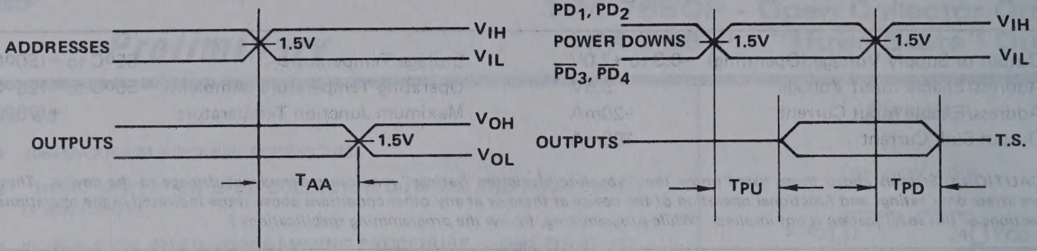
		HM-7680P/81P-5 5V ± 5% 0°C to +75°C			HM-7680P/81P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	50	70	-	-	90	ns
T_{PD}	Chip Power-Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	100	150	-	-	200	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

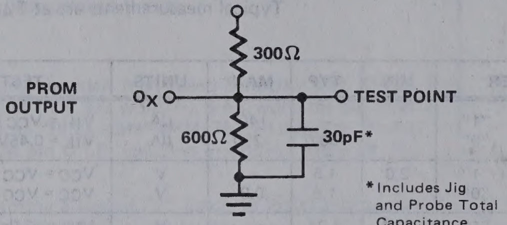
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
V_{IH}
V_{IL}
OUTPUTS
1.5V
V_{OH}
V_{OL}
T_{AA}
PD_1, PD_2
POWER DOWNS
$\overline{PD_3, PD_4}$
1.5V
1.5V
V_{IH}
V_{IL}
OUTPUTS
T.S.
T_{PU}
T_{PD}

A.C. TEST LOAD


300Ω
PROM OUTPUT
O_X
TEST POINT
600Ω
30pF*

*Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680RP/81RP
POWER DOWN 1K x 8 PROM

HM-7680RP - Open Collector Outputs
HM-7681RP - "Three State" Outputs

Preliminary

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- A POWER DOWN INPUT ALLOWING 70% REDUCTION IN NOMINAL POWER DISSIPATION.

Description

The HM-7680RP/81RP are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 1K words by 8 bit/word format with open collector (HM-7680RP) or "Three State" (HM-7681RP) outputs. These PROMs are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7680RP/81RP contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7680RP/81RP. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the device.

There is also a power down input on this device. A powered down device has 70% reduction in nominal power dissipation if the outputs are not latched and 50% reduction in nominal power if the outputs are latched.

The HM-7680RP/81RP is operated in the Transparent Read Mode by holding the the strobe input high and the $\overline{PD}$ input high throughout the read operation. This is the normal read mode where the two chip enables and the power down inputs will control the outputs.

In Latched Read Mode, bringing the strobe input low will latch the outputs and the chip enable inputs. However, the power down input is independent of the latch function and can be changed while in the latched mode. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode, the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

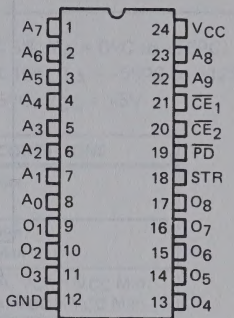
The following is a summary of the functional dependencies of the operating modes:

1. Chip enabled, transparent, powered up - normal mode where the power down input is effectively a chip enable with the I_{CC} reduction function.
2. Chip enabled, latched, power up - this is normal latched mode where the outputs remain latched regardless of address and chip enable switching.
3. Chip enabled, latched, power down - this is the powered down latched mode where the output data remains latched while power is reduced to 50% of its nominal value. If the latch strobe changes state while in this mode, the outputs will go to a high impedance state and power will reduce to 30% of nominal power. This is because the $\overline{PD}$ input becomes an effective chip enable in the Transparent Mode.
4. Chip disabled, transparent, power down - this is the normal powered down mode where the outputs are in a high impedance state and the power is reduced to 30% of the nominal power.

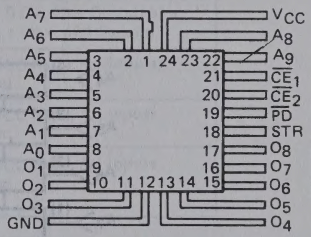
On the following page is a table to clarify the operational interdependencies.

Pinouts

TOP VIEW—DIP



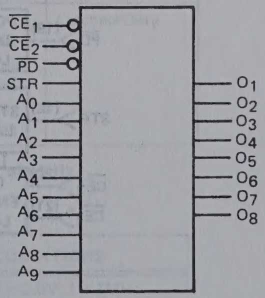
TOP VIEW—FLATPACK



PIN NAMES

A0-A9	Address Inputs
O1-O8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$\overline{PD}$	Power Down Input
STR	Strobe Input

Logic Symbol

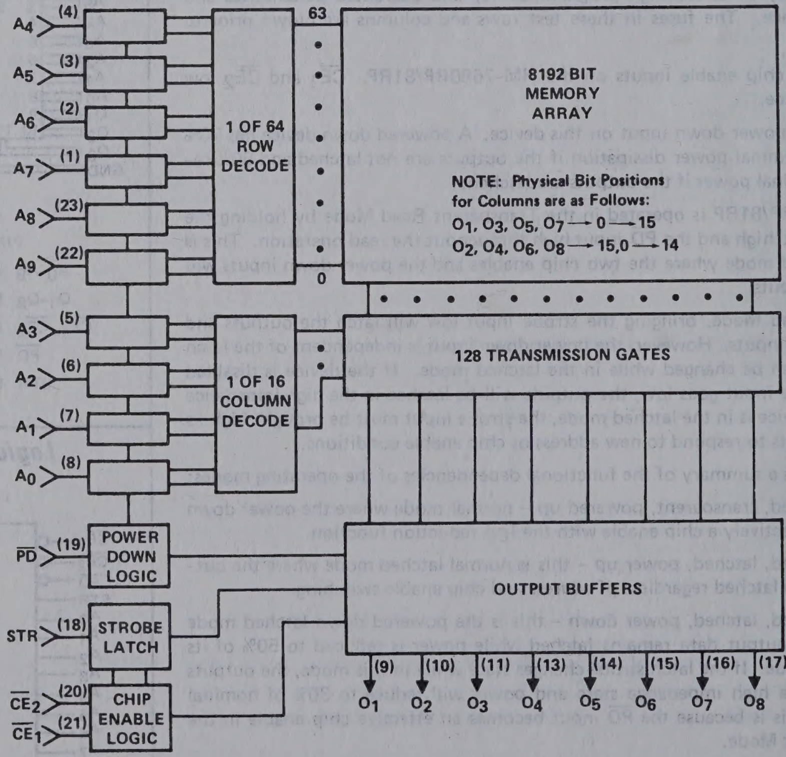


TRUTH TABLE for HM-7680RP/81RP

$\overline{PD}$	STR	$\overline{CE}_2$	$\overline{CE}_1$	OUTPUTS	ICC
0	0	0	0	Latched Data	85mA
0	0	0	1	Latched "Three State"	85mA
0	0	1	0	Latched "Three State"	85mA
0	0	1	1	Latched "Three State"	85mA
0	1	0	0	Unlatched "Three State"	60mA
0	1	0	1	Unlatched "Three State"	60mA
0	1	1	0	Unlatched "Three State"	60mA
0	1	1	1	Unlatched "Three State"	60mA
1	0	0	0	Latched Data	170mA
1	0	0	1	Latched "Three State"	170mA
1	0	1	0	Latched "Three State"	170mA
1	0	1	1	Latched "Three State"	170mA
1	1	0	0	Unlatched Data	170mA
1	1	0	1	Unlatched "Three State"	170mA
1	1	1	0	Unlatched "Three State"	170mA
1	1	1	1	Unlatched "Three State"	170mA

Assume that the sequence of transitions is: 1) Chip Enables, 2) STR, 3) $\overline{PD}$ and the initial state is Unlatched Data.

Functional Diagram


A4 (4)
A5 (3)
A6 (2)
A7 (1)
A8 (23)
A9 (22)
A3 (5)
A2 (6)
A1 (7)
A0 (8)
PD (19)
STR (18)
CE2 (20)
CE1 (21)
1 OF 64 ROW DECODE
63
0
8192 BIT MEMORY ARRAY
NOTE: Physical Bit Positions for Columns are as Follows:
O1, O3, O5, O7 → 0 → 15
O2, O4, O6, O8 → 15,0 → 14
128 TRANSMISSION GATES
1 OF 16 COLUMN DECODE
POWER DOWN LOGIC
STROBE LATCH
CHIP ENABLE LOGIC
OUTPUT BUFFERS
(9) O1
(10) O2
(11) O3
(13) O4
(14) O5
(15) O6
(16) O7
(17) O8

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680RP/81RP-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7680RP/81RP-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable Input Current "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Address/Enable Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold Voltage "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Input Threshold Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Output Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable Current "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max,
I_{OLE}	Output Disable Current "0"	–	–	-40*	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.
I_{CCPD}	Power Supply Current During Power Down	–	50	60	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.
I_{CCLPD}	Power Supply Current During Latched Power Down	–	70	85	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

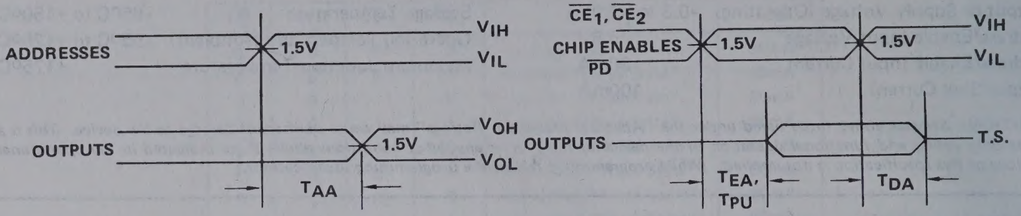
		HM-7680RP/81RP-5 5V ± 5% 0°C to +75°C			HM-7680RP/81RP-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST COND.
T_{AA}	Address Access Time	-	50	70	-	-	90	ns	Latched or Transparent
T_{DA}	Chip Disable Access Time	-	30	40	-	-	50	ns	
T_{EA}	Chip Enable Access Time	-	30	40	-	-	50	ns	
T_{PU}	Chip Power-Up Access Time	-	100	150	-	-	200	ns	
T_{ADH}	Address Hold Time	0	-10	-	0	-10	-	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	-	10	0	-	ns	
T_{SW}	Strobe Pulse Width	30	10	-	40	10	-	ns	
T_{SL}	Strobe Latch Time	70	40	-	90	40	-	ns	
T_{DL}	Strobe Delatch Time	-	-	40	-	-	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	-	-	50	-	-	ns	

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed — but not 100% tested.)

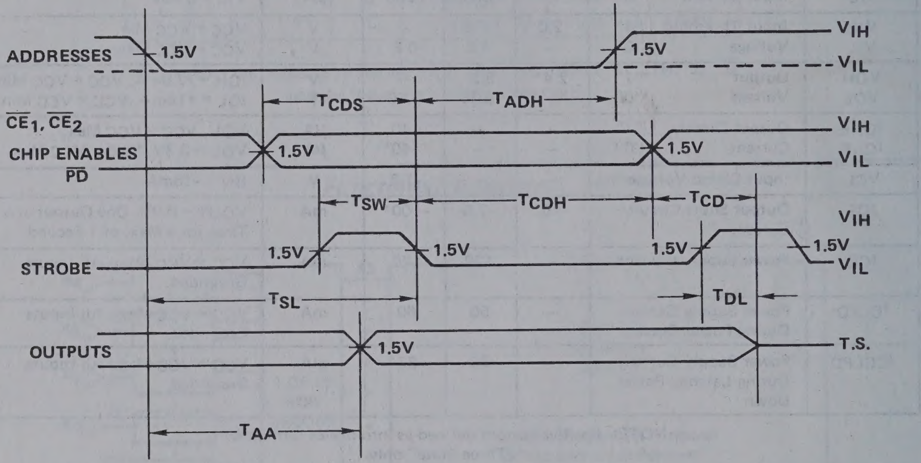
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)

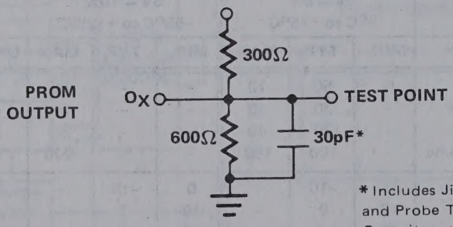

ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE1, CE2
CHIP ENABLES
PD
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA, TPU
TDA

NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)


ADDRESSES
1.5V
1.5V
VIH
VIL
TCDS
TADH
CE1, CE2
CHIP ENABLES
PD
1.5V
1.5V
VIH
VIL
TSW
TCDH
TCD
VIH
1.5V
1.5V
1.5V
1.5V
VIL
STROBE
TSL
TDL
OUTPUTS
1.5V
T.S.
TAA

A.C. TEST LOAD


300Ω
PROM OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7684/85

2K x 4 PROM

HM-7684 - Open Collector Outputs
HM-7685 - "Three State" Outputs

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7684/85 are a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 2K word by a 4 bit/word format with open collector (HM-7684) or "Three State" (HM-7685) outputs. These PROMs are available in an 18 pin DIP (ceramic or epoxy) and an 18 pin flatpack.

All bits are manufactured storing a logical "1"(positive logic) and can be selectively programmed for a logical "0" in any bit position.

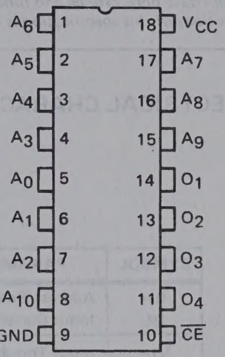
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7684/85 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

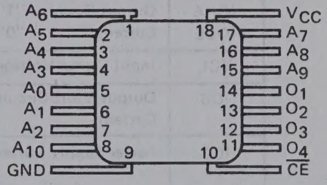
There is a chip enable on the HM-7684/85. $\overline{CE}$ low enables the chip.

Pinouts

TOP VIEW - DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
A10 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 O1
13 O2
12 O3
11 O4
10 CE

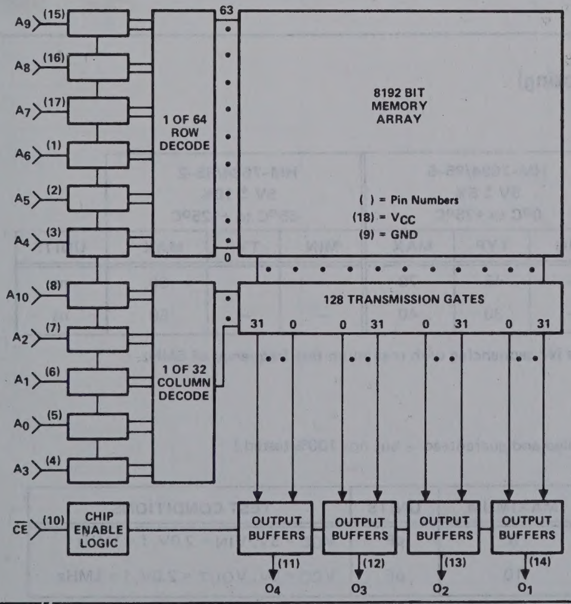
TOP VIEW - FLATPACK


A6
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
A10 8
GND 9
1
18
VCC
17 A7
16 A8
15 A9
14 O1
13 O2
12 O3
11 O4
10 CE

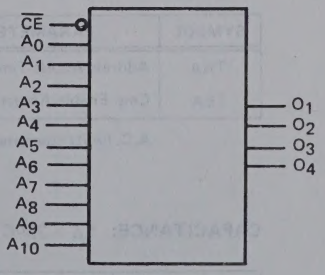
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}$	Chip Enable Input

Functional Diagram


A9 (15)
A8 (16)
A7 (17)
A6 (1)
A5 (2)
A4 (3)
A10 (8)
A2 (7)
A1 (6)
A0 (5)
A3 (4)
CE (10)
CHIP ENABLE LOGIC
1 OF 64 ROW DECODE
63
0
8192 BIT MEMORY ARRAY
( ) = Pin Numbers
(18) = VCC
(9) = GND
128 TRANSMISSION GATES
31 0 0 31 0 31 0 31
1 OF 32 COLUMN DECODE
OUTPUT BUFFERS
OUTPUT BUFFERS
OUTPUT BUFFERS
OUTPUT BUFFERS
(11) O4
(12) O3
(13) O2
(14) O1

Logic Symbol


CE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
O1
O2
O3
O4

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7684/85-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7684/85-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
IIH IIL	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	VIH = VCC Max. VIL = 0.45V
VIH VIL	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	VCC = VCC Min. VCC = VCC Max.
VOH VOL	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	IOH = -2.0mA, VCC = VCC Min. IOL = +16mA, VCC = VCC Min.
IOHE IOLE	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	VOH, VCC = VCC Max. VOL = 0.3V, VCC = VCC Max.
VCL	Input Clamp Voltage	–	–	-1.2	V	IIN = -18mA
IOS	Output Short Circuit Current	-15*	–	-100*	mA	VOUT = 0.0V, One Output at a Time for a Max. of 1 Second
ICC	Power Supply Current	–	120	170	mA	VCC = VCC Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

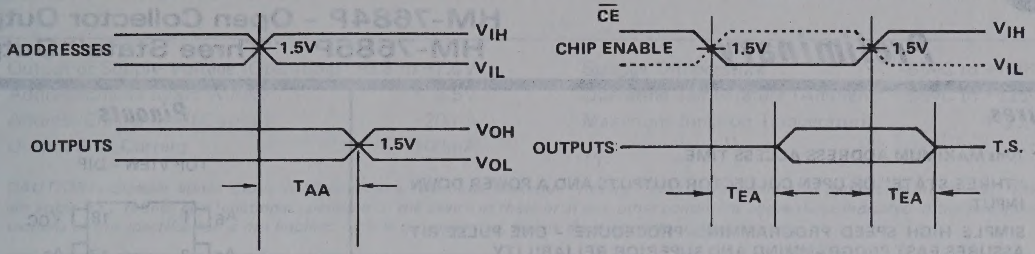
		HM-7684/85-5 5V ± 5% 0°C to +75°C			HM-7684/85-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TAA	Address Access Time	–	45	70	–	–	90	ns
TEA	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

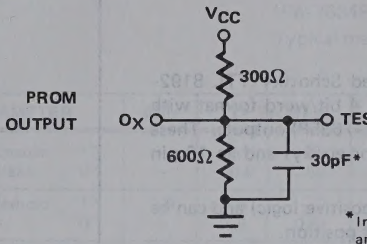
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	VCC = 5V, VIN = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	VCC = 5V, VOUT = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE
CHIP ENABLE
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA

A.C. TEST LOAD


VCC
300Ω
PROM OUTPUT
OX
TEST POINT
600Ω
30pF*

*Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7684P/85P
POWER DOWN 2K x 4 PROM

HM-7684P - Open Collector Outputs
HM-7685P - "Three State" Outputs

Preliminary

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A POWER DOWN INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMP. AND VOLT. RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7684P/85P are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K words by 4 bit/word format with open collector (HM-7684P) or "Three State" (HM-7685P) outputs. These PROMs are available in an 18 pin DIP (ceramic or epoxy) and an 18 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

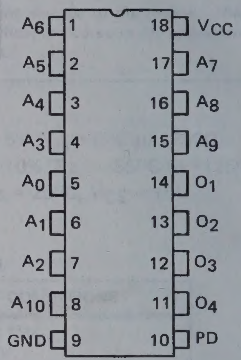
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7684P/85P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

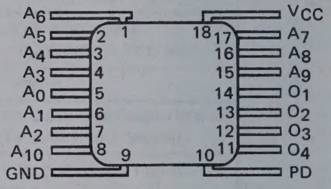
There is a power down input on the HM-7684P/85P which is similar to a chip enable. The chip is enabled or disabled using the power down input where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1 is low.

Pinouts

TOP VIEW - DIP


A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
A10 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 O1
13 O2
12 O3
11 O4
10 PD

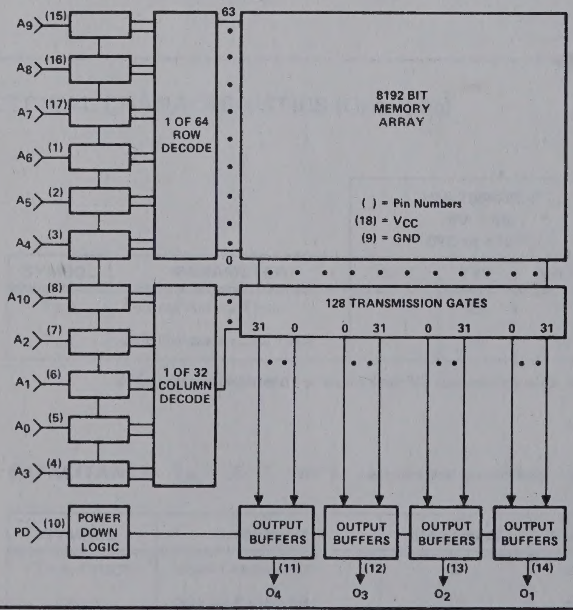
TOP VIEW - FLATPACK


A6
A5
A4
A3
A0
A1
A2
A10
GND
1
2
3
4
5
6
7
8
9
18
17
16
15
14
13
12
11
10
VCC
A7
A8
A9
O1
O2
O3
O4
PD

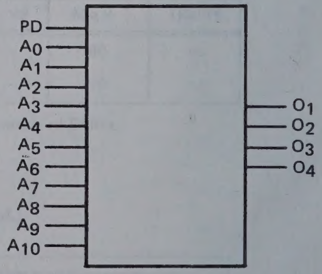
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
PD	Power Down Input

Functional Diagram


A9 (15)
A8 (16)
A7 (17)
A6 (1)
A5 (2)
A4 (3)
A10 (8)
A2 (7)
A1 (6)
A0 (5)
A3 (4)
PD (10)
1 OF 64 ROW DECODE
63
0
8192 BIT MEMORY ARRAY
( ) = Pin Numbers
(18) = VCC
(9) = GND
1 OF 32 COLUMN DECODE
128 TRANSMISSION GATES
31 0 0 31 0 31 0 31
POWER DOWN LOGIC
OUTPUT BUFFERS
OUTPUT BUFFERS
OUTPUT BUFFERS
OUTPUT BUFFERS
(11) O4
(12) O3
(13) O2
(14) O1

Logic Symbol


PD
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
O1
O2
O3
O4

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7684P/85P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7684P/85P-2 (V_{CC} 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*		-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.
I_{CCPD}	Power Supply Current During Power Down	–	30	40	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

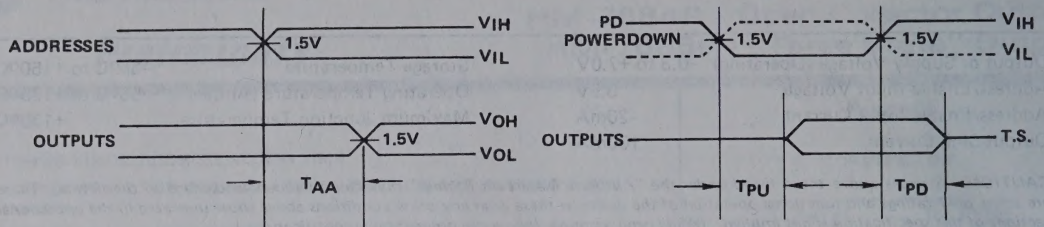
		HM-7684P/85P-5 5V ± 5% 0°C to +75°C			HM-7684P/85P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	45	70	-	-	90	ns
T_{PD}	Chip Power Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	100	150	-	-	200	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

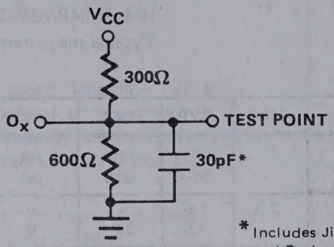
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed — but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
PD
POWERDOWN
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TPU
TPD

A.C. TEST LOAD


VCC
300Ω
PROM
OUTPUT
Ox
TEST POINT
600Ω
30pF*

* Includes Jig and Probe Total Capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7616

2K x 8 PROM

Features

- 80ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME — GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 2716

Description

HM-7616 is a fully decoded high speed Schottky TTL, 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

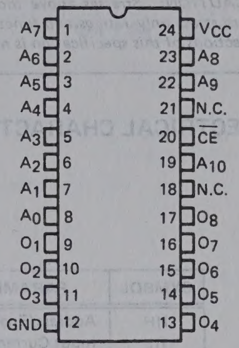
The Nickel-chromium fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510 PROMs.

The HM-7616 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

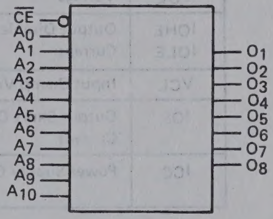
There is a chip enable input on the HM-7616. $\overline{CE}$ low enables the device.

Pinout

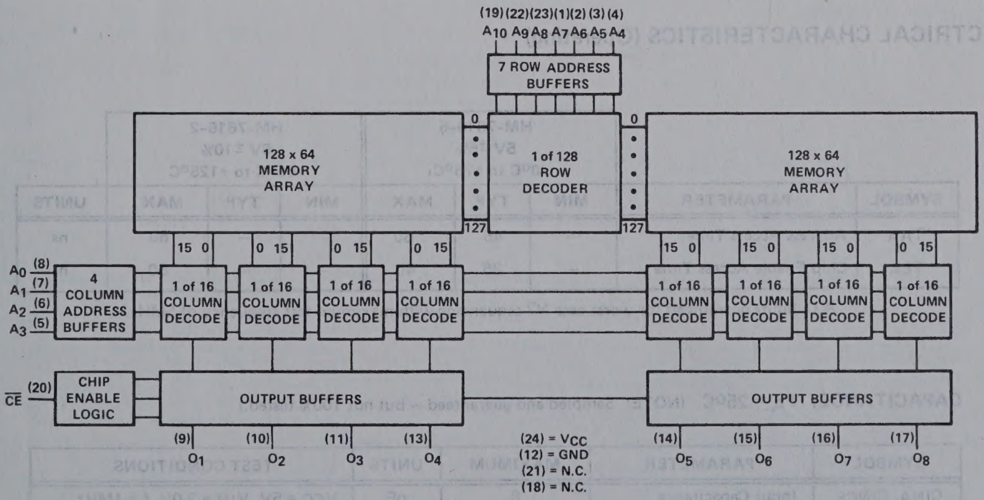
TOP VIEW - D I P


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 N.C.
20 CE
19 A10
18 N.C.
17 O8
16 O7
15 O6
14 O5
13 O4

Logic Symbol


$\overline{CE}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
O1
O2
O3
O4
O5
O6
O7
O8

Functional Diagram


(19)(22)(23)(1)(2) (3) (4)
A10 A9 A8 A7 A6 A5 A4
7 ROW ADDRESS BUFFERS
0
128 x 64 MEMORY ARRAY
1 of 128 ROW DECODER
0
128 x 64 MEMORY ARRAY
127
127
15 0
0 15
0 15
0 15
15 0
15 0
15 0
0 15
A0 (8)
A1 (7)
A2 (6)
A3 (5)
4 COLUMN ADDRESS BUFFERS
1 of 16 COLUMN DECODE
1 of 16 COLUMN DECODE
1 of 16 COLUMN DECODE
1 of 16 COLUMN DECODE
1 of 16 COLUMN DECODE
1 of 16 COLUMN DECODE
1 of 16 COLUMN DECODE
1 of 16 COLUMN DECODE
$\overline{CE}$ (20)
CHIP ENABLE LOGIC
OUTPUT BUFFERS
OUTPUT BUFFERS
(9) O1
(10) O2
(11) O3
(13) O4
(24) = VCC
(12) = GND
(21) = N.C.
(18) = N.C.
(14) O5
(15) O6
(16) O7
(17) O8

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7616-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7616-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	—	—	+40	μA	$V_{IH} = V_{CC}$ Max.
I_{IL}	Input Current "0"	—	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	—	V	$V_{CC} = V_{CC}$ Min.
V_{IL}	Voltage "0"	—	1.5	0.8	V	$V_{CC} = V_{CC}$ Max.
V_{OH}	Output "1"	2.4*	3.2	—	V	I_{OH} = -2.0mA, $V_{CC} = V_{CC}$ Min.
V_{OL}	Voltage "0"	—	0.35	0.50	V	I_{OL} = +16mA, $V_{CC} = V_{CC}$ Min.
I_{OHE}	Output Disable "1"	—	—	+ 40	μA	V_{OH}, $V_{CC} = V_{CC}$ Max.
I_{OLE}	Current "0"	—	—	- 40*	μA	V_{OL} = 0.3V, $V_{CC} = V_{CC}$ Max.
V_{CL}	Input Clamp Voltage	—	—	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	—	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	—	—	180	mA	$V_{CC} = V_{CC}$ Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

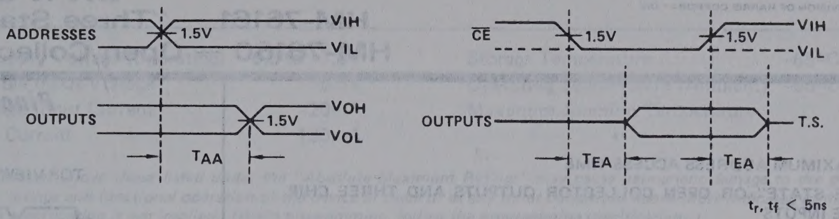
		HM-7616-5 5V ±5% 0°C to +75°C			HM-7616-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TAA	Address Access Time	—	45	60	—	—	80	ns
TEA	Chip Enable Access Time	—	35	40	—	—	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

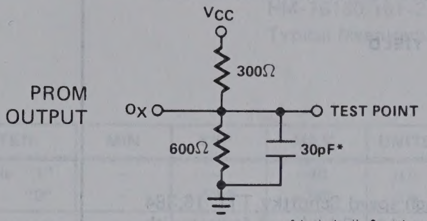
CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA
CE
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA
tr, tf < 5ns

A.C. TEST LOAD


VCC
300Ω
PROM OUTPUT
OX
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-76160/161

2K x 8 PROMS

HM-76161 — "Three State" Outputs
HM-76160 — Open Collector Outputs

Features

- 80ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP
- ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-76160/161 are fully decoded high speed Schottky TTL 16,384 bit Field Programmable ROMs in a 2K word by 8 bit/word format with open collector (HM-76160) or "Three State" (HM-76161) outputs. These PROMs are available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

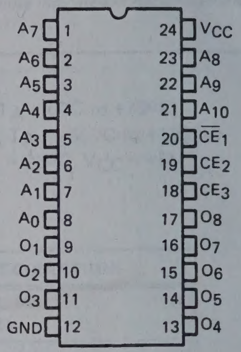
The nickel-chromium fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510 PROMs.

The HM-76160/161 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are three chip enable inputs on the HM-76160/161. $\overline{CE}_1$ low, CE$_2$ high, and CE$_3$ high enables the device.

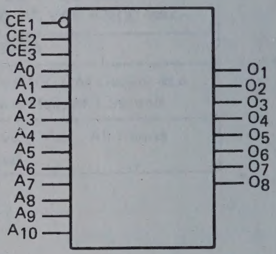
Pinout

TOP VIEW - D I P



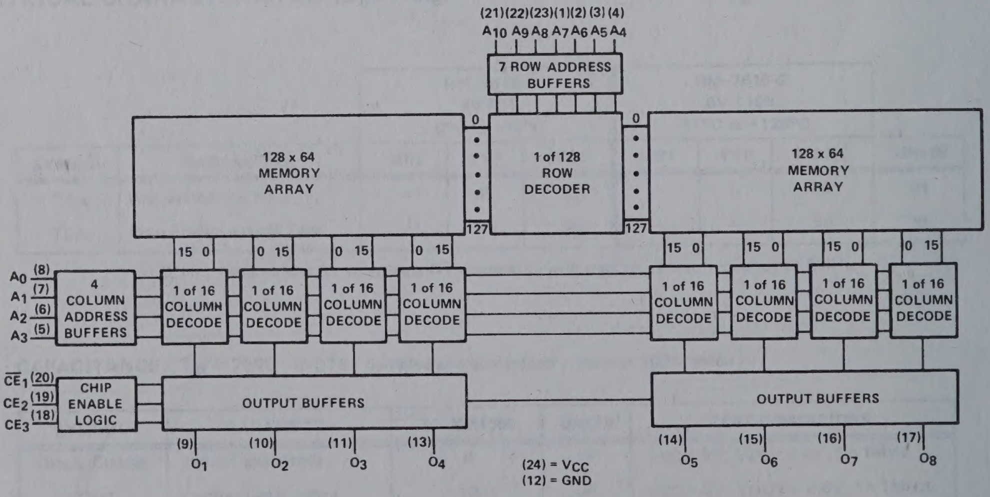
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O1 9
O2 10
O3 11
GND 12
24 VCC
23 A8
22 A9
21 A10
20 $\overline{CE}_1$
19 CE2
18 CE3
17 O8
16 O7
15 O6
14 O5
13 O4

Logic Symbol



$\overline{CE}_1$
CE2
CE3
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
O1
O2
O3
O4
O5
O6
O7
O8

Functional Diagram



(21)(22)(23)(1)(2)(3)(4)
A10 A9 A8 A7 A6 A5 A4
7 ROW ADDRESS BUFFERS
128 x 64 MEMORY ARRAY
1 of 128 ROW DECODER
128 x 64 MEMORY ARRAY
0
127
15 0
0 15
A0 (8)
A1 (7)
A2 (6)
A3 (5)
4 COLUMN ADDRESS BUFFERS
1 of 16 COLUMN DECODE
$\overline{CE}_1$ (20)
CE2 (19)
CE3 (18)
CHIP ENABLE LOGIC
OUTPUT BUFFERS
OUTPUT BUFFERS
(9) O1
(10) O2
(11) O3
(13) O4
(24) = VCC
(12) = GND
(14) O5
(15) O6
(16) O7
(17) O8

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76160/161-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76160/161-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1" Input Current	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Address/Enable "0" Input Current	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold Voltage "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Input Threshold Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Output Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable Current "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Output Disable Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

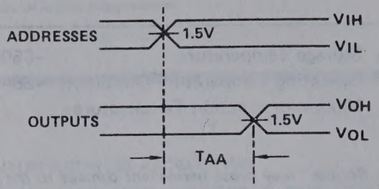
		HM-76160/161-5 5V ±5% 0°C to +75°C			HM-76160/161-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
TAA	Address Access Time	–	45	60	–	–	80	ns
TEA	Chip Enable Access Time	–	35	40	–	–	50	ns

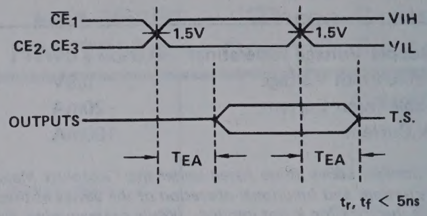
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

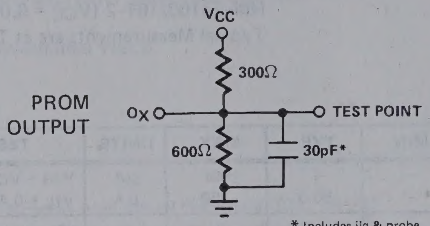
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS


ADDRESSES
1.5V
VIH
VIL
OUTPUTS
1.5V
VOH
VOL
TAA


CE1
CE2, CE3
1.5V
1.5V
VIH
VIL
OUTPUTS
T.S.
TEA
TEA
tr, tf < 5ns

A.C. TEST LOAD


VCC
300Ω
PROM
OUTPUT
Ox
TEST POINT
600Ω
30pF*

* Includes jig & probe total capacitance

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

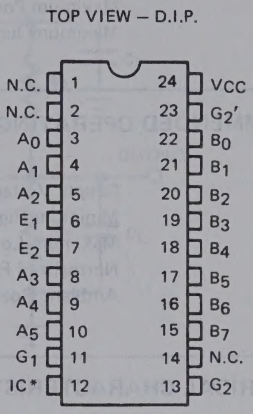
JAN-0512

512 BIT, BIPOLAR PROM
MIL/M38510/20101

Features

- FIELD PROGRAMMABLE
- 64 WORDS/8 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 55ns ACCESS TIME

Pinout

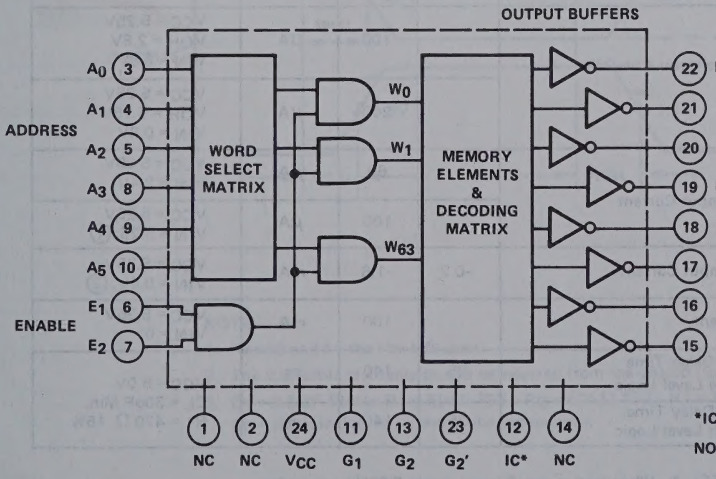

TOP VIEW – D.I.P.
N.C. 1
N.C. 2
A0 3
A1 4
A2 5
E1 6
E2 7
A3 8
A4 9
A5 10
G1 11
IC* 12
24 VCC
23 G2'
22 B0
21 B1
20 B2
19 B3
18 B4
17 B5
16 B6
15 B7
14 N.C.
13 G2

*Must be left open circuit

Description

The JAN-0512 is a field programmable 64 word by 8 bit PROM. In an unprogrammed memory, all "Memory Elements" are short circuits so that logical "zeros" appear at each output bit position for any address input. "Electronic Programming" involves the alteration of specific "Memory Elements" to create logical "ones" in selected bit positions. This alteration is irreversible and cannot be accomplished under normal operating conditions.

Block Diagram


OUTPUT BUFFERS
ADDRESS
A0 3
A1 4
A2 5
A3 8
A4 9
A5 10
ENABLE
E1 6
E2 7
WORD SELECT MATRIX
W0
W1
W63
MEMORY ELEMENTS & DECODING MATRIX
22 B0
21 B1
20 B2
19 B3
18 B4
17 B5
16 B6
15 B7
1 NC
2 NC
24 VCC
11 G1
13 G2
23 G2'
12 IC*
14 NC

*IC – Internal Connection must be left open

NOTE: For operational condition, return pins 11, 13, and 23 to system ground.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	-0.5 V_{DC} to 7.0 V_{DC}
Input Voltage Range	-1.5 V_{DC} at -12mA to 5.5V_{DC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	300°C
Thermal Resistance, Junction-to-Case	JC' Case J = 30°C/w
Output Supply Voltage	-0.5V_{DC} to 7.0V_{DC}
Output Sink Current	+30mA
Maximum Power Dissipation, P_D	575mWdc
Maximum Junction Temperature, T_J	175°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	4.75 V_{DC} Min. to 5.25V_{DC} Maximum
Minimum High Level Input Voltage	2.0V_{DC}
Maximum Low Level Input Voltage	0.8V_{DC}
Normalized Fanout (Each Output)	6 Maximum (10mA)
Ambient Operating Temperature Range	-55°C to +125°C

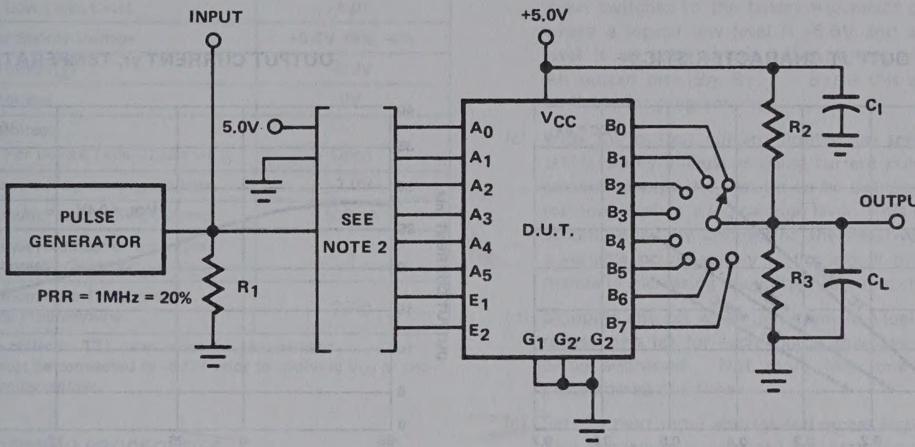
ELECTRICAL CHARACTERISTICS

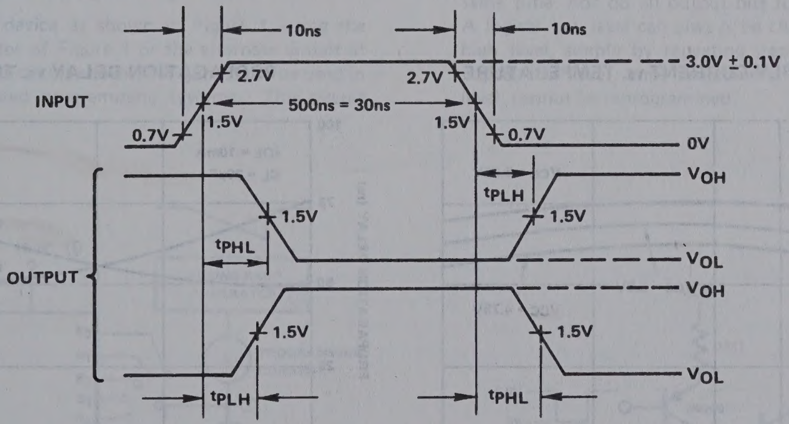
The electrical characteristics are as specified in the table and apply over the full recommended ambient operating temperature range, unless otherwise specified.

SYMBOL	TEST	LIMITS		UNITS	TEST CONDITIONS
		MIN	MAX		
V_{OL}	Low Level Output Voltage		0.45	Volts	V_{CC} = 4.75V V_{IN} = 2.0V I_{OL} = 10mA
V_{IC}	Input Clamp Voltage		-1.5	Volts	V_{CC} = 4.75V I_{IN} = -12mA T_A = 25°C
I_{CEX1}	Maximum Collector Cut-Off Current		100	μA	V_{CC} = 5.25V V_{OH} = 2.8V V_{IN} = 0.8V
I_{CEX2}			200	μA	V_{CC} = 5.25V V_{OH} = 5.25V V_{IN} = 0.8V
I_{IH1}	High Level Input Current		60	μA	V_{CC} = 5.25V V_{IN} = 2.4V;
I_{IH2}			100	μA	V_{CC} = 5.25V V_{IN} = 5.25; ①
I_{IL}	Low Level Input Current	-0.2	-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.4V; ②
I_{CC}	Supply Current		100	mA	V_{CC} = 5.25V V_{IN} = 0
t_{PHL}	Propagation Delay Time High-to-Low Level Logic	25	140	ns	V_{CC} = 5.0V C_L = 30pF Min. R_1 = 470 Ω ±5%
t_{PLH}	Propagation Delay Time Low-to-High Level Logic	25	140	ns	

NOTES: 1. When testing one E input, apply 5.25V to the other.
2. When testing one E input, apply GND to the other.

Switching Time Test Circuits


INPUT
5.0V
PULSE GENERATOR
PRR = 1MHz = 20%
R1
SEE NOTE 2
+5.0V
A0
A1
A2
A3
A4
A5
E1
E2
VCC
D.U.T.
G1 G2' G2
B0
B1
B2
B3
B4
B5
B6
B7
R2
C1
OUTPUT
R3
CL

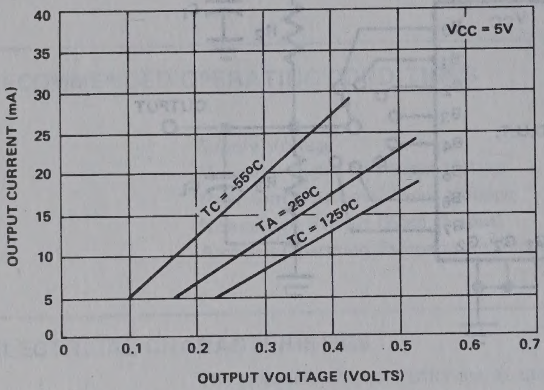

10ns
10ns
3.0V ± 0.1V
INPUT
2.7V
2.7V
500ns = 30ns
1.5V
1.5V
0.7V
0.7V
0V
VOH
tPLH
1.5V
1.5V
tPHL
VOL
OUTPUT
VOH
1.5V
1.5V
VOL
tPLH
tPHL

NOTES:

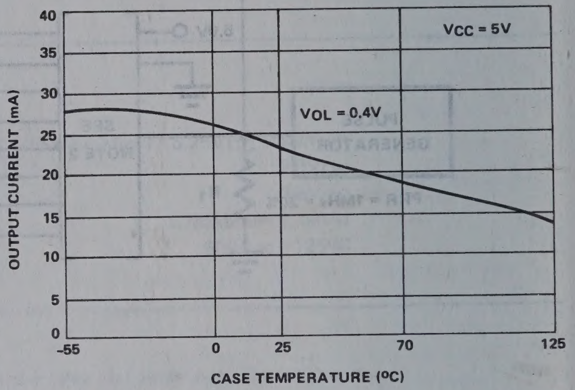
1. Pins 12 and 14 shall be left open.
2. The applicable test table should be selected from the altered item drawing.
3. $C_1 = 0.5\mu F \pm 10\%$; $R_1 = 50\Omega \pm 5\%$; $R_2 = 470\Omega \pm 5\%$; $R_3 = 1k\Omega \pm 5\%$; $C_L = 30pF$ including jig and probe capacitance.

Characteristic Curves

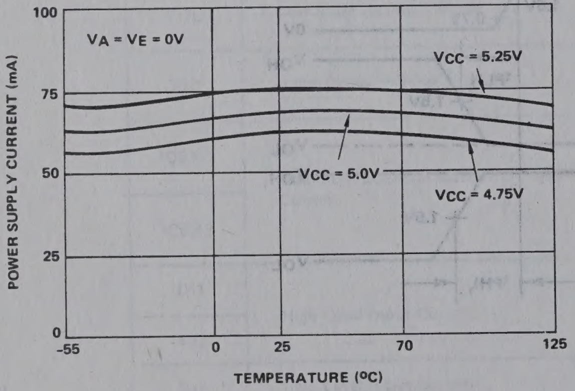
OUTPUT CHARACTERISTICS



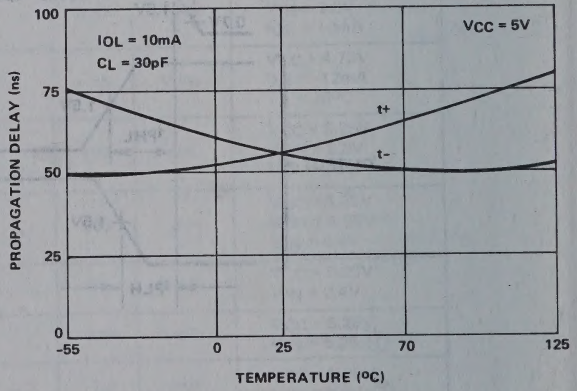
OUTPUT CURRENT vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



JAN-0512 Programming Procedure

PROGRAMMING SPECIFICATIONS

PARAMETER	VALUE
Address Input Voltage High Logic Level Low Logic Level	 Open Circuit ① -5.0V
Power Supply Voltage	+5.0V +5%, -0%
G1 Voltage ②	-5.0V
G2 Voltage	0V
G2′ Voltage For Device Type 01 Circuit A	 Open
Maximum Programming Voltage	-7.0V
Maximum Programming Current	100mA
Maximum Number or Attempts to Program a Given Bit	2
Maximum Case Temperature During Programming	75°C

1. Open collector TTL gates meet this requirement.
2. G_1 must be connected to -5.0V prior to applying V_{CC} or programming voltage.

PROGRAMMING PROCEDURES

Using the test conditions of the table, the following procedures shall be used for programming the device:

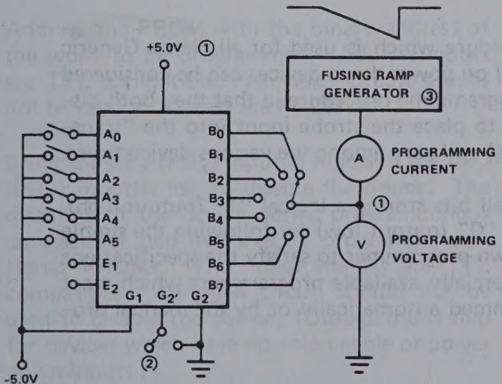
(a) Connect the device as shown in Figure 1, using the fusing generator of Figure 1 or the alternate circuit of Figure 2. The circuit shown in Figure 2 can be used in more automated programming systems. This circuit generates a current pulse which is at the proper voltage and current levels for fast reliable programming. The input programming pulse width shall be 750ms ±50ms. The number of attempts to program a given bit shall be as specified in the table.

(b) To address a particular word in the memory, set the input switches to the binary equivalent of that word, where a logical low level is -5.0V and a logical high level is an open circuit. (Do not return to supply). All output bits (B_0, B_1, . . . B_7) of this word are now available for programming.

(c) With the output current limited (as specified in the table), apply a negative going current pulse to the pin associated with the first bit to be changed from a logical low level to a logical high level. This is most easily accomplished by connecting the negative terminal of a variable power supply to the proper output pin and manually increasing the voltage to approximately 6.0V.

(d) Skipping any bit which is to remain a logical low level, repeat step (c) for each logical low level in the word being addressed. Not more than one bit shall be programmed at a time.

(e) Set the next input address and repeat steps (c) and (d). This procedure is repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A logical low level can always be changed to a logical high level, simply by repeating steps (b) and (c). A logical low level, once programmed to a logical high level, cannot be reprogrammed.



NOTES:
1. Connect -5.0V to G_1 before applying V_{CC} or programming voltage.
2. For device type 01, G_2' shall be open.
3. Generator characterisitics are defined in Programming Procedures.

FIGURE 1
PROGRAMMING CONNECTIONS

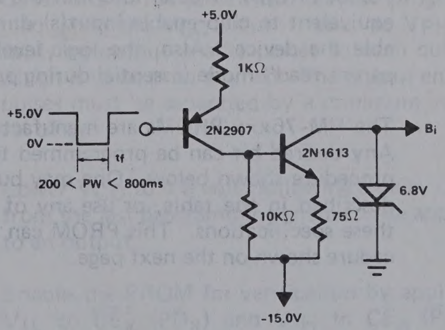


FIGURE 2
PROGRAMMING CIRCUIT

All 76xxx series devices utilize the same programming method which is one of the characteristics that lends to the term "Generic" PROM.

Harris Generic PROMs have the industry's highest programming yield and exhibit an extremely high level of reliability in the field, however, this level of device quality can only be obtained if the PROM has been properly programmed to the data sheet specifications. Outlined below are the key points which deserve attention to assure that programming has been optimumly performed.

- Be certain that you are following the latest revision status of programming specifications.
- If you are utilizing a commercial programmer, be sure that the card set for Harris Generic PROMs is certified for the most recent revision level.
- Have the Programmer calibrated at routine intervals to assure that the electrical and mechanical characteristics are acceptable. This would include such things as:
    - Making certain that the socket which the device is placed into is clean, free of corrosion and is mechanically sound.
    - Check ribbon cable connectors for good continuity.
    - Making sure that all voltage levels conform to the programming specifications.
    - Assuring that all pulses are clean of distortion and exhibit the correct timing characteristics.

If there is any problem in determining how to follow any of these guidelines, contact a local Harris office for assistance.

PROGRAMMING PROCEDURE

The following is the generic programming procedure which is used for all Harris Generic 76xxx PROMs. Please note that the PD input(s) on power down devices can be considered equivalent to chip enable input(s) during the programming procedure in that they both disable the device. Also, the logic levels required to place the strobe input into the "transparent read" mode (essential during programming) will vary among the various device types.

The HM-76xxx PROMs are manufactured with all bits storing a logical "1" (output high). Any desired bit can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build their own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications. This PROM can be programmed automatically or by the manual procedure shown on the next page.

Programming Specifications

SYMBOL	PARAMETER	MINIMUM	RECOMMENDED OR TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to VCC	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low Current at V_{PH}	–	-300	-600	μA
tr tf	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	μs μs
td	Programming Delay	10	10	100	μs
tp	Programming Pulse Width (4)	90	100	110	us
P.D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (6) Disable (5)	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
Ta	Ambient Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable of supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min and V_{PL} max.
4. Note step 11 in programming procedure.
5. Disable condition will be met with output open circuited.
6. V_{OPE} supply must be capable of supplying 10mA.

1. If the device has latched outputs (HM-76xxR): apply a logic "1" to the strobe input to place the device into the "transparent read" mode which is essential during programming. The strobe must remain in the "transparent read" mode throughout the entire programming procedure.

2. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

3. Bring the $\overline{CE}_X$ (PD_X) input(s) high and the CE_X ($\overline{PD}_X$) input(s) low to disable the device. The disabling of the device during programming is an essential step in correctly programming all Harris PROMs. The chip enables are TTL compatible. An open circuit should not be used to disable the device. (Disregard this step for devices which have no chip enable or power down inputs.)

4. Disable the programming circuitry by applying a voltage disable of V_{OPD} to the outputs of the PROM. Any output may be left open to achieve the disable.

5. Raise V_{CC} to V_{PH} with rise time $\leq t_r$.

6. After a delay $\geq t_d$, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is manufactured with fuses intact which generate an output high. Programming a fuse will cause the output to be in the V_{IL} state in the verify mode.

7. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

8. Lower V_{CC} to 4.5 volts following a delay of t_d from the last programming enable pulse applied to an output.

9. Enable the PROM for verification by applying V_{IL} to $\overline{CE}_X$ (PD_X) and V_{IH} to CE_X ($\overline{PD}_X$).

10. Repeat verification (step 9) at V_{CC} = 5.5 volts.

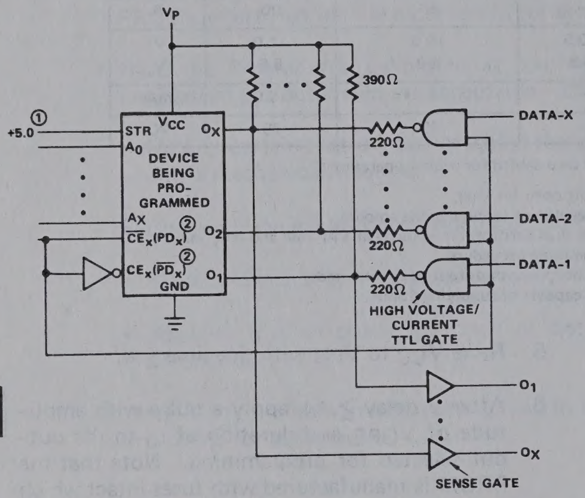
11. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1msec of programming time. Bits which do not program within 1msec are programming rejects. No further attempt to program these parts should be made.

12. Repeat steps 1 through 11 for all other bits to be programmed in the PROM.

13. Programming rejects returned to the factory must be accompanied by data giving address, desired data, and actual output data of the location in which a programming failure has occured.

Typical Programming Circuit

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand up to 11.0 volts during programming.

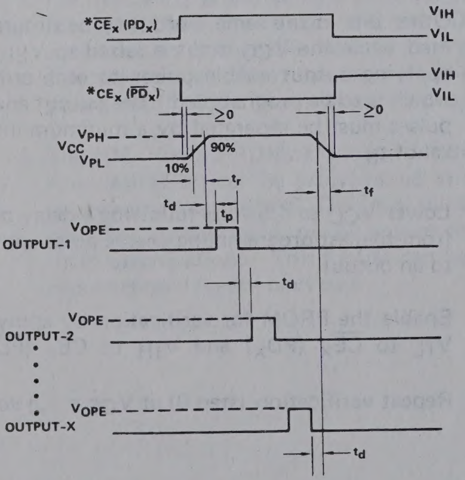


V_P
390Ω
①
+5.0
STR
V_{CC}
O_X
A_0
DEVICE BEING PRO-GRAMMED
A_X
$\overline{CE}_X(PD_X)$ ②
O_2
$CE_X(\overline{PD}_X)$ ②
O_1
GND
220Ω
220Ω
220Ω
DATA-X
DATA-2
DATA-1
HIGH VOLTAGE/ CURRENT TTL GATE
O_1
O_X
SENSE GATE

FIGURE 1

① The strobe input must remain at V_{IH} throughout the procedure. (for latched output devices only.)

② Disregard for devices with no enable inputs.



$*\overline{CE}_X(PD_X)$
V_{IH}
V_{IL}
$*CE_X(\overline{PD}_X)$
V_{IH}
V_{IL}
≥0
≥0
V_{PH}
V_{CC}
V_{PL}
90%
10%
t_r
t_f
t_d
t_p
V_{OPE}
OUTPUT-1
t_d
V_{OPE}
OUTPUT-2
V_{OPE}
OUTPUT-X
t_d

FIGURE 2

* Disregard for devices with no enable inputs.

The strobe input must remain at V_{IH} throughout the procedure. (for latched output devices only.)

This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit, resulting in a low output for that bit. Therefore, a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

Programmer Evaluation

Programming equipment models identified in the accompanying list have been spot checked by Harris Semiconductor and found to be acceptable for use in programming HARRIS PROMs. This list is provided only as a convenience to purchasers of HARRIS PROMs to identify programmer models potentially suitable for programming the PROMs. It is neither intended to be a representation or warranty by Harris of the capability of all listed programmer models nor an indication of unsuitability of other programmer models not contained in the list. PROM purchasers are advised to adhere to the programming requirements specified in HARRIS current data sheets applicable to the PROMs to be programmed. Responsibility for programmer performance lies solely with the equipment manufacturer. The programmer user is cautioned to verify operation and performance according to the manufacturer's instructions and specifications prior to each use, and to determine that the programming complies with the applicable HARRIS PROM data sheet. Harris accepts no responsibility for PROMs which have been subjected to incorrect or faulty programming.

DATA I/O Main Frame: All in which 909-XXXX card sets are specified.

CARD SET	PRODUCTS	COMMENTS
950-0099 UNI PAK	HM-76XX	No Additional hardware required.
909-1063-4 Rev S	HM-76XX	Preferred Requires specified socket adapter.
909-1063-4 Rev H	HM-76XX	Acceptable Requires specified socket adapter.
909-1319-3 Rev D	HM-6611/6661-X	Requires specified socket adapter.
909-1054-3 Rev E	HMX-0512-X	

PROLOG Main Frame: Model M909

MODULE	PRODUCTS	COMMENTS
PM 9031	HM-7602	
PM 9027	HM-7610/11	
	HM-7620/21	
PM 9029	HM-7640/41	
PM 9036	HM-7642/43	
PM 9039A	HM-76XX	Preferred Generic Module requires respective
PM 9039	HM-76XX	Acceptable socket and configurator.
PM 9055	JAN-0512	
PM 9056	HM-6611	

INTERNATIONAL MICROSYSTEMS INC. Main Frame: IM 1000

MODULE	PRODUCTS	COMMENTS
IM-1063	HM-76XX	Generic Module requires specified socket adapter.

DIGITRONICS, ISRAEL LTD. Main Frame: UPP/801

MODULE	PRODUCTS	COMMENTS
PM 106	HM-76XX	Generic Module requires specified interface socket.
PM 130	HM-6611	Requires specified interface socket.

SUNRISE ELECTRONICS Main Frame: Smarty SM-100

MODULE	PRODUCTS	COMMENTS
Family Slave	HM-76XX	Sockets are part of slave unit.

KONTRON ELECTRONICS Main Frame: MPP805

MODULE	PRODUCTS	COMMENTS
#6	HM-76XX	Requires specified socket adapter.

STOLZ AG Main Frame: Maestro M2

MODULE	PRODUCTS	COMMENTS
HM-76XX	HM-76XX	Requires specified socket adapter.

Data Entry Formats for Harris Custom Programming *

For Harris to custom program to a user data pattern specification, the user must supply the data in one of the following formats:

1. Master PROM of same organization and pinout as device ordered. Two pieces required, three preferred.
2. Paper tape in Binary or ASCII BPNF.

* BINARY PAPER TAPE FORMAT

- A minimum of six inches of leader.
- A rubout (all eight locations punched).
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N"), with no interruptions or extraneous characters of any kind.
- Specifiy whether a punched hole is a VOH = "1" = logic high or is a VOL = "0" = logic low.
- A minimum trailer of six inches of tape.

* ASCII BPNF FORMAT

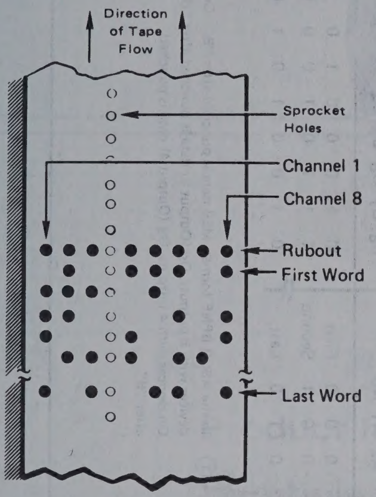
- A minimum leader of twenty rubouts (all eight locations punched).
- Any characters desired (none necessary) except "B".
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N").
- Data words consist of:
  1. The character "B" denoting the beginning of a data word.
  2. A sequence of characters, only "P" or "N", one character for each bit in the word.
  3. The character "F" denoting the finish of the data word.
- No extraneous characters of any kind may appear within a data word (between any "B" and the next "F").
- Errors may be deleted by rubouts superimposed over the entire word including the "B", and beginning the word again with a new "B".
- Any text of any kind (except the character "B") is allowed between data words (between any "F" and the next "B"), including carriage return and line feed.
- A minimum trailer of twenty-five rubouts.
- Specify whether a "P" is a "1" = VOH = logic high or is a "0" = VOL = logic low.
- The use of even or odd parity is optional.

2

---

* *Harris can not assume responsibility for PROMs programmed to data tapes or masters which contain errors. The user must insure the accuracy of the data provided to Harris. Harris guarantees that the programmed PROMs will contain the information provided if either of the following formats are followed.*

BINARY PAPER TAPE EXAMPLE


Direction of Tape Flow
Sprocket Holes
Channel 1
Channel 8
Rubout
First Word
Last Word

Punched Hole = "0" = VOL = Logic Low

Word				PROM Output Data ①								
				Channel	8	7	6	5	4	3	2	1
AX ··· A2	A1	A0		Output	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ···· 0	0	0	First		0	1	0	0	0	1	0	1
0 ···· 0	0	1	Second		1	1	1	0	1	0	0	0
0 ···· 0	1	0	Third		0	1	0	1	1	1	0	0
0 ···· 0	1	1	Fourth		0	1	1	1	0	1	1	0
0 ···· 1	0	0	Fifth		1	0	0	1	0	0	0	1
1 ···· 1	1	1	Last		0	1	0	0	1	0	1	0

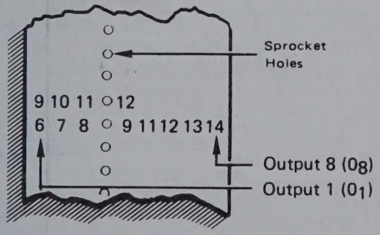
NOTES:

① PROMs with 4 bit wide data outputs require punching only first 4 channels on tape (Channels 1 thru 4).

② On HARRIS PROMs O_X (Example: O_1) designates a respective output pin on the device. O_1 (Output 1) is always LSB.

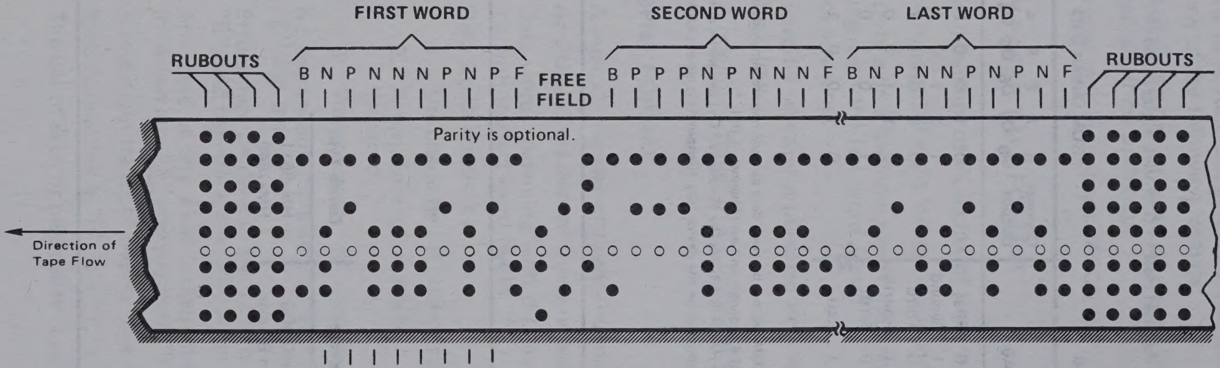
DEVICE OUTPUT PACKAGE PINS

EXAMPLE:


Sprocket Holes
9 10 11 12
6 7 8 9 11 12 13 14
Output 8 (O_8)
Output 1 (O_1)

Package	Device Type
16 Pin CMOS	HM-6611
20 Pin Bipolar	HM-7649

ASCII BPNF PAPER TAPE EXAMPLE


FIRST WORD
SECOND WORD
LAST WORD
RUBOUTS
B N P N N N P N P F
FREE FIELD
B P P P N P N N N F
B N P N N P N P N F
RUBOUTS
Parity is optional.
Direction of Tape Flow

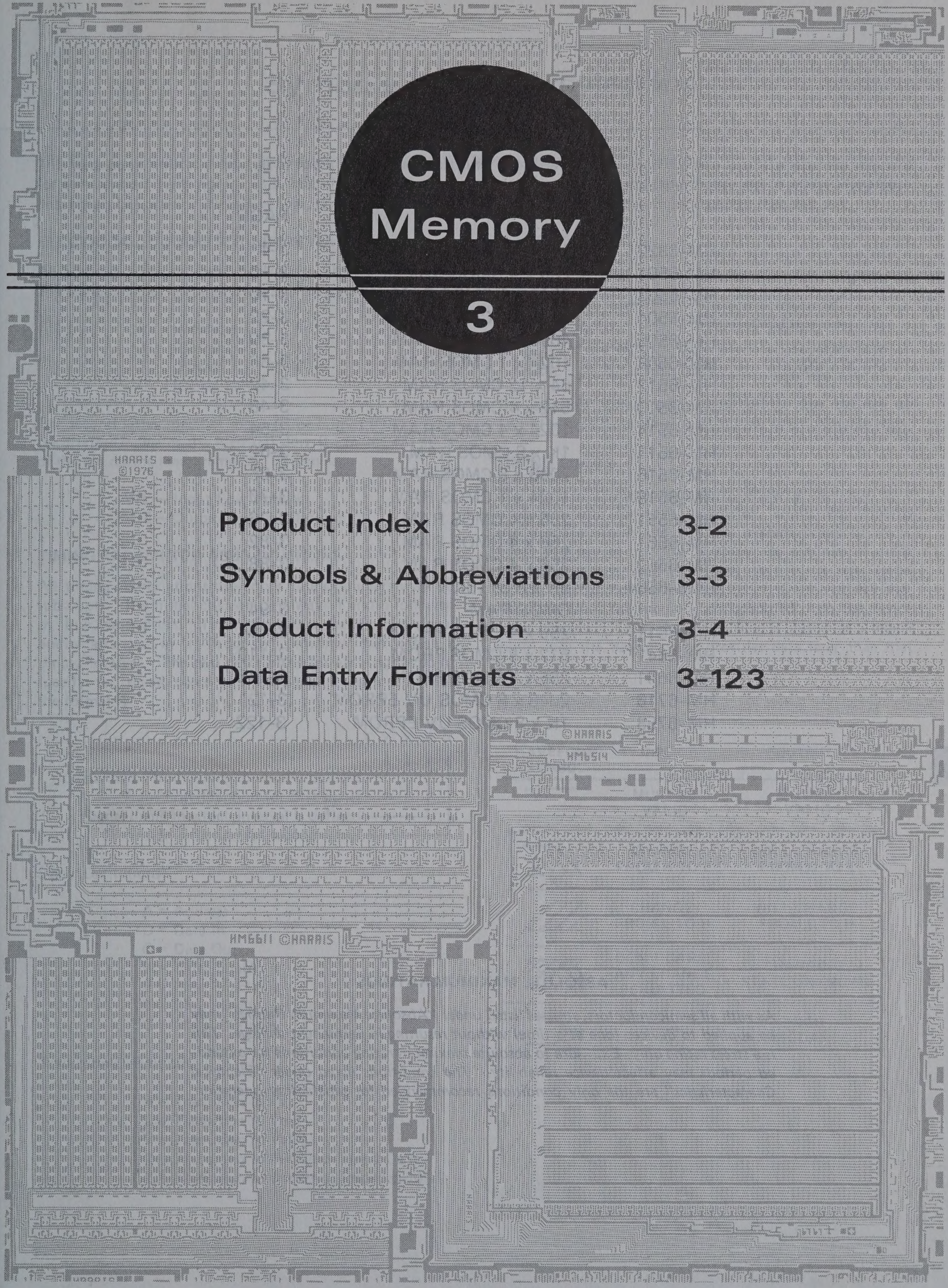
EXAMPLE	PACKAGE TYPE	DEVICE OUTPUT PINS
HM-6611	16 Pin Pkg.	12 11 10 9 (MOS)
HM-7649	20 Pin Pkg.	14 13 12 11 9

Truth Table
Character "D" = "1" = VOH = Logic High
Character "V" = "0" = VOL = Logic Low

Word					PROM Outputs Data ①							
AX ···· A2	A1	A0			O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ····· 0	0	0	First		0	1	0	0	0	1	0	1
0 ····· 0	0	1	Second		1	1	1	0	1	0	0	0
1 ····· 0	1	0	Last		0	1	0	0	1	0	1	0

NOTES:

① In the ASCII BPNF format, MSB data is punched after "B". On devices with 8 outputs, O_8 (Output 8) data is punched after "B". On devices with 4 outputs, O_4 (Output 4) data is punched after "B".


HARRIS
©1976
©HARRIS
HM6514
HM6611 ©HARRIS

CMOS Memory

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HM-6512	64 x 12 CMOS RAM	3-42
HM-6513	512 x 4 CMOS RAM	3-48
HM-6514	1024 x 4 CMOS RAM	3-54
HM-6515	1K x 8 CMOS RAM	3-62
HM-6516	2048 x 8 CMOS RAM	3-66
HM-6518	1024 x 1 CMOS RAM	3-70
HM-6551	256 x 4 CMOS RAM	3-76
HM-6561	256 x 4 CMOS RAM	3-82
HM-6562	256 x 4 CMOS RAM	3-88
HM5-6564	8K x 8 or 16K x 4 CMOS RAM	3-94
HM-6611	256 x 4 CMOS PROM	3-104
HM-6641	512 x 8 CMOS PROM	3-110
HM-6661	256 x 4 CMOS PROM	3-115
HM-6716	2048 x 8 CMOS UV EPROM	3-121
HM-6758	1K x 8 CMOS UV EPROM	3-122

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Symbols and Abbreviations

This data book utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

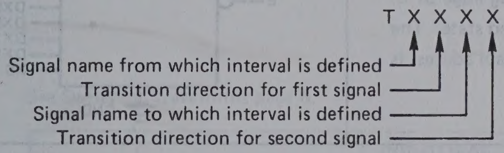
V	(Voltage)
I	(Current)
P	(Power)
C	(Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:


T X X X X
Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

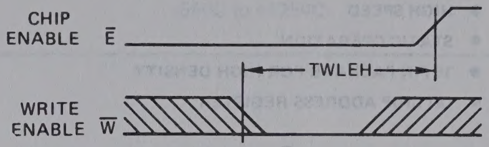
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

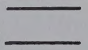
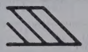
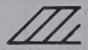
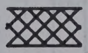
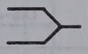


The example shows Write pulse setup time defined as TWLEH–Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6322

CMOS ROM

1024 Word x 12 Bit

Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY 500μW
- HIGH SPEED
- STATIC OPERATION
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Description

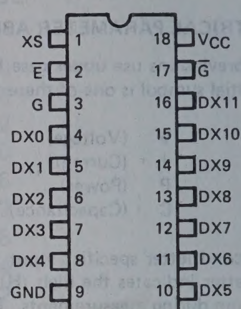
The HM-6322 is a high speed, low power, silicon gate CMOS Static ROM, organized 1024 words by 12 bits, with multiplexed data and address lines. The XS output pin is a mask programmable, external select line used to activate an external device, usually RAM. Signal polarities and functions are specified for direct compatibility with the HM-6100.

Operation

Address and data out are multiplexed on the 12 DX lines (DX0 - DX11). The address is latched into the on chip register by the falling edge of $\overline{E}$. Data out becomes valid when $\overline{E}$, $\overline{G}$ and G are all in the enabled state. The XS pin becomes valid a propagation delay after an appropriate address is presented to the address register.

Pinout

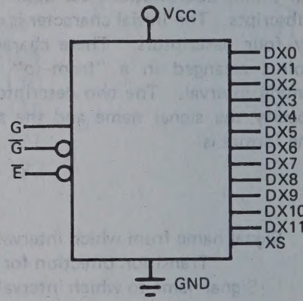
TOP VIEW—DIP


XS 1
$\overline{E}$ 2
G 3
DX0 4
DX1 5
DX2 6
DX3 7
DX4 8
GND 9
18 VCC
17 $\overline{G}$
16 DX11
15 DX10
14 DX9
13 DX8
12 DX7
11 DX6
10 DX5

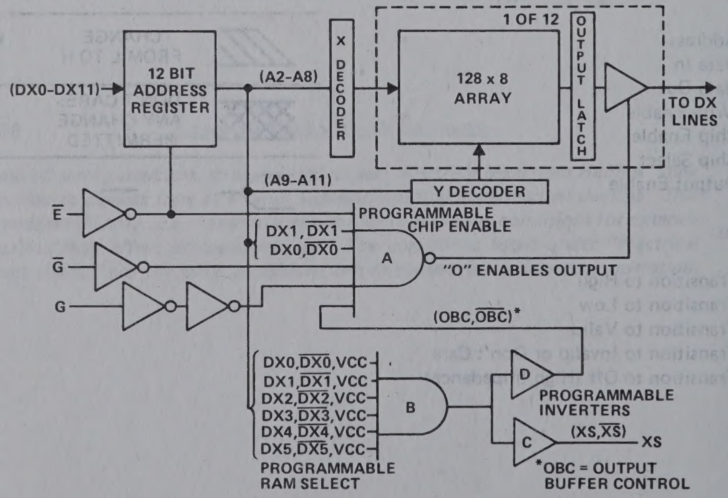
PIN NAMES

DX – Address Input and Data Out
$\overline{E}$ – Chip Enable
G – Output Enable
$\overline{G}$ – Output Enable
XS – External Select

Logic Symbol


VCC
G
$\overline{G}$
$\overline{E}$
DX0
DX1
DX2
DX3
DX4
DX5
DX6
DX7
DX8
DX9
DX10
DX11
XS
GND

Functional Diagram


(DX0-DX11)
12 BIT ADDRESS REGISTER
(A2-A8)
X DECODER
1 OF 12
128 x 8 ARRAY
OUTPUT LATCH
TO DX LINES
(A9-A11)
Y DECODER
$\overline{E}$
PROGRAMMABLE CHIP ENABLE
DX1,$\overline{DX1}$
DX0,$\overline{DX0}$
$\overline{G}$
A
"O" ENABLES OUTPUT
G
(OBC,$\overline{OBC}$)*
DX0,$\overline{DX0}$,VCC
DX1,$\overline{DX1}$,VCC
DX2,$\overline{DX2}$,VCC
DX3,$\overline{DX3}$,VCC
DX4,$\overline{DX4}$,VCC
DX5,$\overline{DX5}$,VCC
B
D
PROGRAMMABLE INVERTERS
C
(XS,$\overline{XS}$)
XS
PROGRAMMABLE RAM SELECT
*OBC = OUTPUT BUFFER CONTROL

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	GND -0.3 to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial -9	-40°C to +85°C
Military -2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ± 10%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	3.0			V	
VIL	Logical "0" Input Voltage			1.1	V	
IIL	Input Leakage	-1.0		+1.0	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage	3.5			V	IOUT = -2.0mA
VOL	Logical "0" Output Voltage			0.4	V	IOUT = 2.0mA
IO	Output Leakage	-1.0		1.0	μA	0V ≤ VO ≤ VCC
ICCSB	Standby Supply Current			100	μA	VI = 0 or VCC
ICCOP	Operating Current ①		3	5	mA	f = 1MHz, IO = 0
CI	Input Capacitance ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance ②		6.0	10.0	pF	

See Switching Waveforms page 6.

A.C.

SYMBOL	PARAMETER	INDUSTRIAL		MILITARY		UNITS	TEST CONDITIONS ③
		MIN	MAX	MIN	MAX		
TELQV	Access Time from $\overline{E}$		350		400	ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		160		180	ns	
TGLQZ	Output Disable Time		160		180	ns	
TEHEL	Strobe Pos. Pulse Width	80		90		ns	
TELEL	Cycle Time	430		490		ns	
TAVEL	Address Set-Up Time	40		50		ns	
TELAX	Address Hold Time	40		50		ns	
TELXSV	Propagation to XS		110		125	ns	

NOTES:

① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 3mA/MHz.

② Capacitance sampled and guaranteed - not 100% tested.

③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - CLoad = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6322C-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC – GND)	-0.3V to +8.0V
Applied Input or Output Voltage	GND -0.3 to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ± 10%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	3.0			V	
VIL	Logical "0" Input Voltage			0.8	V	
IIL	Input Leakage	-10		+10	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage	3.5			V	IOUT = -1.0mA
VOL	Logical "0" Output Voltage			0.4	V	IOUT = 1.0mA
IO	Output Leakage	-10		10	μA	0V ≤ VO ≤ VCC
ICCSB	Standby Supply Current			500	μA	VI = 0 or VCC
ICCOP	Operating Current ①		3	5	mA	f = 1MHz, IO = 0
CI	Input Capacitance ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance ②		6.0	10.0	pF	

See Switching Waveforms page 6.

A.C.

SYMBOL	PARAMETER	INDUSTRIAL		UNITS	TEST CONDITIONS ③
		MIN	MAX		
TELQV	Access Time from $\overline{E}$		500	ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		250	ns	
TGLQZ	Output Disable Time		250	ns	
TEHEL	Strobe Pos. Pulse Width	250		ns	
TELEL	Cycle Time	750		ns	
TAVEL	Address Set-Up Time	75		ns	
TELAX	Address Hold Time	100		ns	
TELXSV	Propagation to XS		200	ns	

NOTES:

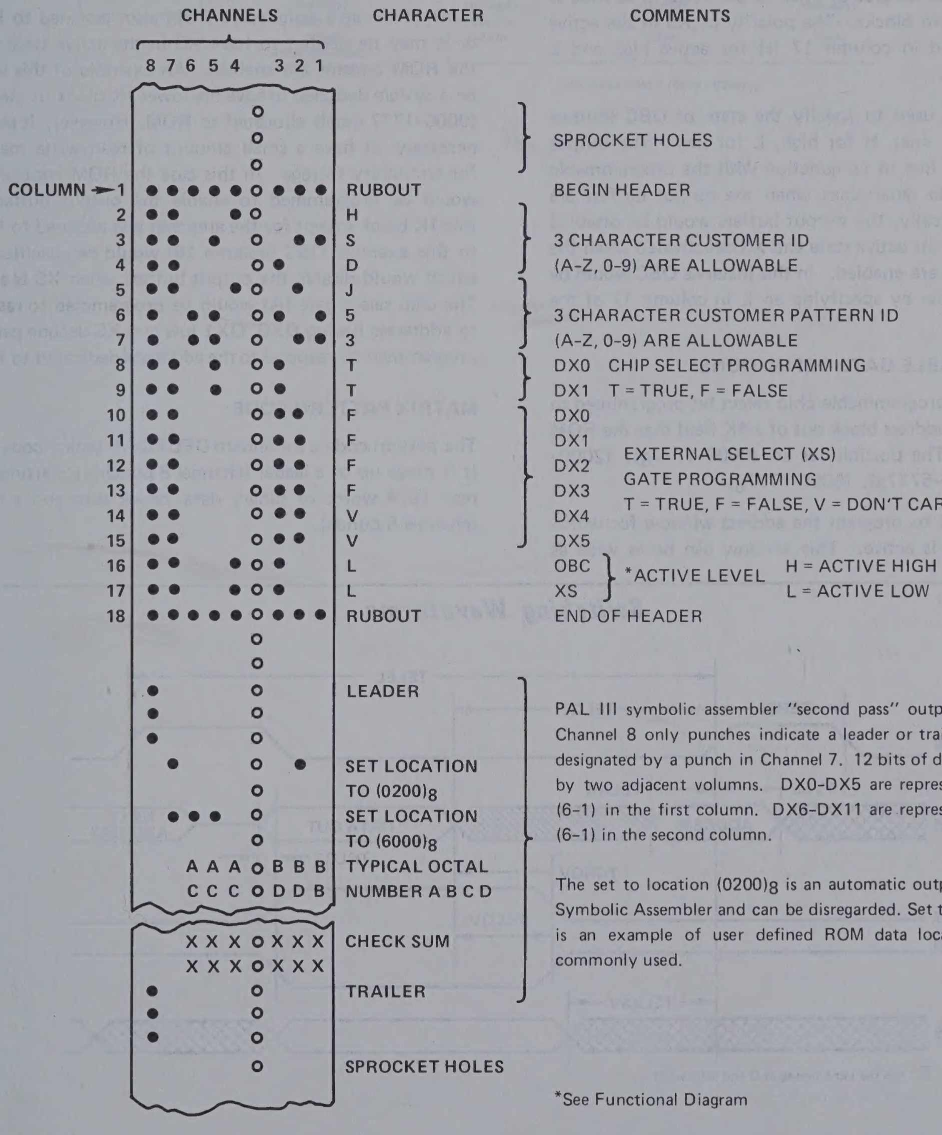
① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 3mA/MHz.

② Capacitance sampled and guaranteed – not 100% tested.

③ A.C. test conditions: Inputs – TRise = TFall = 20ns; Outputs – CLoad = 50pF. All timing measurements at 1.5V reference level.

Custom ROM Programming

HM-6322 programming information is generated from the PAL III Symbolic Assembler, (in conjunction with the DEC PDP/8 Type System) as a "second pass" binary tape. A separate tape is required for each 1024 word ROM pattern. A header is added to the front of each tape giving customer ID, chip select and XS programming information. The header consists of 16 ASCII characters generated from a standard teletype. Channel 8 is always punched. The header begins with a rubout followed by 6 alphanumeric characters identifying the customer and the pattern number. Next are 2 characters designating true or false for inputs DX0 and DX1 to chips select gate A (see Functional Diagram) and 6 characters designating true, false or don't care for inputs DX0, DX1, DX2, DX3, DX4 and DX5 to the RAM select gate B (see Functional Diagram). Next is one character (H or L), designating OBC as active high or active low (column 16). Column 17 is for designating XS as active high or active low (H or L). The header ends with a rubout.


CHANNELS
CHARACTER
COMMENTS
8 7 6 5 4 3 2 1
SPROCKET HOLES
COLUMN → 1
RUBOUT
BEGIN HEADER
2 H
3 S
4 D
3 CHARACTER CUSTOMER ID
(A-Z, 0-9) ARE ALLOWABLE
5 J
6 5
7 3
3 CHARACTER CUSTOMER PATTERN ID
(A-Z, 0-9) ARE ALLOWABLE
8 T
9 T
DX0 CHIP SELECT PROGRAMMING
DX1 T = TRUE, F = FALSE
10 F
11 F
12 F
13 F
14 V
15 V
DX0
DX1
DX2
DX3
DX4
DX5
EXTERNAL SELECT (XS)
GATE PROGRAMMING
T = TRUE, F = FALSE, V = DON'T CARE
16 L
17 L
OBC
XS
*ACTIVE LEVEL
H = ACTIVE HIGH
L = ACTIVE LOW
18 RUBOUT
END OF HEADER
LEADER
SET LOCATION TO (0200)8
SET LOCATION TO (6000)8
A A A B B B
C C C D D B
TYPICAL OCTAL NUMBER A B C D
X X X X X X
X X X X X X
CHECK SUM
TRAILER
SPROCKET HOLES

PAL III symbolic assembler "second pass" output is of this form. Channel 8 only punches indicate a leader or trailer. An address is designated by a punch in Channel 7. 12 bits of data are represented by two adjacent volumns. DX0-DX5 are represented by channels (6-1) in the first column. DX6-DX11 are represented by channels (6-1) in the second column.

The set to location $(0200)_8$ is an automatic output of the PAL III Symbolic Assembler and can be disregarded. Set to location $(6000)_8$ is an example of user defined ROM data location and is most commonly used.

*See Functional Diagram

HEADER BLOCK:

The header block defines the customer and pattern identification code and the ROM control function programming information (columns 2-7). The control functions are chip select programming, external select (XS) active area and polarity, ROM output buffer control (OBC). The chip select programming information provided in column 8 and 9 of the header block addresses the ROM, which responds in 1K blocks (e.g. 0000-1024_{10} - 0000-1777_8).

The external select (XS) active area is defined in columns 10-15, it can be an area as small as 64 words or as wide as 4096 in 64 word blocks. The polarity of XS in the active state is defined in column 17 (H for active high and L for active low).

Column 16 is used to specify the state of OBC (output buffer control line), H for high, L for low. The output buffer control line in conjunction with the programmable chip select gate determines when the output buffers are enabled. Typically, the output buffers would be disabled when XS is in the active state and XS deactivated when the output buffers are enabled. In this instance OBC would be programmed low by specifying an L in column 17 of the header.

PROGRAMMABLE GATE DEFINITIONS:

Gate A is the programmable chip select bit programmed to define the 1K address block out of a 4K field that the ROM responds to. The possibilities are (0000-1777_8); (2000-3777_8); (4000-5777_8); (6000-7777_8).

Gate B is used to program the address window for which external select is active. This window can be as wide as 4096 words or as narrow as 64 words and positioned any where in the 4K field.

Gate C is a programmable inverter used to determine the polarity of XS in the active window.

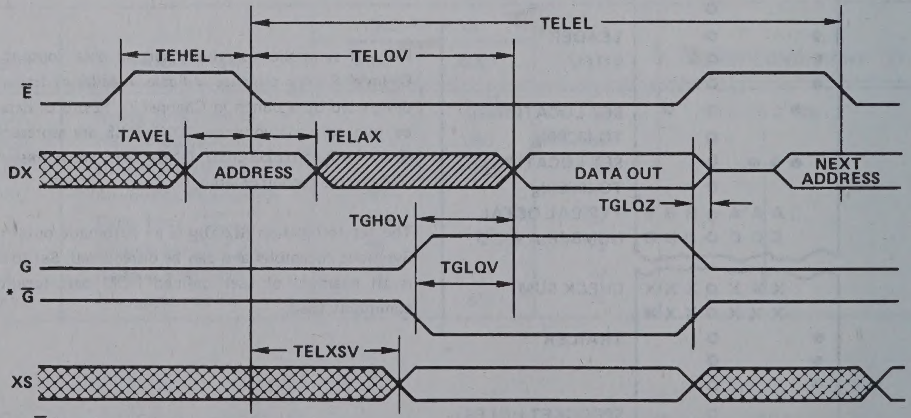
Gate D is a programmable inverter used in combination with Gates A and B to control the output buffer enable line. Gate D is normally programmed as an inverter. This serves to disable Gate A and the ROM output buffers anytime that XS is active.

In special case applications, there may be a need to have some of the area assigned to ROM also assigned to RAM, or it may be desired to have XS in the active state while the ROM outputs are enabled. An example of this would be a system designed to have the lower 1K block of memory (0000-1777 octal) allocated to ROM. However, it may be necessary to have a small amount of read-write memory for temporary storage. In this case the ROM control logic would be programmed to enable the output buffers for this 1K block except for the area that was assigned to RAM. In this example OBC (column 16) would be specified low which would disable the output buffers when XS is active. The chip select gate (A) would be programmed to respond to addresses having DX0, DX1 low and XS decode gate (B) programmed to respond to the addresses dedicated to RAM.

MATRIX PATTERN CODE:

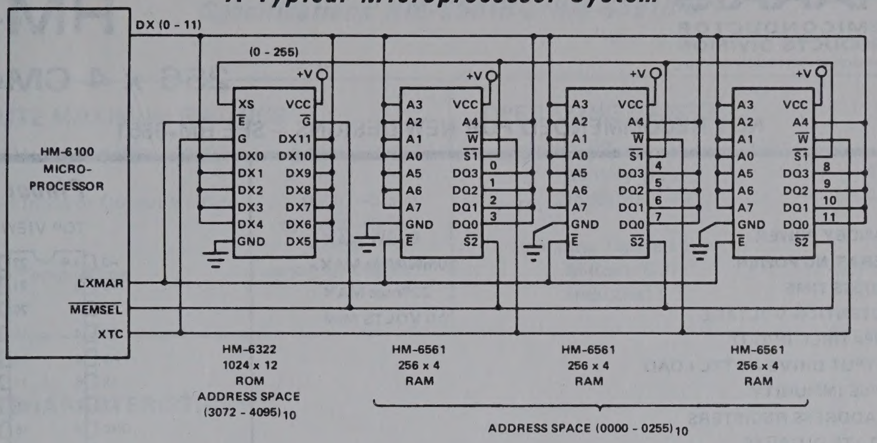
The pattern code is a standard DEC PDP/8 binary code tape. It is made up of a leader (channel 8 punch), a starting address, 1024 words of binary data, check sum and a trailer (channel 8 punch).

Switching Waveforms



G̅ * has the same timing as G and is inverted

A Typical Microprocessor System


DX (0 - 11)
(0 - 255)
+V
HM-6100 MICRO-PROCESSOR
LXMAR
MEMSEL
XTC
XS
E
G
DX0
DX1
DX2
DX3
DX4
GND
VCC
G
DX11
DX10
DX9
DX8
DX7
DX6
DX5
A3
A2
A1
A0
A5
A6
A7
GND
E
VCC
A4
W
S1
DQ3
DQ2
DQ1
DQ0
S2
0
1
2
3
4
5
6
7
8
9
10
11
HM-6322 1024 x 12 ROM ADDRESS SPACE (3072 - 4095)10
HM-6561 256 x 4 RAM
HM-6561 256 x 4 RAM
HM-6561 256 x 4 RAM
ADDRESS SPACE (0000 - 0255)10

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6501
256 x 4 CMOS RAM

NOT RECOMMENDED FOR NEW DESIGNS – SEE HM-6551

Features

• LOW STANDBY POWER	50µW MAX
• LOW OPERATING POWER	20mW/MHz MAX
• FAST ACCESS TIME	220nsec MAX
• DATA RETENTION VOLTAGE	2.0 VOLTS MIN
• TTL COMPATIBLE IN/OUT	
• HIGH OUTPUT DRIVE - 1 TTL LOAD	
• HIGH NOISE IMMUNITY	
• ON CHIP ADDRESS REGISTERS	
• THREE STATE OUTPUTS	
• EASY MICROPROCESSOR INTERFACING	
• LATCHED OUTPUTS	
• MILITARY AND INDUSTRIAL TEMPERATURE RANGES	

Description

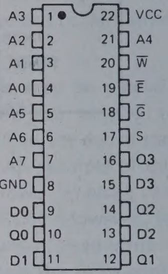
The HM-6501 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6501 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

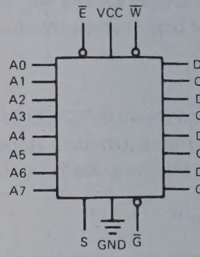
Pinout

TOP VIEW

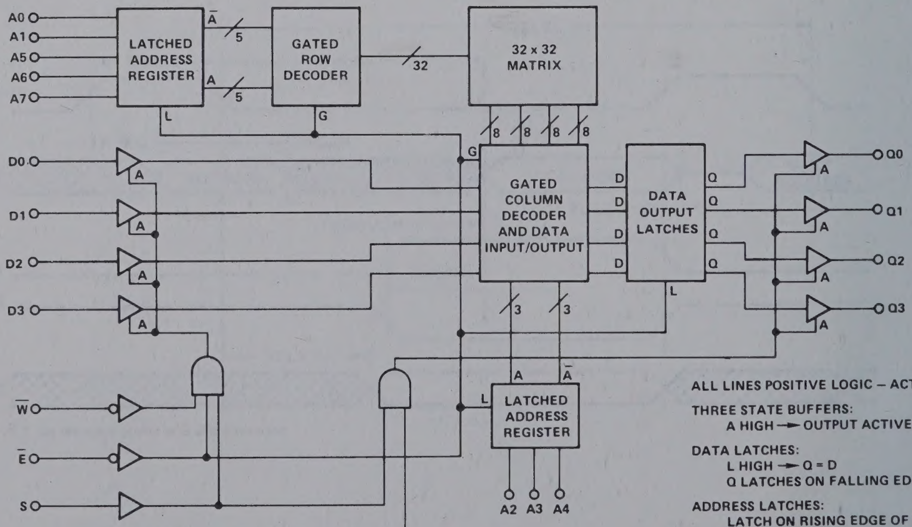

A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
D0 9
Q0 10
D1 11
22 VCC
21 A4
20 $\overline{W}$
19 $\overline{E}$
18 $\overline{G}$
17 S
16 Q3
15 D3
14 Q2
13 D2
12 Q1

A - ADDRESS INPUT
$\overline{E}$ - CHIP ENABLE
$\overline{W}$ - WRITE ENABLE
$\overline{G}$ - OUTPUT ENABLE
S - CHIP SELECT
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol


$\overline{E}$
VCC
$\overline{W}$
A0
A1
A2
A3
A4
A5
A6
A7
D0
Q0
D1
Q1
D2
Q2
D3
Q3
S
GND
$\overline{G}$

Functional Diagram


A0
A1
A5
A6
A7
LATCHED ADDRESS REGISTER
A
5
A
5
GATED ROW DECODER
32
32 x 32 MATRIX
L
G
8
8
8
8
G
GATED COLUMN DECODER AND DATA INPUT/OUTPUT
D
D
D
D
DATA OUTPUT LATCHES
Q
Q
Q
Q
L
Q0
Q1
Q2
Q3
D0
D1
D2
D3
A
A
A
A
3
3
A
$\overline{A}$
L
LATCHED ADDRESS REGISTER
A2
A3
A4
$\overline{W}$
$\overline{E}$
S
$\overline{G}$

ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6501B-2/HM-6501B-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IOH = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TSHQX	Chip Select Output Enable Time	20	130	50	ns	④
	TGLQX	Output Enable Output Enable Time	20	130	50	ns	④
	TSLQZ	Chip Select Output Disable Time		130	50	ns	④
	TGHQZ	Output Enable Output Disable Time		130	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		-10	ns	④
	TWLSL	Chip Select Write Pulse Setup Time	120		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
	TSHWH	Chip Select Write Pulse Hold Time	120		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
	TWLWH	Write Enable Pulse Width	120		60	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6501-2/HM-6501-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - Gnd)	-0.3V to +8.0V
Applied Input or Output Voltage	(Gnd -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IOH = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		300	150	ns	④
	TSHQX	Chip Select Output Enable Time	20	150	60	ns	④
	TGLQX	Output Enable Output Enable Time	20	150	60	ns	④
	TSLQZ	Chip Select Output Disable Time		150	60	ns	④
	TGHQZ	Output Enable Output Disable Time		150	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	150		100	ns	④
	TWHDX	Data Hold Time	0		-10	ns	④
	TWLSL	Chip Select Write Pulse Setup Time	180		120	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		120	ns	④
	TSHWH	Chip Select Write Pulse Hold Time	180		120	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		120	ns	④
	TWLWH	Write Enable Pulse Width	180		120	ns	④
	TELEL	Read or Write Cycle Time	400		210	ns	④

NOTES:

1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6501-5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

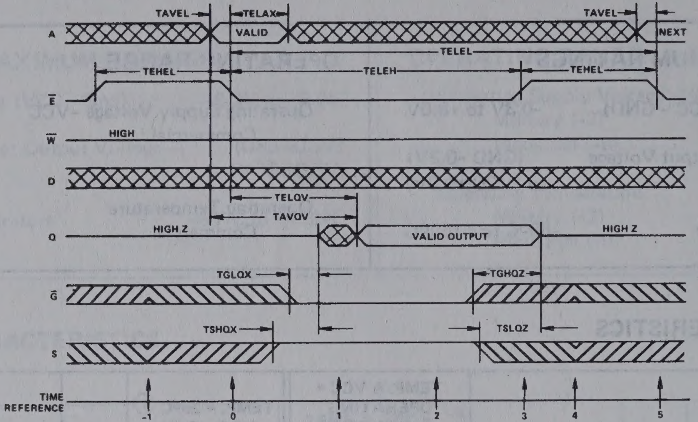
Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		100	1.0	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IOH = -0.2mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		360	200	ns	④
	TSHQX	Chip Select Output Enable Time	20	180	80	ns	④
	TGLQX	Output Enable Output Enable Time	20	180	80	ns	④
	TSLQZ	Chip Select Output Disable Time		180	80	ns	④
	TGHQZ	Output Enable Output Disable Time		180	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TELAX	Address Hold Time	70		40	ns	④
	TDVWH	Data Setup Time	170		120	ns	④
	TWHDX	Data Hold Time	0		-10	ns	④
	TWLSL	Chip Select Write Pulse Setup Time	210		150	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		150	ns	④
	TSHWH	Chip Select Write Pulse Hold Time	210		150	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		150	ns	④
	TWLWH	Write Enable Pulse Width	210		150	ns	④
	TELEL	Read or Write Cycle Time	500		290	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle


TAVEL
TELAX
TAVEL
A
VALID
NEXT
TELEL
TEHEL
TELEH
TEHEL
$\overline{E}$
$\overline{W}$
HIGH
D
TELQV
TAVQV
Q
HIGH Z
VALID OUTPUT
HIGH Z
TGLQX
TGHQZ
$\overline{G}$
TSHQX
TSLQZ
S
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

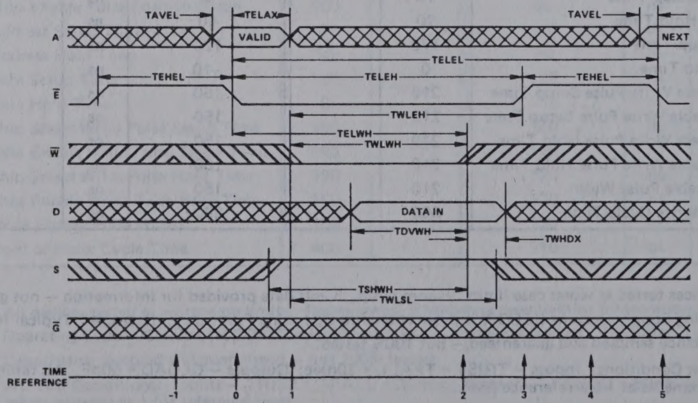
TIME REFERENCE	INPUTS $\overline{E}$	S	$\overline{G}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	L	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	H	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	H	X	X	X	OUTPUT ENABLED
2	L	H	L	H	X	X	V	OUTPUT VALID
3	↗	H	L	H	X	X	V	OUTPUT LATCHED
4	H	L	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	L	H	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, $\overline{G}$ and $\overline{E}$ must be low; $\overline{W}$ and S must be high. The output data will be valid at accesss time (TELQV) or at one output enable time (TSHQX or TGLQX), whichever is the latter occuring signal.

S and $\overline{G}$ are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when or-tying several memories in an array.

The HM-6501 has output data latches that are controlled by $\overline{E}$. When $\overline{E}$ goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either $\overline{G}$ or S but the latches will only unlatch on the falling edge of $\overline{E}$.

Write Cycle


TAVEL
TELAX
TAVEL
A
VALID
NEXT
TELEL
TEHEL
TELEH
TEHEL
$\overline{E}$
TWLEH
TELWH
TWLWH
$\overline{W}$
D
DATA IN
TDVWH
TWHDX
S
TSHWH
TWLSL
$\overline{G}$
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	S	$\overline{G}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	L	X	X	X	X	SEE NOTE	MEMORY DISABLED
0	↓	X	X	X	V	X		CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	↓	X	X		WRITE PERIOD BEGINS
2	L	H	X	↑	X	V		DATA IN IS WRITTEN
3	↑	X	X	H	X	X		WRITE IS COMPLETED
4	H	L	X	X	X	X		PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	X	X	V	X		CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTE: IF $\overline{G}$ IS HIGH, THE OUTPUT WILL BE HIGH IMPEDANCE.
IF $\overline{G}$ IS LOW, THE INPUT DATA WILL PROPAGATE TO THE OUTPUT.

As in the read mode, the write cycle is initiated by the falling edge of $\overline{E}$ which latches the addresses. The write portion of the cycle is defined as $\overline{E}$ and $\overline{W}$ being low simultaneously with S high. If the inputs and outputs are tied together, $\overline{G}$ must be high. The write portion of the cycle is terminated on the first rising edge of $\overline{E}$, $\overline{W}$, or the falling edge of S. Data setup and hold times must be referenced to the terminating signal. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$ or to the falling edge of S, whichever occurs first.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH) various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSHQX or TGLQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

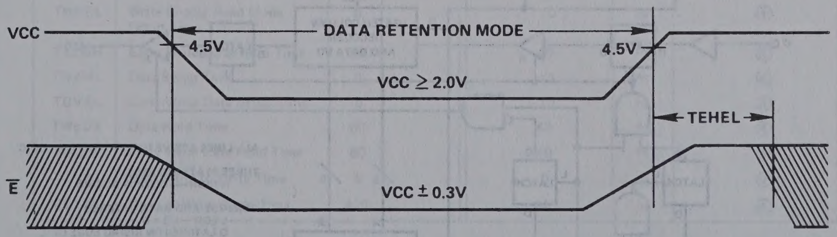
The data inputs and data outputs may be tied together for use with a common I/O bus structure if the system control line G ($\overline{G}$ NOT) is NAND-ed with $\overline{W}$ to produce the device $\overline{G}$ signal. This will force the output buffers to a high impedance state during write operations so input data can be applied to the bus. A minimum delay of one output disable time must be allowed before applying input data to the bus. This will insure that the output buffers are not active.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HM-6503
2048 x 1 CMOS RAM

Features

- LOW POWER STANDBY 250μW MAX.
- LOW POWER OPERATION 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION @ 2.0V MIN.
- TTL COMPATIBILITY INPUT/OUTPUT
- THREE STATE OUTPUT
- FAST ACCESS TIME 300nsec MAX.
- INDUSTRIAL OR COMMERCIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- PINOUT ALLOWS UPGRADE TO 6504

Description

The HM-6503 is a 2048 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

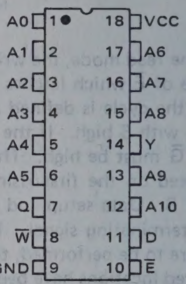
On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6503 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

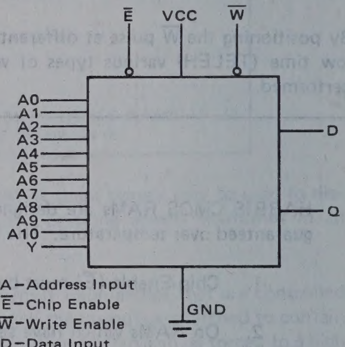
The HM-6503 is supplied in two versions, the HM-6503H and the HM-6503L. The H or L is used to designate the logic level to be connected to the Y input. If a HM-6503H is procured the user must connect the Y input to VCC in the system. If a HM-6503L is used the Y input must be connected to system ground.

Pinout

TOP VIEW

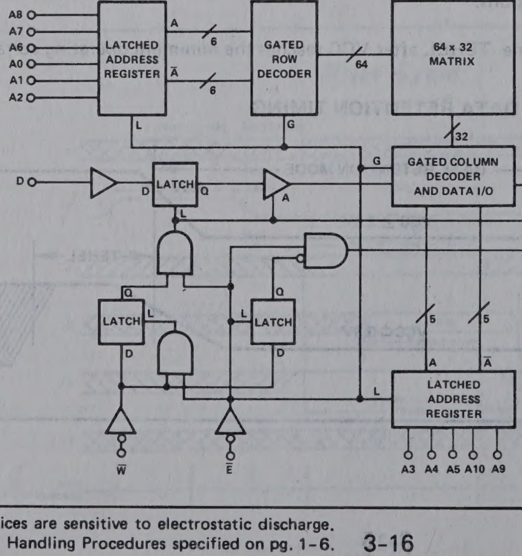

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
Q 7
$\overline{W}$ 8
GND 9
18 VCC
17 A6
16 A7
15 A8
14 Y
13 A9
12 A10
11 D
10 $\overline{E}$

Logic Symbol


$\overline{E}$
VCC
$\overline{W}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
Y
D
Q
GND

A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
D – Data Input
Q – Data Output
Y – Hard Wired Input

Functional Diagram


A8
A7
A6
A0
A1
A2
LATCHED ADDRESS REGISTER
A
$\overline{A}$
6
6
L
GATED ROW DECODER
G
64
64 x 32 MATRIX
32
D
LATCH
D
Q
L
A
G
GATED COLUMN DECODER AND DATA I/O
LATCH
D
Q
L
A
Q
Q
LATCH
L
D
Q
L
LATCH
D
5
5
A
$\overline{A}$
L
LATCHED ADDRESS REGISTER
$\overline{W}$
$\overline{E}$
A3
A4
A5
A10
A9

ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

CONTROL AND DATA LATCHES:
L LOW → Q = D
Q LATCHES ON RISING EDGE OF L

ADDRESS LATCHES:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6503-9

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Industrial (-9)	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V		
	SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	170	ns	④
	TAVQV	Address Access Time		320	170	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	80		40	ns	④
	TWLEH	Write Enable Pulse Setup Time	200		130	ns	④
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		-10	ns	④
	TELWH	Early Write Pulse Hold Time	80		40	ns	④
	TDVWL	Data Setup Time	0		-10	ns	④
	TDVEL	Early Write Data Setup Time	0		-10	ns	④
	TWLDX	Data Hold Time	80		40	ns	④
	TELDX	Early Write Data Hold Time	80		40	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TELEL	Read or Write Cycle Time	420		240	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

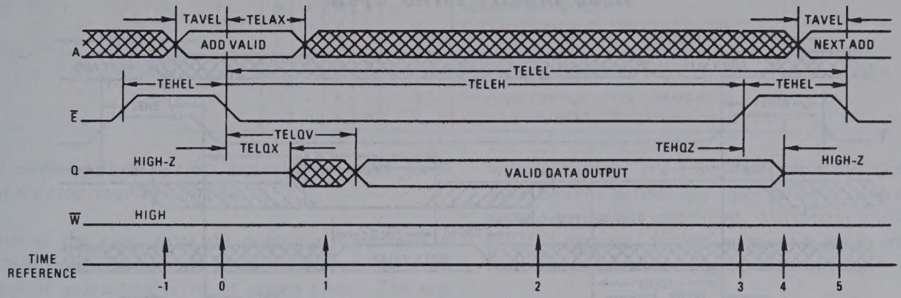
ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage – (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)	Operating Temperature Commercial	0°C to +75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		500	50	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Curr		500	10	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Volt.	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance ③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	pF	f = 1MHz VO=VCC or GND
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		370	200	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	100		60	ns	④
	TWLEH	Write Enable Pulse Setup Time	250		100	ns	④
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	④
	TWHEL	Write Enable Read Setup Time	0		-10	ns	④
	TELWH	Early Write Pulse Hold Time	100		60	ns	④
	TDVWL	Data Setup Time	30		0	ns	④
	TDVEL	Early Write Data Setup Time	30		0	ns	④
	TWLDX	Data Hold Time	100		60	ns	④
	TELDX	Early Write Data Hold Time	100		80	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TELEL	Read or Write Cycle Time	500		300	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle

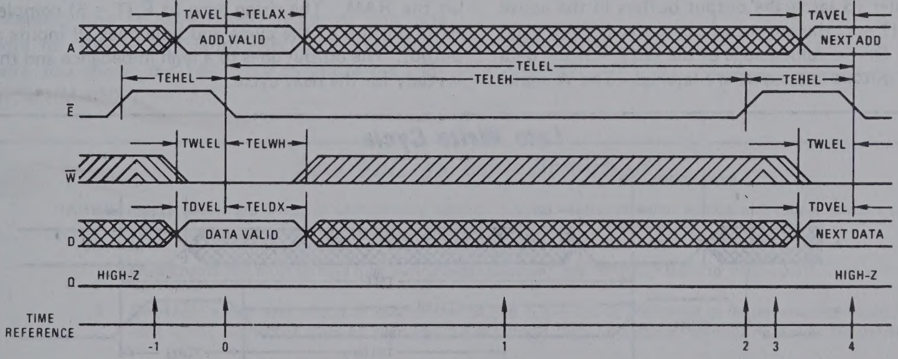

TAVEL
TELAX
TAVEL
A
ADD VALID
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
E
TELQV
TELQX
TEHQZ
HIGH-Z
HIGH-Z
Q
VALID DATA OUTPUT
W
HIGH
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↑	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

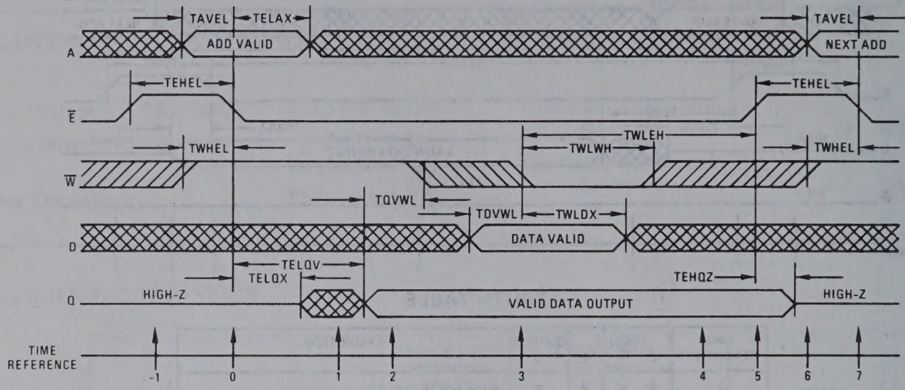

TAVEL
TELAX
TAVEL
A
ADD VALID
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
E
TWLEL
TELWH
TWLEL
W
TDVEL
TELDX
TDVEL
D
DATA VALID
NEXT DATA
Q
HIGH-Z
HIGH-Z
TIME REFERENCE
-1
0
1
2
3
4

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↑	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↓	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low in the early write cycle the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle

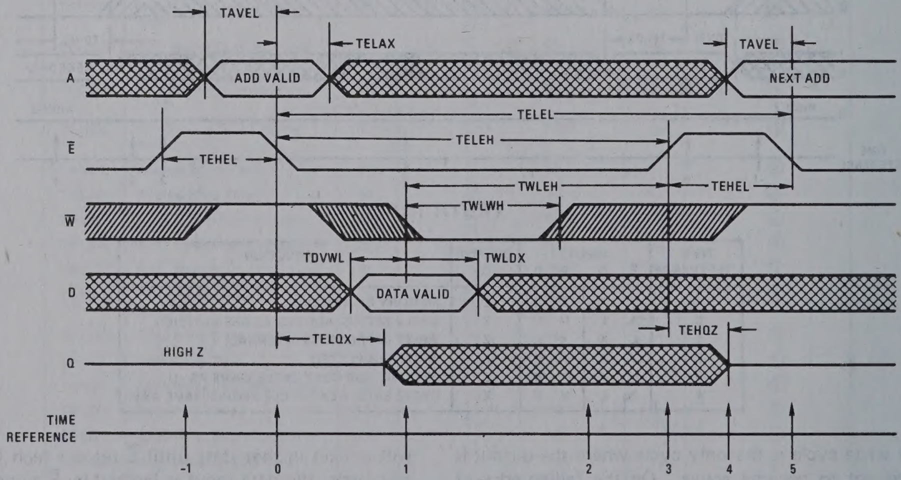

TAVEL
TELAX
ADD VALID
TAVEL
NEXT ADD
A
TEHEL
TEHEL
E
TWLEH
TWLWH
TWHEL
TWHEL
W
TQVWL
TDVWL
TWLDX
DATA VALID
D
TELQV
TELQX
TEHQZ
HIGH-Z
VALID DATA OUTPUT
HIGH-Z
Q
TIME REFERENCE
-1
0
1
2
3
4
5
6
7

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↓	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↑	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↓	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T = 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle


TAVEL
TELAX
ADD VALID
TAVEL
NEXT ADD
A
TELEL
TELEH
TEHEL
E
TWLEH
TEHEL
TWLWH
W
TDVWL
TWLDX
DATA VALID
D
TEHQZ
TELQX
HIGH Z
Q
TIME REFERENCE
-1
0
1
2
3
4
5

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↓	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↑	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

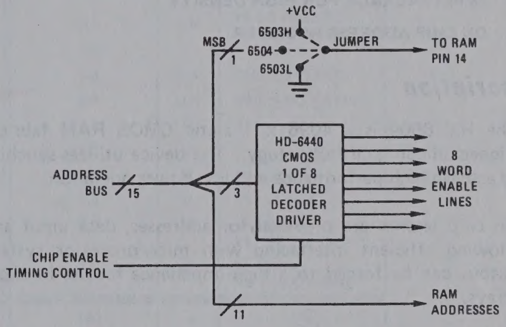
Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

NOTES:

In the above descriptions the numbers in parenthesis (T = X) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Suggestions For 6503 Memory Array Design

The HM-6503 is a device that can be used to good advantage in systems which are offered with choices of memory array size. With one common memory board layout the designer can easily offer two different array sizes. This is accomplished by using the conveniently similiar pinouts of the HM-6503 (2K by 1) and the HM-6504 (4K by 1). For example, a 16K word by 8 bit array using HM-6503s and a 32K word by 8 bit array using HM-6504s can be easily implemented on the same printed circuit card. The circuit diagram suggests one implementation requiring only one jumper wire for 16K or 32K word selection. This single jumper wire also allows the 16K array to utilize the HM-6503H or the HM-6503L version.

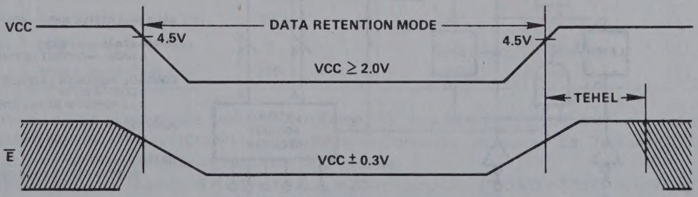


Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6504

4096 x 1 CMOS RAM

Features

- LOW POWER STANDBY 250μW MAX.
- LOW POWER OPERATION 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- THREE-STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME 200nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Description

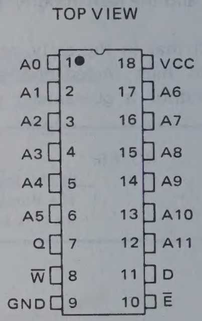
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

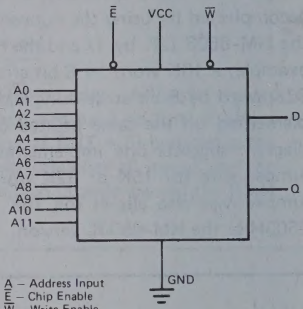
The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

Pinout

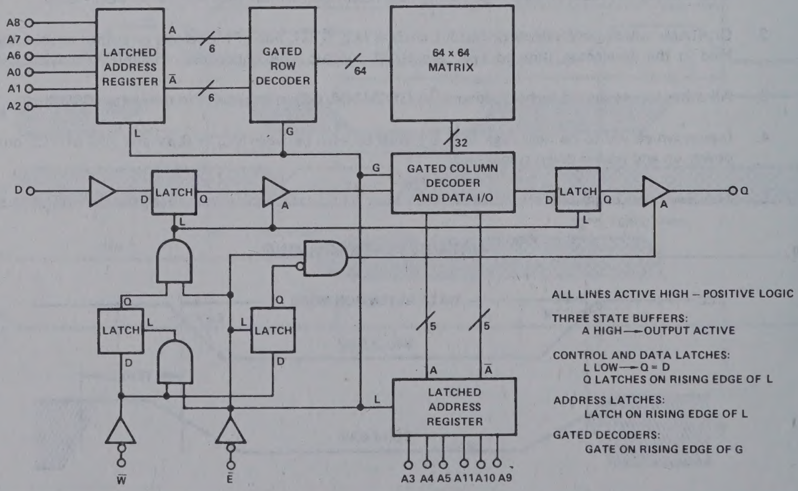

TOP VIEW
A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
Q 7
$\overline{W}$ 8
GND 9
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 D
10 $\overline{E}$

Logic Symbol


$\overline{E}$
VCC
$\overline{W}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
D
Q
GND

A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
D – Data Input
Q – Data Output

Functional Diagram


A8
A7
A6
A0
A1
A2
LATCHED ADDRESS REGISTER
A
$\overline{A}$
6
6
L
GATED ROW DECODER
G
64
64 x 64 MATRIX
32
GATED COLUMN DECODER AND DATA I/O
G
D
LATCH
D
Q
L
A
LATCH
D
Q
L
A
Q
LATCH
Q
L
D
LATCH
Q
L
D
5
5
A
$\overline{A}$
L
LATCHED ADDRESS REGISTER
A3 A4 A5 A11 A10 A9
$\overline{W}$
$\overline{E}$

ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

CONTROL AND DATA LATCHES:
L LOW → Q = D
Q LATCHES ON RISING EDGE OF L

ADDRESS LATCHES:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	IO = 0 VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200	150	ns	④
	TAVQV	Address Access Time		220	150	ns	④
	TELQX	Chip Enable Output Enable Time	20	80	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		80	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	200		150	ns	④
	TEHEL	Chip Enable Pulse Positive Width	90		60	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	60		40	ns	④
	TWLEH	Write Enable Pulse Setup Time	150		100	ns	④
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		-10	ns	④
	TELWH	Early Write Pulse Hold Time	60		40	ns	④
	TDVWL	Data Setup Time	0		0	ns	④
	TDVEL	Early Write Data Setup Time	0		0	ns	④
	TWLDX	Data Hold Time	60		40	ns	④
	TELDX	Early Write Data Hold Time	60		40	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TELEL	Read or Write Cycle Time	290		210	ns	④

NOTES:
① All devices tested at worst case limits. Room Temp., 5V data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC test conditions: Inputs — TRISE = TFALL = 20ns; Output — CLOAD = 50pF. All timing measured at 1.5V reference level.

3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP = 25°C① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	IO = 0, VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	170	ns	④
	TAVQV	Address Access Time		320	170	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	80		40	ns	④
	TWLEH	Write Enable Pulse Setup Time	200		130	ns	④
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		-10	ns	④
	TELWH	Early Write Pulse Hold Time	80		40	ns	④
	TDVWL	Data Setup Time	0		0	ns	④
	TDVEL	Early Write Data Setup Time	0		0	ns	④
	TWLDX	Data Hold Time	80		40	ns	④
	TELDX	Early Write Data Hold Time	80		40	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TELEL	Read or Write Cycle Time	420		240	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6504C-9

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP = 25°C① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		50	25	μA	IO = 0 VCC = 2.0V VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	170	ns	④
	TAVQV	Address Access Time		320	170	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	80		40	ns	④
	TWLEH	Write Enable Pulse Setup Time	200		130	ns	④
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		-10	ns	④
	TELWH	Early Write Pulse Hold Time	80		40	ns	④
	TDVWL	Data Setup Time	0		0	ns	④
	TDVEL	Early Write Data Setup Time	0		0	ns	④
	TWLDX	Data Hold Time	80		40	ns	④
	TELDX	Early Write Data Hold Time	80		40	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TELEL	Read or Write Cycle Time	420		240	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6504-5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

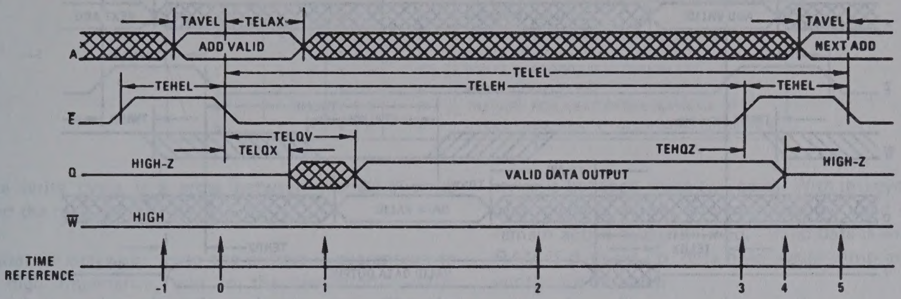
Operating Supply Voltage Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		500	50	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	10	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance ③		8.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		370	200	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	100		60	ns	④
	TWLEH	Write Enable Pulse Setup Time	250		100	ns	④
	TWLEL	Early Write Pulse Setup Time	0		-10	ns	④
	TWHEL	Write Enable Read Setup Time	0		-10	ns	④
	TELWH	Early Write Pulse Hold Time	100		60	ns	④
	TDVWL	Data Setup Time	30		0	ns	④
	TDVEL	Early Write Data Setup Time	30		0	ns	④
	TWLDX	Data Hold Time	100		60	ns	④
	TELDX	Early Write Data Hold Time	100		80	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TELEL	Read or Write Cycle Time	500		300	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle

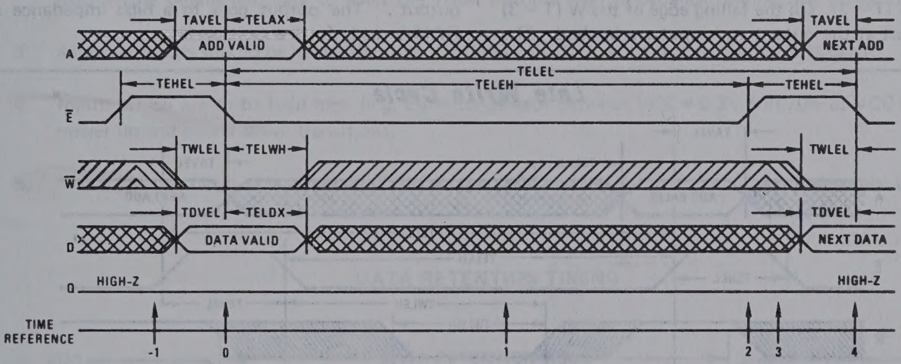

A
TAVEL
TELAX
ADD VALID
TAVEL
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
Ē
TELQV
TELQX
TEHQZ
Q
HIGH-Z
VALID DATA OUTPUT
HIGH-Z
W̄
HIGH
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS Ē	INPUTS W̄	INPUTS A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

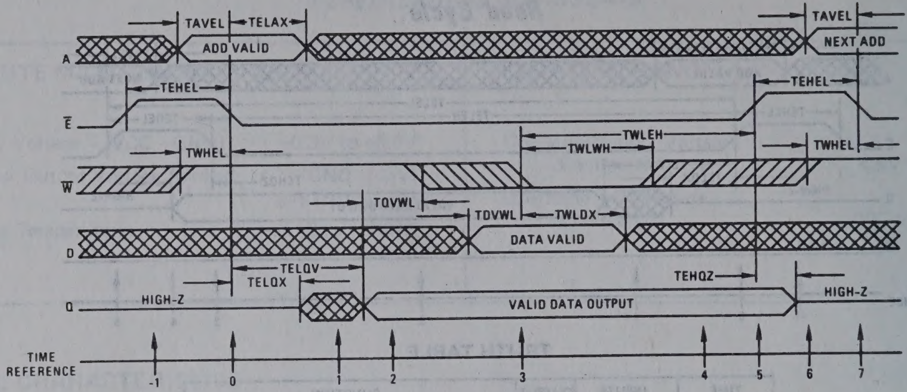

A
TAVEL
TELAX
ADD VALID
TAVEL
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
Ē
TWLEL
TELWH
TWLEL
W̄
TDVEL
TELDX
TDVEL
D
DATA VALID
NEXT DATA
Q
HIGH-Z
HIGH-Z
TIME REFERENCE
-1
0
1
2
3
4

TRUTH TABLE

TIME REFERENCE	INPUTS Ē	INPUTS W̄	INPUTS A	INPUTS D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle

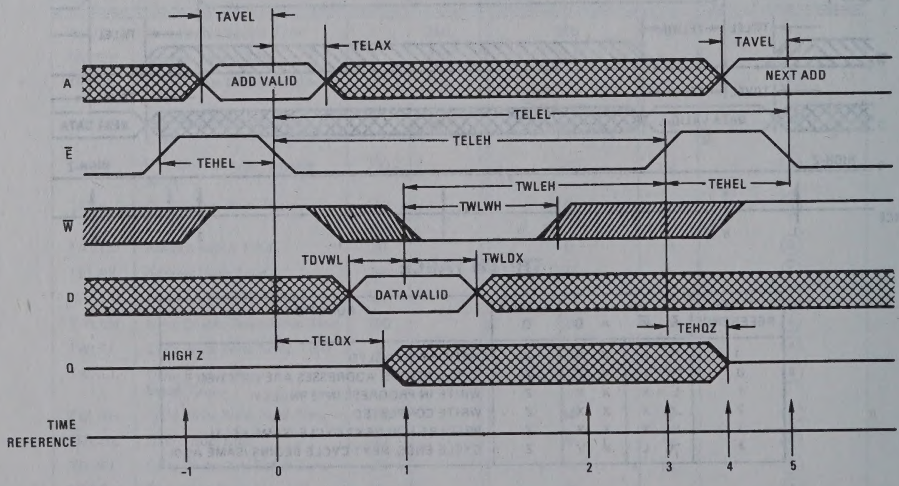

TAVEL
TELAX
ADD VALID
TAVEL
NEXT ADD
A
TEHEL
TEHEL
E
TWLEH
TWLWH
TWHEL
TWHEL
W
TQVWL
TDVWL
TWLDX
DATA VALID
D
TELQV
TELQX
TEHQZ
HIGH-Z
HIGH-Z
VALID DATA OUTPUT
Q
TIME REFERENCE
-1
0
1
2
3
4
5
6
7

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T= 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and output . The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle


TAVEL
TELAX
TAVEL
A
ADD VALID
NEXT ADD
TELEL
TELEH
E
TEHEL
TWLEH
TEHEL
TWLWH
W
TDVWL
TWLDX
D
DATA VALID
TEHQZ
TELQX
HIGH Z
Q
TIME REFERENCE
-1
0
1
2
3
4
5

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↗	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

NOTES:

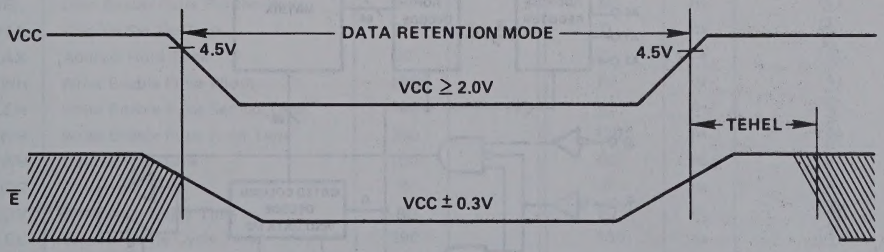
In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6505
4096 x 1 CMOS RAM

Advance Information

Features

LOW POWER STANDBY	250μW MAX.
LOW POWER OPERATION	35mW/MHz MAX.
FAST ACCESS TIME	200ns MAX.
DATA RETENTION	@ 2.0V MIN.

- EXTREMELY LOW SPEED POWER PRODUCT
- TTL COMPATIBLE INPUT/OUTPUT
- EASY MICROPROCESSOR INTERFACING
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES
- 18 PIN PACKAGE FOR HIGH DENSITY

Description

The HM-6505 is a 4096 x 1 CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

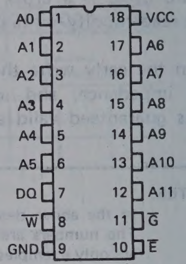
On chip address latches are provided to allow efficient interfacing with microprocessor systems. The common data in/out can be forced to a high impedance state for use in expanded memory arrays.

The HM-6505 is a fully static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current specifications are guaranteed over temperature.

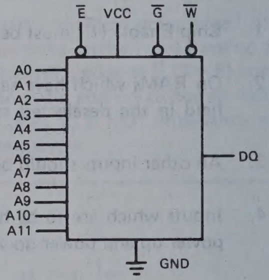
Pinout

TOP VIEW

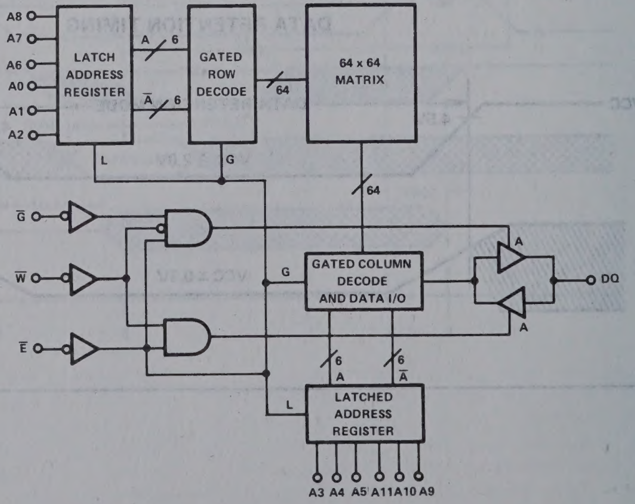

A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
DQ 7
$\overline{W}$ 8
GND 9
18 VCC
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 $\overline{G}$
10 $\overline{E}$

A Address Input
DQ Data In/Out
$\overline{E}$ Chip Enable
$\overline{W}$ Write Enable
$\overline{G}$ Output Enable

Logic Symbol


$\overline{E}$
VCC
$\overline{G}$
$\overline{W}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQ
GND

Functional Diagram


A8
A7
A6
A0
A1
A2
LATCH ADDRESS REGISTER
A 6
$\overline{A}$ 6
GATED ROW DECODE
64
64 x 64 MATRIX
L
G
64
$\overline{G}$
$\overline{W}$
$\overline{E}$
G
GATED COLUMN DECODE AND DATA I/O
A
A
DQ
6 A
6 $\overline{A}$
L
LATCHED ADDRESS REGISTER
A3 A4 A5 A11 A10 A9

ALL LINES ACTIVE HIGH –
POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6505B-2/HM-6505B-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3 to 8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to 150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP & VCC = OPERATING RANGE		① TEMP = 25°C VCC = 5.0V		
	SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.5	μA	IO = 0, VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200	130	ns	④
	TAVQV	Address Access Time		220	130	ns	④
	TELQX	Chip Enable Output Enable Time	20	80	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		80	50	ns	④
	TGLQV	Output Enable Output Enable Time	20	80	50	ns	④
	TGHQZ	Output Enable Output Disable Time		80	50	ns	④
	TWLQZ	Write Enable Output Disable Time		80	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	200		130	ns	④
	TEHEL	Chip Enable Pulse Positive Width	90		50	ns	④
	TAVEL	Address Set Up Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	100		60	ns	④
	TWLEH	Write Enable Pulse Set Up Time	100		60	ns	④
	TELWH	Write Enable Pulse Hold Time	200		130	ns	④
	TDVWH	Data Set Up Time	100		60	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	80		50	ns	④
	TELEL	Read or Write Cycle Time	290		180	ns	④

NOTES:

① All devices tested at worst case limits. Room temp., 5 volt data provided for information–not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.

③ Capacitance sampled and guaranteed–not 100% tested.

④ AC test conditions: Inputs–TRISE = TFALL = 20nsec; Output–C load = 50pF. All timing measured at 1.5V reference level.

Specifications HM-6505-2/HM-6505-9

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage (VCC - GND)	-0.3 to 8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to 150°C

OPERATING RANGE	
Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	TEMP & VCC = OPERATING RANGE MAX	① TEMP = 25°C VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.5	µA	IO = 0, VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND≤VIO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	170	ns	④
	TAVQV	Address Access Time		320	170	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TGLQV	Output Enable Output Enable Time	20	100	50	ns	④
	TGHQZ	Output Enable Output Disable Time		100	50	ns	④
	TWLQZ	Write Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	④
	TAVEL	Address Set Up Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	120		80	ns	④
	TWLEH	Write Enable Pulse Set Up Time	120		80	ns	④
	TELWH	Write Enable Pulse Hold Time	300		160	ns	④
	TDVWH	Data Set Up Time	120		80	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TELEL	Read or Write Cycle Time	420		240	ns	④

NOTES:

① All devices tested at worst case limits. Room temp., 5 volt data provided for information–not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.

③ Capacitance sampled and guaranteed–not 100% tested.

④ AC test conditions: Inputs–TRISE = TFALL = 20nsec; Output–C load = 50pF. All timing measured at 1.5V reference level.

Specifications HM-6505-5

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to +75°C

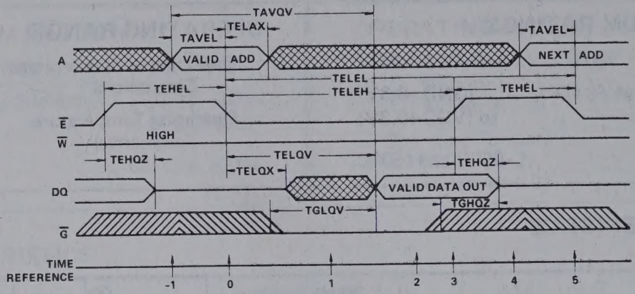
ELECTRICAL CHARACTERISTICS

			TEMP & VCC = OPERATING RANGE		① TEMP = 25°C VCC = 5.0V		
	SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	100	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	10	µA	IO = 0, VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	± 0.5	µA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	± 0.5	µA	GND≤VIO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.25	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		370	200	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TGLQV	Output Enable Output Enable Time	20	100	50	ns	④
	TGHQZ	Output Enable Output Disable Time		100	50	ns	④
	TWLQZ	Write Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	④
	TAVEL	Address Set Up Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	150		100	ns	④
	TWLEH	Write Enable Pulse Set Up Time	150		100	ns	④
	TELWH	Write Enable Pulse Hold Time	350		180	ns	④
	TDVWH	Data Set Up Time	150		100	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TELEL	Read or Write Cycle Time	500		320	ns	④

NOTES:

① All devices tested at worst case limits. Room temp., 5 volt data provided for information-not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed—not 100% tested.
④ AC test conditions: Inputs—TRISE = TFALL = 20nsec; Output—C load = 50pF. All timing measured at 1.5V reference level.

Read Cycle

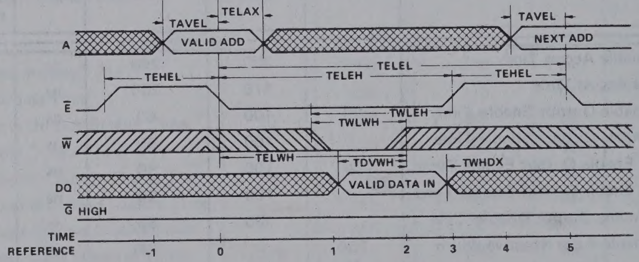

TAVQV
TELAX
TAVEL
TAVEL
A
VALID ADD
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
E
W
HIGH
TEHQZ
TELQV
TELQX
TEHQZ
DQ
VALID DATA OUT
TGLQV
TGHQZ
G
TIME
REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS					FUNCTION
	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	OUTPUT ENABLED
2	L	H	L	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers by the falling edge of $\overline{E}$ (T = 0), minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle

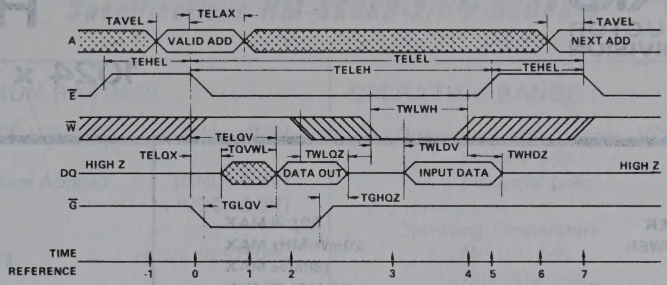

TELAX
TAVEL
TAVEL
A
VALID ADD
NEXT ADD
TEHEL
TELEL
TELEH
TEHEL
E
TWLEH
TWLWH
W
TELWH
TDVWH
TWHDX
DQ
VALID DATA IN
G HIGH
TIME
REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS					FUNCTION
	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	
-1	H	X	H	X	X	MEMORY DISABLED
0	↘	X	H	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	DATA IN IS WRITTEN
3	↗	H	H	X	X	WRITE COMPLETED
4	H	X	H	X	X	PREPARE FOR NEXT CYCLE (SAME AS-1)
5	↘	X	H	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE.	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DATA I/O DQ	FUNCTION
–1	H	X	H	X	Z	MEMORY DISABLED
0	↘	H	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	READ MODE, OUTPUT ENABLED ($\overline{W}$ = HIGH, $\overline{G}$ = LOW)
2	L	H	L	X	V	READ MODE, OUTPUT VALID
3	L	L	H	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	H	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	H	X	Z	WRITE COMPLETED
6	H	X	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS –1)
7	↘	H	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$, a combination read write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the output will become active during time (T = 1) provided $\overline{G}$ is low. Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minimum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffer and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

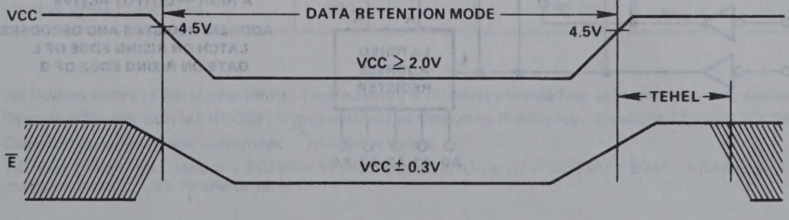
In the above descriptions, the numbers in parentheses (T=n), refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR PRODUCTS DIVISION

HM-6508

1024 x 1 CMOS RAM

Features

- LOW STANDBY POWER	50 μW MAX
- LOW OPERATING POWER	20mW/MHz MAX
- FAST ACCESS TIME	180nsec MAX
- DATA RETENTION VOLTAGE	2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT	
- HIGH OUTPUT DRIVE – 2 TTL LOADS	
- HIGH NOISE IMMUNITY	
- ON CHIP ADDRESS REGISTER	
- MILITARY TEMPERATURE RANGE	
- INDUSTRIAL TEMPERATURE RANGE	
- THREE-STATE OUTPUTS	
- 16 PIN PACKAGE FOR HIGH DENSITY	

Description

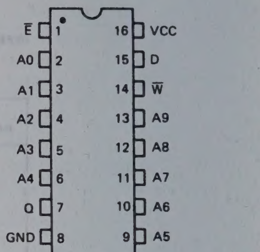
The HM-6508 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Pinout

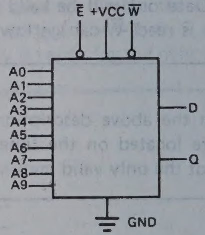
TOP VIEW



Ē 1
A0 2
A1 3
A2 4
A3 5
A4 6
Q 7
GND 8
16 VCC
15 D
14 W̄
13 A9
12 A8
11 A7
10 A6
9 A5

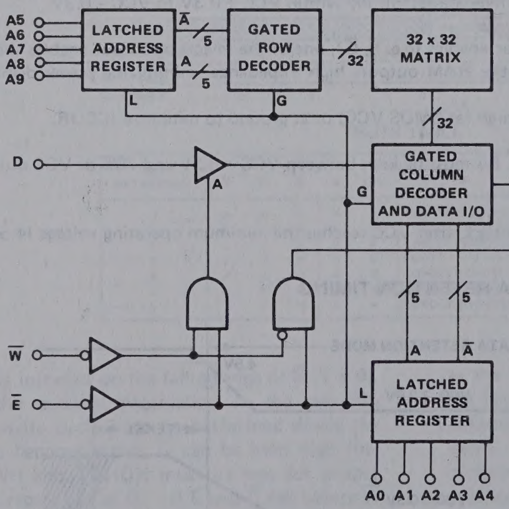
A – Address Input
Ē – Chip Enable
W̄ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Ē
+VCC
W̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
D
Q
GND

Functional Diagram



A5
A6
A7
A8
A9
LATCHED ADDRESS REGISTER
Ā
A
5
5
GATED ROW DECODER
32
32 x 32 MATRIX
L
G
32
D
A
G
GATED COLUMN DECODER AND DATA I/O
A
Q
5
5
A
Ā
W̄
Ē
L
LATCHED ADDRESS REGISTER
A0
A1
A2
A3
A4

ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6508B-2/HM-6508B-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V		
	SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		5	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
.C.	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		180	100	ns	④
	TAVQV	Address Access Time		180	90	ns	④
	TELQX	Chip Enable Output Enable Time	20	120	40	ns	④
	TWLQZ	Write Enable Output Disable Time		120	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		120	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		100	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
.C.	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	80		40	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		50	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		50	ns	④
	TWLWH	Write Enable Pulse Width	100		50	ns	④
	TELEL	Read or Write Cycle Time	280		150	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6508-2/HM-6508-9

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250	110	ns	④
	TAVQV	Address Access Time		250	100	ns	④
	TELQX	Chip Enable Output Enable Time	20	160	60	ns	④
	TWLQZ	Write Enable Output Disable Time		160	60	ns	④
	TEHQZ	Chip Enable Output Disable Time		160	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		110	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	110		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		60	ns	④
	TWLWH	Write Enable Pulse Width	130		60	ns	④
	TELEL	Read or Write Cycle Time	350		160	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6508-5

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Commercial	0°C to +75°C
Storage Temperature	-65°C to +150°C		

LECTRICAL CHARACTERISTICS

.C.

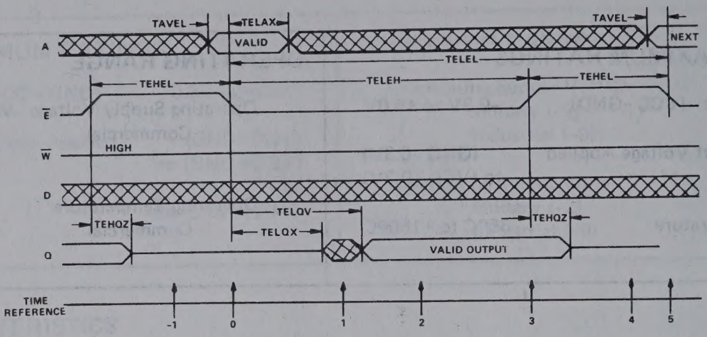
SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
		MIN	MAX	TYPICAL		
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		100	1.0	μA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0			V	
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz

.C.

SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access Time		300	160	ns	④
TAVQV	Address Access Time		310	160	ns	④
TELQX	Chip Enable Output Enable Time	20	200	60	ns	④
TWLQZ	Write Enable Output Disable Time		200	60	ns	④
TEHQZ	Chip Enable Output Disable Time		200	60	ns	④
TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
TAVEL	Address Setup Time	10		0	ns	④
TELAX	Address Hold Time	70		40	ns	④
TDVWH	Data Setup Time	130		80	ns	④
TWHDX	Data Hold Time	0		0	ns	④
TWLEH	Chip Enable Write Pulse Setup Time	160		100	ns	④
TELWH	Chip Enable Write Pulse Hold Time	160		100	ns	④
TWLWH	Write Enable Pulse Width	160		100	ns	④
TELEL	Read or Write Cycle Time	450		250	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle

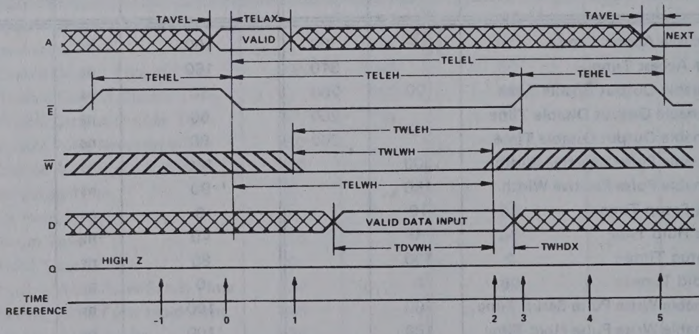

TAVEL
TELAX
VALID
TAVEL
NEXT
TELEL
TEHEL
TELEH
TEHEL
A
E
W
HIGH
D
TELQV
TEHQZ
TELQX
TEHQZ
Q
VALID OUTPUT
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID
3	↑	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6508 Read Cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Write Cycle


TAVEL
TELAX
VALID
TAVEL
NEXT
TELEL
TEHEL
TELEH
TEHEL
A
E
TWLEH
TWLWH
W
TELWH
D
VALID DATA INPUT
TDVWH
TWHDX
HIGH Z
Q
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↓	X	X	Z	WRITE PERIOD BEGINS
2	L	↑	X	V	Z	DATA IS WRITTEN
3	↑	H	X	X	Z	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

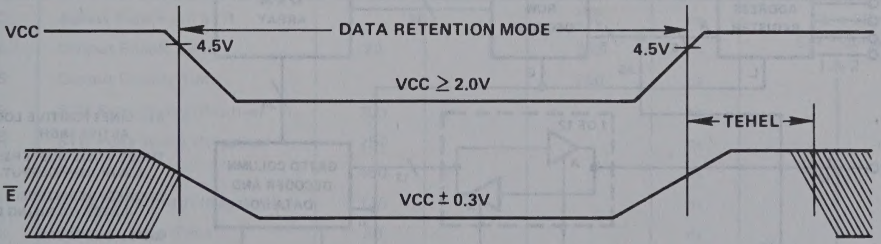
If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-651

64 × 12 CMOS RA

Features

- LOW POWER STANDBY 500µW MAX.
- LOW POWER OPERATION 20mW/MHz MAX.
- DATA RETENTION @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- TWO HM-6512's CAN BE USED WITH HM-6100 AND HM-6322 WITHOUT ADDITIONAL COMPONENTS
- THREE STATE OUTPUTS
- FAST ACCESS TIME 250ns MAX.
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

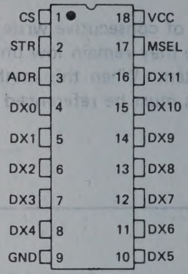
Description

The HM-6512 is a high speed, low power, silicon gate CMOS 768 bit static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4-7 volts with a typical 5 volt, 25°C access time of 150ns.

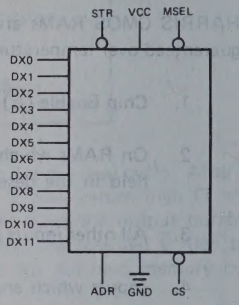
Signal polarities and functions are specified for direct interfacing with the HM-6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

Pinout

TOP VIEW

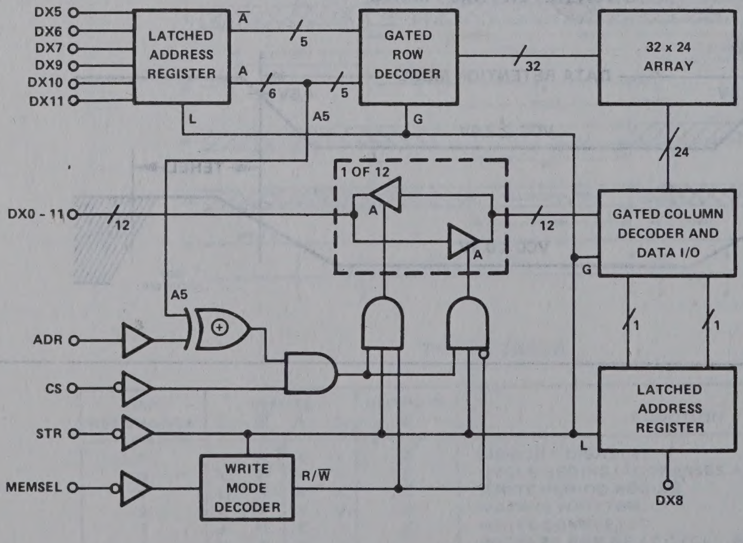

CS 1
STR 2
ADR 3
DX0 4
DX1 5
DX2 6
DX3 7
DX4 8
GND 9
18 VCC
17 MSEL
16 DX11
15 DX10
14 DX9
13 DX8
12 DX7
11 DX6
10 DX5

Logic Symbol


STR
VCC
MSEL
DX0
DX1
DX2
DX3
DX4
DX5
DX6
DX7
DX8
DX9
DX10
DX11
ADR
GND
CS

CS – Chip Select
STR – Chip Enable
MSEL – Enable and R/W Decode
ADR – Address Decode
DX – Address Input and Data I/O

Functional Diagram


DX5
DX6
DX7
DX9
DX10
DX11
LATCHED ADDRESS REGISTER
$\overline{A}$
A
5
6
5
L
A5
GATED ROW DECODER
G
32
32 x 24 ARRAY
24
1 OF 12
A
A
DX0 - 11
12
12
GATED COLUMN DECODER AND DATA I/O
G
A5
1
1
ADR
CS
STR
MEMSEL
WRITE MODE DECODER
R/$\overline{W}$
LATCHED ADDRESS REGISTER
L
DX8

ALL LINES POSITIVE LOGIC:
ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC – GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512-9	-40°C to +85°C
Military HM-6512-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ± 10%, TA = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -2.0			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-1.0		+1.0	µA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IO = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IO = 2.0mA
	IO	Output Leakage	-1.0		+1.0	µA	0V ≤ VO ≤ VCC
	VCCDR	Data Retention Supply Voltage	2.0	1.4		V	
	ICCSB	Supply Current Standby		1.0	100	µA	STR = VCC = 5.5V VI = VCC or GND
	ICCDR	Supply Current Data Retention		0.1	50	µA	STR = VCC = 2.0V VI = VCC or GND
	ICCOP	Operating Supply Current			4.0	mA	f = 1MHz, IO = 0 VI = VCC or GND
	CI*	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			250	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time	20		200	ns	
	TDIS	Output Disable Time			200	ns	
	TSTR	STR Pulse Width (Positive)	200			ns	
	$\overline{TSTR}$	STR Pulse Width (Negative)	250			ns	
	TC	Cycle Time	450			ns	
	TWP	Write Pulse Width (Negative)	130			ns	
	TAS	Address Setup Time	30			ns	
	TAH	Address Hold Time	50			ns	
	TDS	Data Setup Time	130			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	50			ns	
	TMH	MSEL Hold Time	50			ns	

* Guaranteed but not 100% tested.

Specifications HM-6512C-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ± 5%, TA = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -1.5			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-5.0		+5.0	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IO = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IO = 1.6mA
	IO	Output Leakage	-5.0		+5.0	μA	0V ≤ VO ≤ VCC
	VCCDR	Data Retention Supply Voltage	2.0	1.4		V	
	ICCSB	Supply Current Standby			800	μA	STR = VCC = 5.25V VI = VCC or GND
	ICCDR	Supply Current Data Retention			800	μA	STR = VCC = 2.0V VI = VCC or GND
	ICCOP	Operating Supply Current			4.0	mA	f = 1MHz. IO = 0 VI = VCC or GND
	CIN*	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			400	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time	20		300	ns	
	TDIS	Output Disable Time			300	ns	
	TSTR	STR Pulse Width (Positive)	250			ns	
	$\overline{\text{TSTR}}$	STR Pulse Width (Negative)	400			ns	
	TC	Cycle Time	650			ns	
	TWP	Write Pulse Width (Negative)	200			ns	
	TAS	Address Setup Time	60			ns	
	TAH	Address Hold Time	100			ns	
	TDS	Data Setup Time	200			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	100			ns	
	TMH	MSEL Hold Time	100			ns	

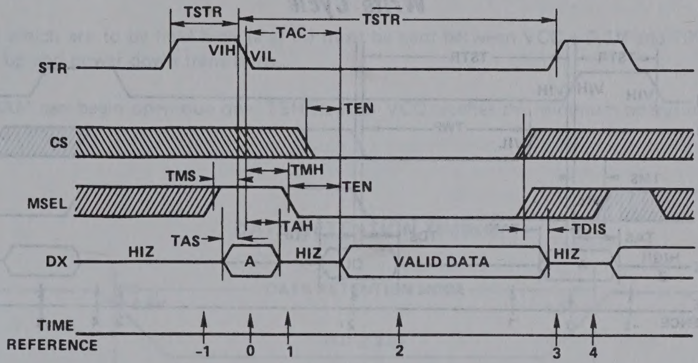
* Guaranteed but not 100% tested.

Functional Description

MSEL — The MSEL pin functions as a second chip enable and a write enable pin. If MSEL is low during the address strobe time the chip is placed in the write mode immediately. If MSEL is high during address strobe the chip performs a read operation during the first MSEL pulse and a write operation during the second MSEL pulse. In the event that a read only operation is desired the second MSEL pulse would be omitted.

ADR — The ADR pin provides the user with a method for using two HM-6512 chips in a HM-6100, HM-6312 ROM based system without any further decoding. The data on this pin is compared internally with address on DX5. If the two match, the chip will respond to MSEL and CS, otherwise the outputs remain high impedance and the stored data is unchanged. Using the HM-6312 with RSEL pin programmed for an active low for address 0-377_8 and one or two HM-6512 RAMs provides for a 64 or 128 word scratch pad memory on page 0.

Read Cycle


TSTR
TSTR
TAC
VIH
VIL
STR
TEN
CS
TMS
TMH
TEN
MSEL
TAH
TDIS
TAS
DX
HIZ
A
HIZ
VALID DATA
HIZ
TIME REFERENCE
-1
0
1
2
3
4

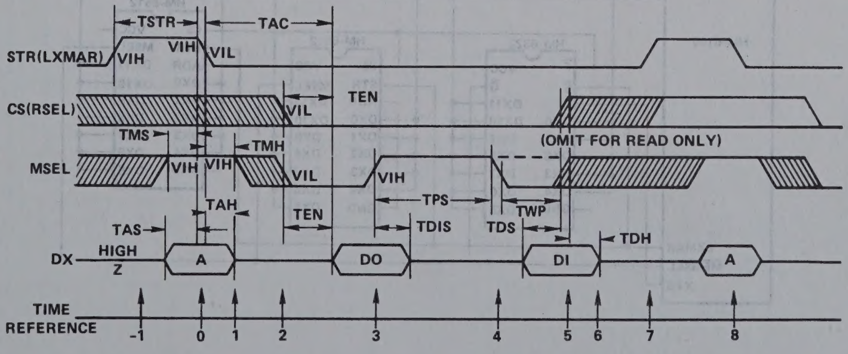
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↓	X	V*	Valid, Address Latched In
1	L	↓	X	End of Address Time
2	L	L	V	Valid, Data on Output
3	↑	H	Z	End of Read Cycle
4	H	X	Z	Begin New Cycle, Same as -1

*Address valid during this time.

FIGURE 1

Read Modify Write Cycle


TSTR
TAC
STR(LXMAR)
VIH
VIH
VIL
TEN
CS(RSEL)
VIL
TMS
TMH
(OMIT FOR READ ONLY)
MSEL
VIH
VIH
VIL
VIH
TAH
TPS
TWP
TAS
TEN
TDIS
TDS
TDH
DX
HIGH Z
A
DO
DI
A
TIME REFERENCE
-1
0
1
2
3
4
5
6
7
8

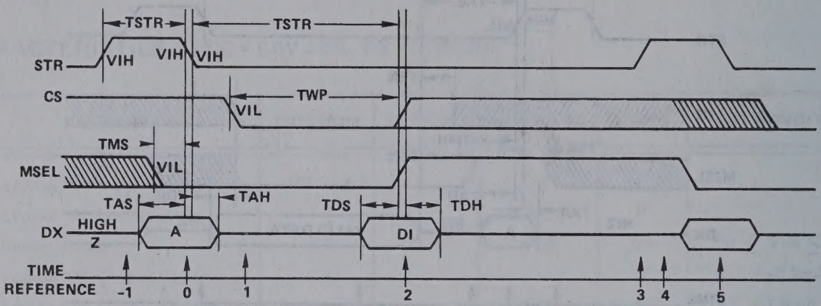
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↓	H	V*	Cycle Begins, Address Latched In
1	L	↓	Z	End of Address Time
2	L	L	X	Begin Read Time
3	L	↑	V	End of Read Time
4	L	↓	Z	Begin Write Time
5	L	↑	V	Data Written In
6	L	H	Z	End of Write Time
7	H	X	Z	End of Cycle, Memory Disabled
8	↓	H	V*	Begin New Cycle, New Address Latched In

*Address valid during this time.

FIGURE 2

Write Cycle


TSTR
TSTR
STR
VIH
VIH
VIH
CS
VIL
TWP
TMS
MSEL
VIL
TAS
TAH
TDS
TDH
DX
HIGH
Z
A
DI
TIME
REFERENCE
-1
0
1
2
3
4
5

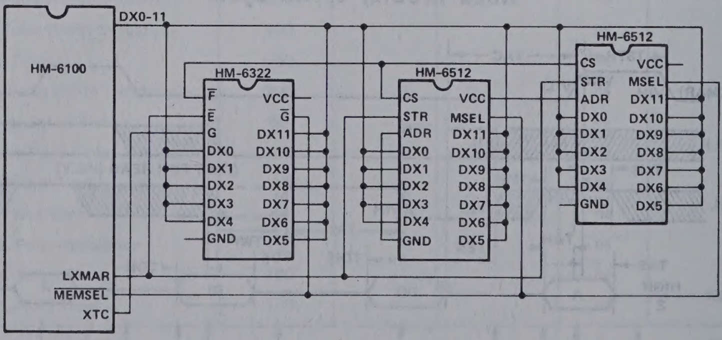
TRUTH TABLE

TIME REFERENCE	INPUTS STR	MSEL	DX	FUNCTION
-1	H	X	Z	Memory Disabled
0	↓	X	V*	Cycle Begins, Addresses are Latched
1	L	L	Z	Write Period Begins
2	L	↑	V	Data In is Written
3	↑	H	Z	Write Completed
4	H	X	Z	Prepare for Next Cycle
5	↓	X	V*	Cycle Ends, Next Cycle Begins

*Address valid during this time.

FIGURE 3

Typical Microprocessor System

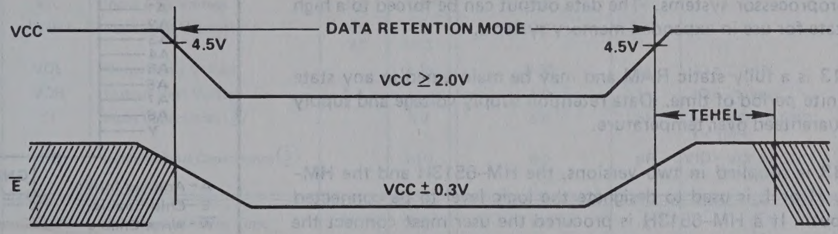

HM-6100
DX0-11
LXMAR
MEMSEL
XTC
HM-6322
F
E
G
DX0
DX1
DX2
DX3
DX4
GND
VCC
G
DX11
DX10
DX9
DX8
DX7
DX6
DX5
HM-6512
CS
STR
ADR
DX0
DX1
DX2
DX3
DX4
GND
VCC
MSEL
DX11
DX10
DX9
DX8
DX7
DX6
DX5
HM-6512
CS
STR
ADR
DX0
DX1
DX2
DX3
DX4
GND
VCC
MSEL
DX11
DX10
DX9
DX8
DX7
DX6
DX5

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HM-6513

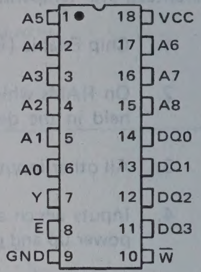
512 x 4 CMOS RAM

Features

LOW POWER STANDBY	250μW MAX.
LOW POWER OPERATION	35mW/MHz MAX.
DATA RETENTION	@ 2.0V MIN.
TTL COMPATIBILITY INPUT/OUTPUT	
COMMON DATA IN/OUT	
THREE STATE OUTPUTS	
FAST ACCESS TIME	300nsec MAX.
INDUSTRIAL OR COMMERCIAL TEMPERATURE RANGE	
18 PIN PACKAGE FOR HIGH DENSITY	
ON CHIP ADDRESS REGISTER	
PINOUT ALLOWS UPGRADE TO HM-6514	

Pinout

TOP VIEW


A5 1
A4 2
A3 3
A2 4
A1 5
A0 6
Y 7
$\overline{E}$ 8
GND 9
18 VCC
17 A6
16 A7
15 A8
14 DQ0
13 DQ1
12 DQ2
11 DQ3
10 $\overline{W}$

Description

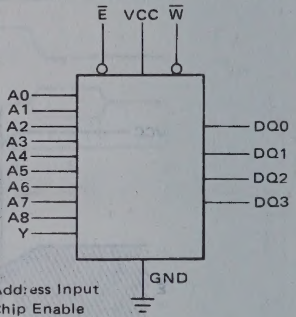
The HM-6513 is a 512 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6513 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

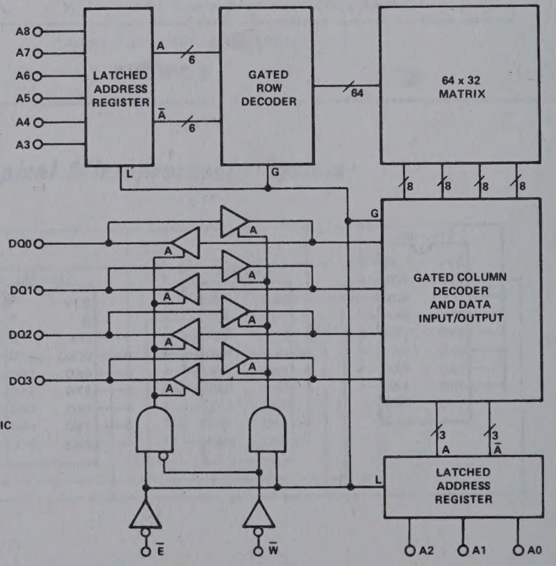
The HM-6513 is supplied in two versions, the HM-6513H and the HM-6513L. The H or L is used to designate the logic level to be connected to the Y input. If a HM-6513H is procured the user must connect the input to VCC in the system. If a HM-6513L is used the Y input must be connected to system ground.

Logic Symbol


$\overline{E}$
VCC
$\overline{W}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
Y
DQ0
DQ1
DQ2
DQ3
GND

A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
DQ – Data In/Out
Y – Hard Wired Input

Functional Diagram


A8
A7
A6
A5
A4
A3
LATCHED ADDRESS REGISTER
A
6
$\overline{A}$
6
L
GATED ROW DECODER
G
64
64 x 32 MATRIX
8
8
8
8
G
GATED COLUMN DECODER AND DATA INPUT/OUTPUT
DQ0
DQ1
DQ2
DQ3
A
3
A
3
$\overline{A}$
L
LATCHED ADDRESS REGISTER
$\overline{E}$
$\overline{W}$
A2
A1
A0

ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage — (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Range Industrial (-9)	-40°C to 85°C

LECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V		
	SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	µA	IO = 0VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	170	ns	④
	TAVQV	Address Access Time		320	170	ns	④
	TELQX	Chip Enable Output Enable Time		100	50	ns	④
	TWLQZ	Write Enable Output Disable Time	20	100	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	300		150	ns	④
	TWLEH	Write Enable Pulse Setup Time	300		150	ns	④
	TELWH	Write Enable Pulse Hold Time	300		150	ns	④
	TDVWH	Data Setup Time	200		100	ns	④
	TWHDZ	Data Hold Time	0		-10	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TWLEL	Early Output High-Z Time	0		-10	ns	④
	TEHWH	Late Output High-Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	420		240	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

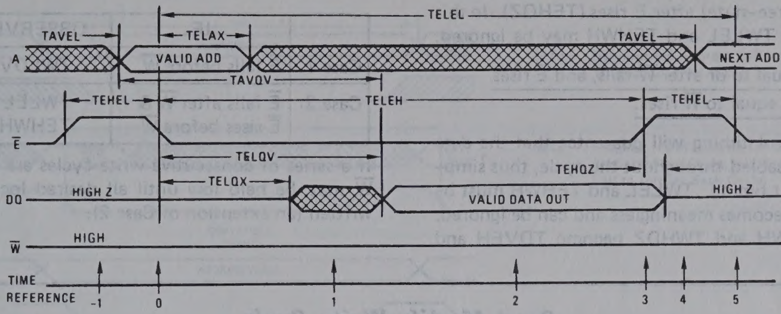
Operating Supply Voltage Commercial	4.5V to 5.5V
Operating Temperature Range Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C① VCC = 5.0V		
	SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	50	µA	VI = VCC or GND IO = 0
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	10	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	±0.5	µA	GND ≤ VIO ≤ VCC
	VIL	Logical "0" Input Voltage	-0.3	0.8	2.0	V	
	VIH	Logical "1" Input Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Logical "0" Output Voltage		0.45	0.35	V	IO = 1.6mA
	VOH	Logical "1" Output Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		370	200	ns	④
	TELQX	Chip Enable Output Enable Time		100	50	ns	④
	TWLQZ	Write Enable Output Disable Time	20	100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	350		200	ns	④
	TWLEH	Write Enable Pulse Setup Time	350		200	ns	④
	TELWH	Write Enable Pulse Hold Time	350		200	ns	④
	TDVWH	Data Setup Time	250		150	ns	④
	TWHDZ	Data Hold Time	0		-10	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TWLEL	Early Output High-Z Time	0		-10	ns	④
	TEHWH	Late Output High-Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	500		320	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle


TELEL
TAVEL
TELAX
TAVEL
A
VALID ADD
NEXT ADD
TAVQV
TEHEL
TELEH
TEHEL
Ē
TELQV
TELQX
TEHQZ
DQ
HIGH Z
VALID DATA OUT
HIGH Z
W̄
HIGH
TIME REFERENCE
-1
0
1
2
3
4
5

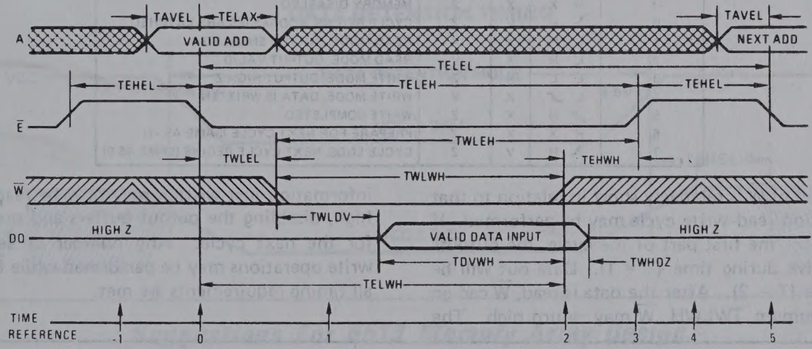
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until time (T = 2).

$\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle


TAVEL
TELAX
TAVEL
A
VALID ADD
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
Ē
TWLEH
TWLEL
TEHWH
W̄
TWLWH
TWLDV
DQ
HIGH Z
VALID DATA INPUT
HIGH Z
TDVWH
TWHDZ
TELWH
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TLWDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before E. The RAM outputs will disable (three-state) after E rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

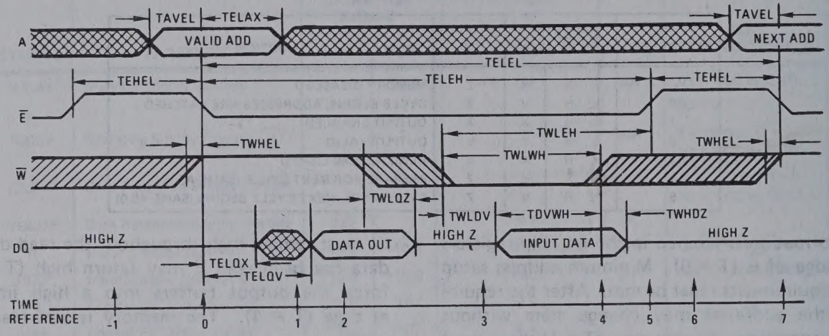
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Read Modify Write Cycle



TRUTH TABLE

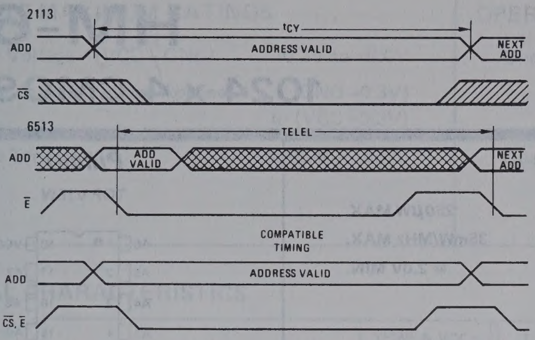
TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = X) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2113 Compatibility


2113
ADD
tCY
ADDRESS VALID
NEXT ADD
CS
6513
ADD
TELEL
ADD VALID
NEXT ADD
E
COMPATIBLE TIMING
ADD
ADDRESS VALID
CS, E

2113 – Requires the Address to Remain Valid Throughout the Cycle.

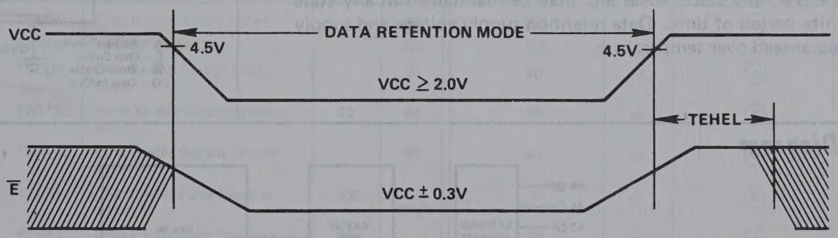
6513 – Requires Valid Address for Only a Small Portion of the Cycle, but Requires E̅ to Fall to Initiate Each Cycle.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

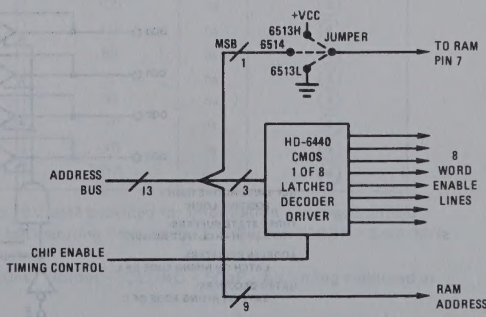
1. Chip Enable (E̅) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. S̅, G̅), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. E̅) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING


VCC
DATA RETENTION MODE
4.5V
4.5V
VCC ≥ 2.0V
TEHEL
E
VCC ± 0.3V

Suggestions For 6513 Memory Array Design

The HM-6513 is a device that can be used to good advantage in systems which are offered with choices of memory array size. With one common memory board layout the designer can easily offer two different array sizes. This is accomplished by using the conveniently similar pinouts of the HM-6513 (512 by 4) and the HM-6514 (1K by 4). For example, a 4K by 8 bit array using HM-6513s and a 8K word by 8 bit array using HM-6514s can be easily implemented on the same printed circuit card. The circuit diagram suggests one implementation requiring only one jumper wire for 4K or 8K word selection. This simple jumper wire also allows the 4K array to utilize the HM-6513H or the HM-6513L version.


+VCC
6513H
JUMPER
MSB
6514
1
TO RAM PIN 7
6513L
HD-6440 CMOS 1 OF 8 LATCHED DECODER DRIVER
8 WORD ENABLE LINES
ADDRESS BUS
13
3
CHIP ENABLE TIMING CONTROL
9
RAM ADDRESSES

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6514

1024 x 4 CMOS RAM

Features

LOW POWER STANDBY	250μW MAX.
LOW POWER OPERATION	35mW/MHz MAX.
DATA RETENTION	@ 2.0V MIN.
TTL COMPATIBLE INPUT/OUTPUT	
COMMON DATA IN/OUT	
THREE-STATE OUTPUTS	
STANDARD JEDEC PINOUT	
FAST ACCESS TIME	200nsec MAX.
MILITARY TEMPERATURE RANGE	
INDUSTRIAL TEMPERATURE RANGE	
18 PIN PACKAGE FOR HIGH DENSITY	
ON CHIP ADDRESS REGISTER	

Description

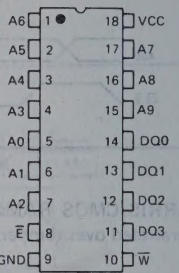
The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

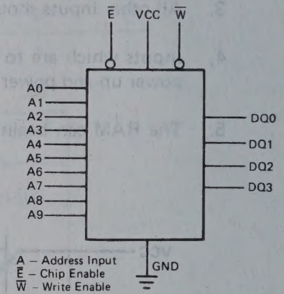
The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Pinout

TOP VIEW

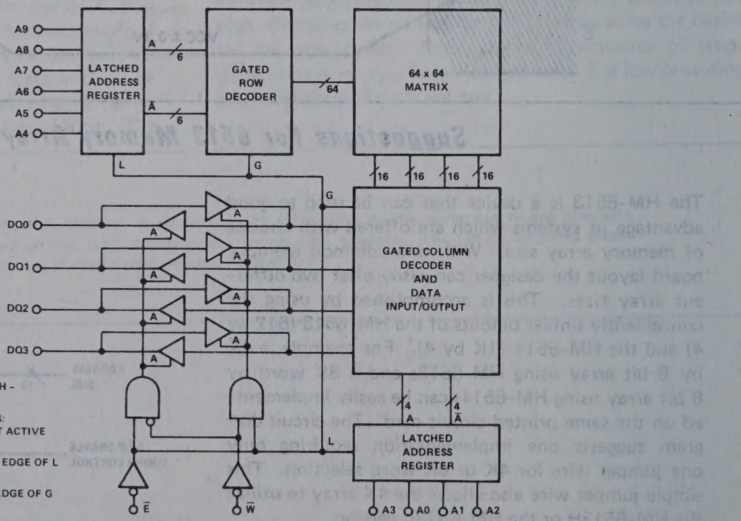

A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
Ē 8
GND 9
18 VCC
17 A7
16 A8
15 A9
14 DQ0
13 DQ1
12 DQ2
11 DQ3
10 W̄

Logic Symbol


Ē
VCC
W̄
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
DQ0
DQ1
DQ2
DQ3
GND

A – Address Input
Ē – Chip Enable
W̄ – Write Enable
DQ – Data In/Out

Functional Diagram


A9
A8
A7
A6
A5
A4
LATCHED ADDRESS REGISTER
A
6
Ā
6
GATED ROW DECODER
64
64 x 64 MATRIX
L
G
16
16
16
16
G
DQ0
DQ1
DQ2
DQ3
A
GATED COLUMN DECODER AND DATA INPUT/OUTPUT
4
A
4
Ā
L
LATCHED ADDRESS REGISTER
Ē
W̄
A3
A0
A1
A2

ALL LINES ACTIVE HIGH - POSITIVE LOGIC
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE
ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L
GATED DECODERS:
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	4.5V to 5.5V
Military (-2)	4.5V to 5.5V
Industrial (-9)	
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	0.1	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200	150	ns	④
	TAVQV	Address Access Time		220	150	ns	④
	TELQX	Chip Enable Output Enable Time		80	40	ns	④
	TWLQZ	Write Enable Output Disable Time	20	80	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		80	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	200		150	ns	④
	TEHEL	Chip Enable Pulse Positive Width	90		60	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	200		100	ns	④
	TWLEH	Write Enable Pulse Setup Time	200		100	ns	④
	TELWH	Write Enable Pulse Hold Time	200		150	ns	④
	TDVWH	Data Setup Time	120		80	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	80		50	ns	④
	TWLEL	Early Output High-Z Time	0		-10	ns	④
	TEHWH	Late Output High-Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	290		210	ns	④

NOTES:
① All devices tested at worst case limits. Room Temp., 5V data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC test conditions: Inputs — TRISE = TFALL = 20ns; Output — CLOAD = 50pF. All timing measured at 1.5V reference level.

Specifications HM-6514-2/HM-6514-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		50	1.0	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		25	0.1	μA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
CIO	Input/Output Capacitance ③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz

A.C.

SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access Time		300	170	ns	④
TAVQV	Address Access Time		320	170	ns	④
TELQX	Chip Enable Output Enable Time		100	40	ns	④
TWLQZ	Write Enable Output Disable Time	20	100	40	ns	④
TEHQZ	Chip Enable Output Disable Time		100	40	ns	④
TELEH	Chip Enable Pulse Negative Width	300		170	ns	④
TEHEL	Chip Enable Pulse Positive Width	120		70	ns	④
TAVEL	Address Setup Time	20		0	ns	④
TELAX	Address Hold Time	50		20	ns	④
TWLWH	Write Enable Pulse Width	300		150	ns	④
TWLEH	Write Enable Pulse Setup Time	300		150	ns	④
TELWH	Write Enable Pulse Hold Time	300		150	ns	④
TDVWH	Data Setup Time	200		100	ns	④
TWHDZ	Data Hold Time	0		0	ns	④
TWLDV	Write Data Delay Time	100		50	ns	④
TWLEL	Early Output High-Z Time	0		-10	ns	④
TEHWH	Late Output High-Z Time	0		-10	ns	④
TELEL	Read or Write Cycle Time	420		240	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Industrial (-9)	-40°C to +85°C

LECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C① VCC = 5.0V		
	SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		50	0.1	μA	VCC = 2.0V, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	170	ns	④
	TAVQV	Address Access Time		320	170	ns	④
	TELQX	Chip Enable Output Enable Time		100	40	ns	④
	TWLQZ	Write Enable Output Disable Time	20	100	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		70	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	300		150	ns	④
	TWLEH	Write Enable Pulse Setup Time	300		150	ns	④
	TELWH	Write Enable Pulse Hold Time	300		170	ns	④
	TDVWH	Data Setup Time	200		100	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TWLEL	Early Output High-Z Time	0		-10	ns	④
	TEHWH	Late Output High-Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	420		240	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6514-5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

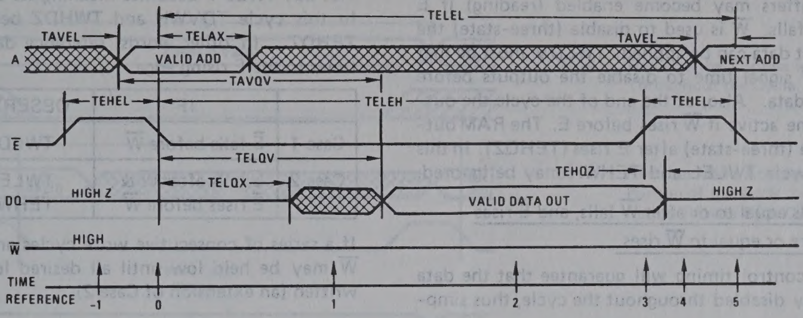
Operating Supply Voltage Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	50	μA	VI = VCC or GND IO = 0
	ICCOP	Operating Supply Current ②		7	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	10	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	±0.5	μA	VCC ≤ VIO ≤ GND
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
	CI	Input Capacitance③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance③		10.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	200	ns	④
	TAVQV	Address Access Time		370	200	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TWLQZ	Write Enable Output Disable Time		100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		100	ns	④
	TAVEL	Address Setup Time	20		0	ns	④
	TELAX	Address Hold Time	50		20	ns	④
	TWLWH	Write Enable Pulse Width	350		200	ns	④
	TWLEH	Write Enable Pulse Setup Time	350		200	ns	④
	TELWH	Write Enable Pulse Hold Time	350		200	ns	④
	TDVWH	Data Setup Time	250		150	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TWLEL	Early Output High-Z Time	0		-10	ns	④
	TEHWH	Late Output High-Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	500		320	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle

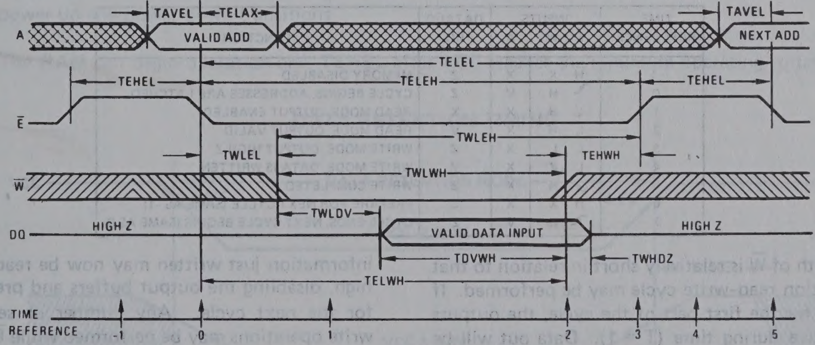

TELEL
TAVEL
TELAX
TAVEL
A
VALID ADD
NEXT ADD
TAVQV
TEHEL
TELEH
TEHEL
$\overline{E}$
TELQV
TEHQZ
TELQX
DQ
HIGH Z
VALID DATA OUT
HIGH Z
HIGH
$\overline{W}$
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS			DATA I/O	FUNCTION
	$\overline{E}$	$\overline{W}$	A	DQ	
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle


TAVEL
TELAX
TAVEL
A
VALID ADD
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
$\overline{E}$
TWLEH
TWLEL
TEHWH
TWLWH
$\overline{W}$
TWLDV
DQ
HIGH Z
VALID DATA INPUT
HIGH Z
TDVWH
TWHDZ
TELWH
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS				FUNCTION
	$\overline{E}$	$\overline{W}$	A	DQ	
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before E. The RAM outputs will disable (three-state) after E rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

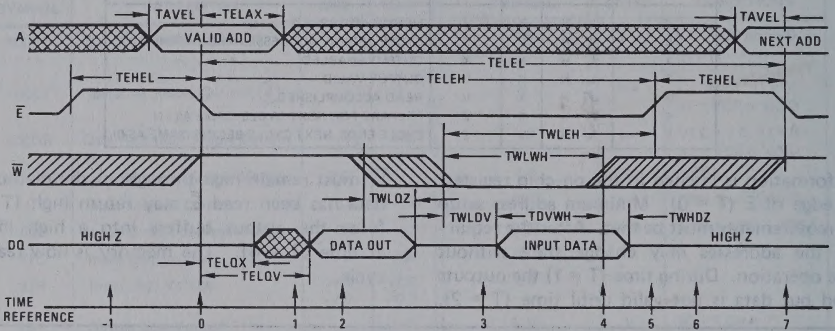
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Read Modify Write Cycle



TRUTH TABLE

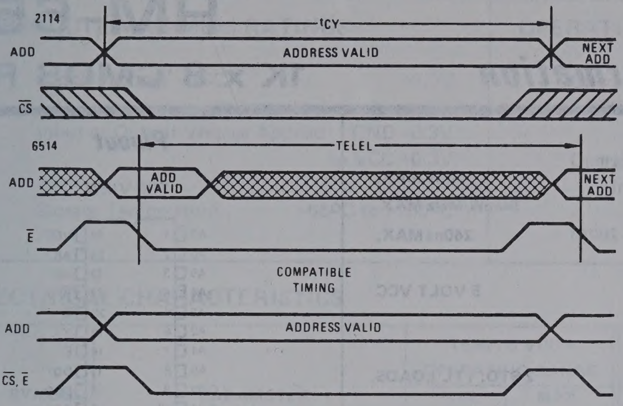
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

2114 Compatibility


2114
ADD
tCY
ADDRESS VALID
NEXT ADD
CS
6514
ADD
TELEL
ADD VALID
NEXT ADD
E
COMPATIBLE TIMING
ADD
ADDRESS VALID
CS, E

2114 — Requires the Address to Remain Valid Throughout the Cycle.

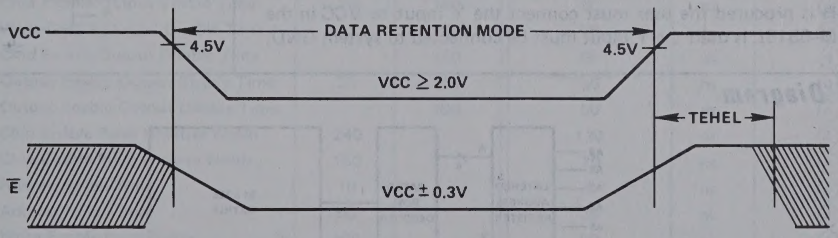
6514 — Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING


VCC
4.5V
DATA RETENTION MODE
4.5V
VCC ≥ 2.0V
TEHEL
E
VCC ± 0.3V

HM-6515

1K x 8 CMOS RAM

Advance Information

Features

• LOW POWER STANDBY	5mW MAX.
• LOW POWER OPERATION	50mW/MHz MAX.
• FAST ACCESS	240ns MAX.
• INDUSTRY STANDARD PINOUT	
• SINGLE SUPPLY	5 VOLT VCC
• TTL COMPATIBLE	
• STATIC MEMORY CELLS	
• HIGH OUTPUT DRIVE	2 STD. TTL LOADS
• ON CHIP ADDRESS LATCHES	
• EASY MICROPROCESSOR INTERFACING	
• WIDE TEMPERATURE RANGE	

Description

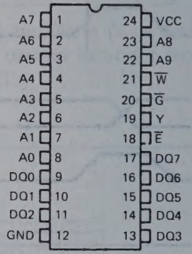
The HM-6515 is a CMOS 1024 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6515 is the popular 24 pin, 8 bit wide standard which allows easy memory board layouts, flexible enough to accomodate a variety of PROMs, RAMs, EPROMs and ROMs.

The HM-6515 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus, such as the 8085. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

The HM-6515 is supplied in two versions, the HM-6515H and the HM-6515L. The H or L is used to designate the logic level to be connected to the Y input. If an HM-6515H is procured the user must connect the Y input to VCC in the system. If an HM-6515L is used the Y input must be connected to system GND.

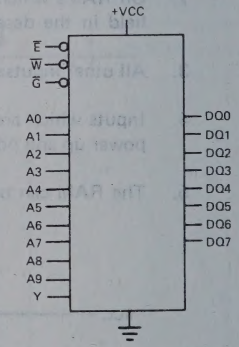
Pinout

TOP VIEW

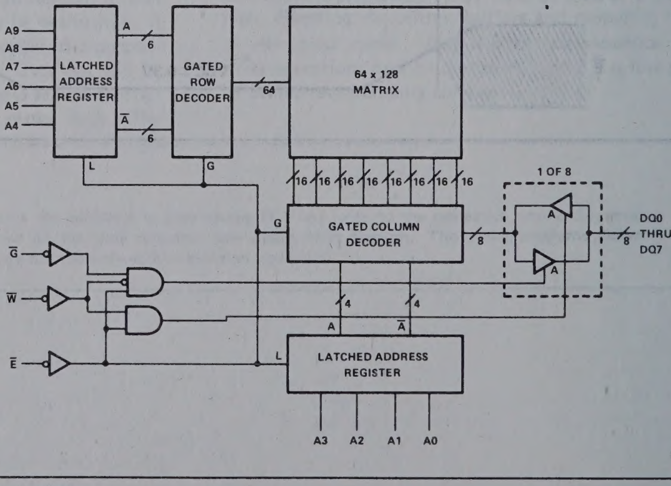

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
GND 12
24 VCC
23 A8
22 A9
21 W̄
20 Ḡ
19 Y
18 Ē
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
Y	Hard Wired Input

Logic Symbol


+VCC
Ē
W̄
Ḡ
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
Y
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7

Functional Diagram


A9
A8
A7
A6
A5
A4
LATCHED ADDRESS REGISTER
A
6
Ā
6
L
GATED ROW DECODER
G
64
64 x 128 MATRIX
16 16 16 16 16 16 16 16
G
GATED COLUMN DECODER
8
1 OF 8
A
A
8
DQ0 THRU DQ7
Ḡ
W̄
Ē
4
4
A
Ā
L
LATCHED ADDRESS REGISTER
A3
A2
A1
A0

ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Ranges: Industrial (-9)	-40°C to +85°C
Input Rise/Fall Time	≤10μs

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYP		
D.C.	ICCSB	Standby Supply Current		1.0	0.10	mA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10.0	7.0	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	0.05	μA	IO = 0, VCC = 2.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.40	0.35	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	7.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		240	130	ns	④
	TAVQV	Address Access Time		250	130	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TWLQZ	Write Enable Output Disable Time		100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TGLQV	Output Enable Output Enable Time	20	100	50	ns	④
	TGHQZ	Output Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	240		130	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		70	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TELAX	Address Hold Time	50		35	ns	④
	TWLWH	Write Enable Pulse Width	100		50	ns	④
	TWLEH	Write Enable Pulse Setup Time	100		50	ns	④
	TELWH	Write Enable Pulse Hold Time	240		130	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWHEL	Write Enable Read Setup Time	0		0	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TELEL	Read or Write Cycle Time	390		200	ns	④

NOTES:

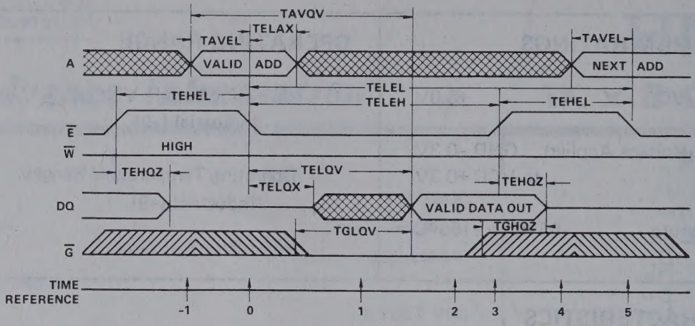
① All devices tested at worst case limits. Room temp., 5 volt data provided for information-not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
Example: Typical ICCOP = 5mA/MHz.

③ Capacitance sampled and guaranteed-not 100% tested.

④ AC test conditions: Inputs—TRISE = TFALL = 20ns; Output—CLOAD = 50pF. All timing measured at 1.5V reference level.

Read Cycle

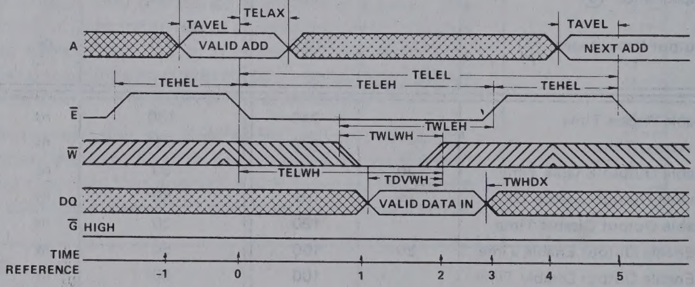

TAVQV
TELAX
TAVEL
TAVEL
A
VALID ADD
NEXT ADD
TEHEL
TELEL
TELEH
TEHEL
$\overline{E}$
$\overline{W}$
HIGH
TEHQZ
TELQV
TELQX
TEHQZ
DQ
VALID DATA OUT
TGLQV
TGHQZ
$\overline{G}$
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	OUTPUT ENABLED
2	L	H	L	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle

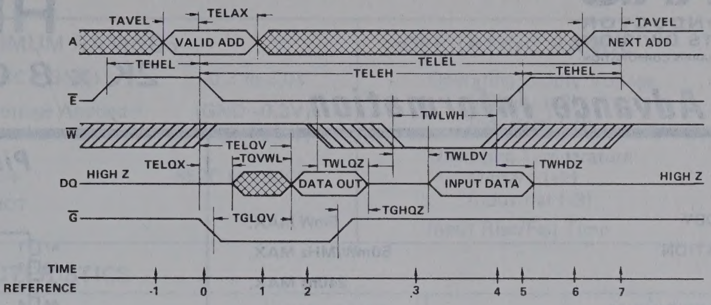

TELAX
TAVEL
TAVEL
A
VALID ADD
NEXT ADD
TEHEL
TELEH
TELEL
TEHEL
$\overline{E}$
TWLEH
TWLWH
$\overline{W}$
TELWH
TDVWH
TWHDX
DQ
VALID DATA IN
$\overline{G}$ HIGH
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS E	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	H	X	X	MEMORY DISABLED
0	↘	X	H	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	DATA IN IS WRITTEN
3	↗	H	H	X	X	WRITE COMPLETED
4	H	X	H	X	X	PREPARE FOR NEXT CYCLE (SAME AS-1)
5	↘	X	H	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$(T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low unitl all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DATA I/O DQ	FUNCTION
-1	H	X	H	X	Z	MEMORY DISABLED
0	↘	H	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	READ MODE, OUTPUT ENABLED ($\overline{W}$ = HIGH, $\overline{G}$ = LOW)
2	L	H	L	X	V	READ MODE, OUTPUT VALID
3	L	L	H	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	H	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	H	X	Z	WRITE COMPLETED
6	H	X	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$, a combination read write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the output will become active during time (T = 1) provided $\overline{G}$ is low. Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minimum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffer and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

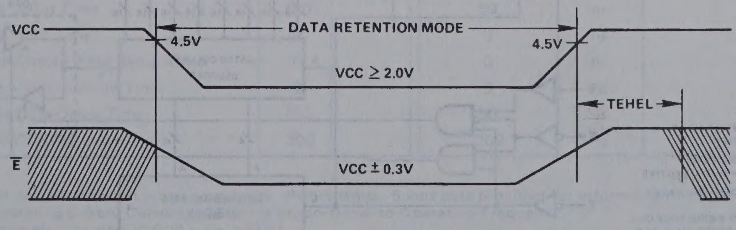
In the above descriptions, the numbers in parentheses (T = n), refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6516

2K x 8 CMOS RAM

Advance Information

Features

LOW POWER STANDBY	5mW MAX.
LOW POWER OPERATION	50mW/MHz MAX.
FAST ACCESS	240ns MAX.
INDUSTRY STANDARD PINOUT	
SINGLE SUPPLY	5 VOLT VCC
TTL COMPATIBLE	
STATIC MEMORY CELLS	
HIGH OUTPUT DRIVE	2 STD. TTL LOADS
ON CHIP ADDRESS LATCHES	
EASY MICROPROCESSOR INTERFACING	
WIDE TEMPERATURE RANGE	

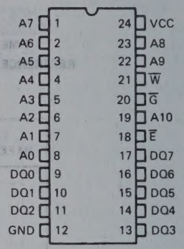
Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6516 is the popular 24 pin, 8 bit wide standard which allows easy memory board layouts, flexible enough to accomodate a variety of PROMs, RAMs, EPROMs, and ROMs.

The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus, such as the 8085. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independant of the chip enable.

Pinout

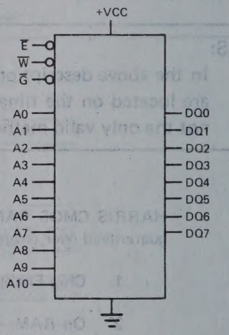
TOP VIEW



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
GND 12
24 VCC
23 A8
22 A9
21 $\overline{W}$
20 $\overline{G}$
19 A10
18 $\overline{E}$
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

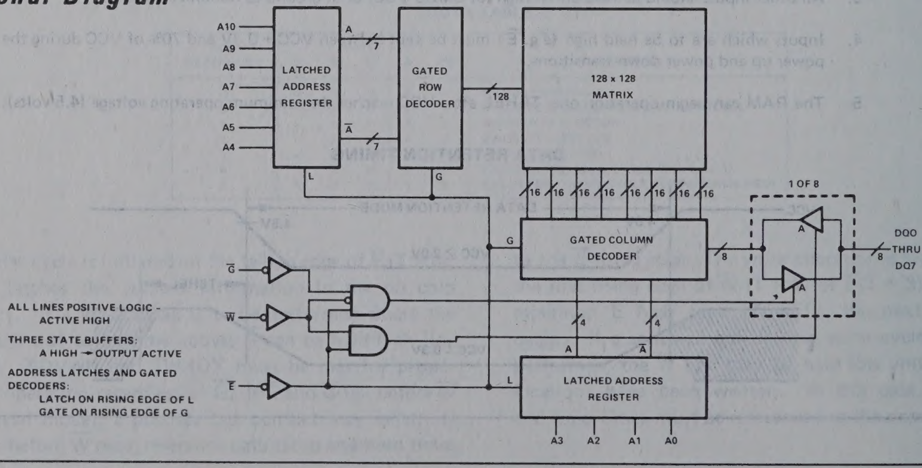
A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

Logic Symbol



+VCC
$\overline{E}$
$\overline{W}$
$\overline{G}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7

Functional Diagram



A10
A9
A8
A7
A6
A5
A4
LATCHED ADDRESS REGISTER
A
7
$\overline{A}$
7
L
GATED ROW DECODER
G
128
128 x 128 MATRIX
16
GATED COLUMN DECODER
G
8
1 OF 8
A
A
DQ0 THRU DQ7
8
$\overline{G}$
$\overline{W}$
$\overline{E}$
ALL LINES POSITIVE LOGIC - ACTIVE HIGH
THREE STATE BUFFERS: A HIGH → OUTPUT ACTIVE
ADDRESS LATCHES AND GATED DECODERS: LATCH ON RISING EDGE OF L GATE ON RISING EDGE OF G
4
4
A
$\overline{A}$
L
LATCHED ADDRESS REGISTER
A3
A2
A1
A0

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6516-2/HM-6516-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3 to 8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to 150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C
Input Rise/Fall Time	≤10μs

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C VCC = 5.0V ① TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0	0.10	mA	IO = 0, VI = VCC or GND
	ICCOP	Operating Supply Current ②		10.0	7.0	mA	f = 1MHz, IO = 0, VI = VCC or GND
	ICCDR	Data Retention Supply Current		500	0.05	μA	IO = 0, VCC = 2.0, VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0			V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	-3.0	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.45	0.35	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	7.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		240	130	ns	④
	TAVQV	Address Access Time		250	130	ns	④
	TELQX	Chip Enable Output Enable Time	20	100	50	ns	④
	TWLQZ	Write Enable Output Disable Time		100	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	ns	④
	TGLQV	Output Enable Output Enable Time	20	100	50	ns	④
	THGQZ	Output Enable Output Disable Time		100	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	240		130	ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		70	ns	④
	TAVEL	Address Setup Time	10		0	ns	④
	TELAX	Address Hold Time	50		35	ns	④
	TWLWH	Write Enable Pulse Width	100		50	ns	④
	TWLEH	Write Enable Pulse Setup Time	100		50	ns	④
	TELWH	Write Enable Pulse Hold Time	240		130	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDZ	Data Hold Time	0		0	ns	④
	TWHEL	Write Enable Read Setup Time	0		0	ns	④
	TQVWL	Data Valid to Write Time	0		0	ns	④
	TWLDV	Write Data Delay Time	100		50	ns	④
	TELEL	Read or Write Cycle Time	390		200	ns	④

NOTES:

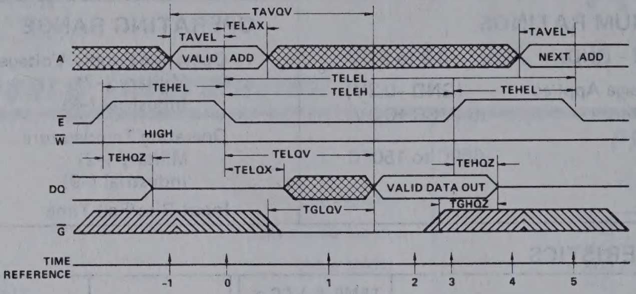
① All devices tested at worst case limits. Room temp., 5 volt data provided for information-not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
Example: Typical ICCOP = 5mA/MHz.

③ Capacitance sampled and guaranteed-not 100% tested.

④ AC test conditions: Inputs—TRISE = TFALL = 20ns; Output—CLOAD = 50pF. All timing measured at 1.5V reference level.

Read Cycle

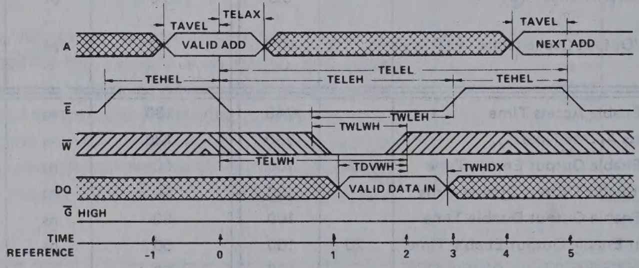

TAVQV
TELAX
TAVEL
TAVEL
A
VALID ADD
NEXT ADD
TEHEL
TELEL
TELEH
TEHEL
E
W
HIGH
TEHQZ
TELQV
TELQX
TEHQZ
DQ
VALID DATA OUT
TGLQV
TGHQZ
G
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
	INPUTS					
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	OUTPUT ENABLED
2	L	H	L	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers by the falling edge of $\overline{E}$ (T = 0), minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle

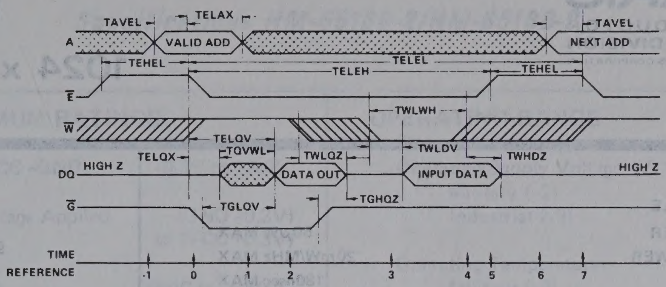

TELAX
TAVEL
TAVEL
A
VALID ADD
NEXT ADD
TEHEL
TELEL
TELEH
TEHEL
E
TWLEH
TWLWH
W
TELWH
TDVWH
TWHDX
DQ
VALID DATA IN
G HIGH
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
	INPUTS					
-1	H	X	H	X	X	MEMORY DISABLED
0	↘	X	H	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	DATA IN IS WRITTEN
3	↗	H	H	X	X	WRITE COMPLETED
4	H	X	H	X	X	PREPARE FOR NEXT CYCLE (SAME AS-1)
5	↘	X	H	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$ (T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

Read Modify Write Cycle


TAVEL
TELAX
TAVEL
A
VALID ADD
NEXT ADD
TEHEL
TELEL
TELEH
TEHEL
$\overline{E}$
TWLWH
$\overline{W}$
TELQV
TQVWL
TWLQZ
TWLDV
TWHDZ
TELQX
HIGH Z
DQ
DATA OUT
INPUT DATA
HIGH Z
TGHQZ
$\overline{G}$
TGLQV
TIME REFERENCE
-1
0
1
2
3
4
5
6
7

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{G}$	A	DATA I/O DQ	FUNCTION
–1	H	X	H	X	Z	MEMORY DISABLED
0	↘	H	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	READ MODE, OUTPUT ENABLED ($\overline{W}$ = HIGH, $\overline{G}$ = LOW)
2	L	H	L	X	V	READ MODE, OUTPUT VALID
3	L	L	H	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	H	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	H	X	Z	WRITE COMPLETED
6	H	X	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS –1)
7	↘	H	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$, a combination read write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the output will become active during time (T = 1) provided $\overline{G}$ is low. Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minimum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffer and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

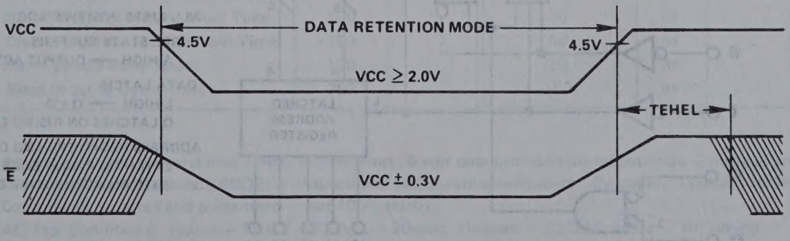
In the above descriptions, the numbers in parentheses (T=n), refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING


VCC
DATA RETENTION MODE
4.5V
4.5V
VCC ≥ 2.0V
TEHEL
$\overline{E}$
VCC ± 0.3V

HM-6518

1024 x 1 CMOS RAM

Features

• HM-6100 COMPATIBLE	
• LOW STANDBY POWER	50µW MAX
• LOW OPERATING POWER	20mW/MHz MAX
• FAST ACCESS TIME	180nsec MAX
• DATA RETENTION VOLTAGE	2.0 VOLTS MIN
• TTL COMPATIBLE IN/OUT	
• HIGH OUTPUT DRIVE - 2 TTL LOADS	
• HIGH NOISE IMMUNITY	
• ON CHIP ADDRESS REGISTER	
• TWO CHIP SELECTS FOR EASY ARRAY EXPANSION	
• THREE STATE OUTPUTS	
• MILITARY TEMPERATURE RANGE	
• INDUSTRIAL TEMPERATURE RANGE	

Description

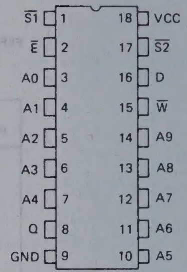
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

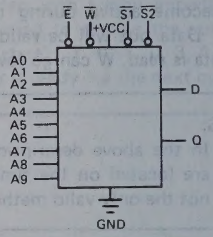
Pinout

TOP VIEW


$\overline{S1}$ 1
$\overline{E}$ 2
A0 3
A1 4
A2 5
A3 6
A4 7
Q 8
GND 9
18 VCC
17 $\overline{S2}$
16 D
15 $\overline{W}$
14 A9
13 A8
12 A7
11 A6
10 A5

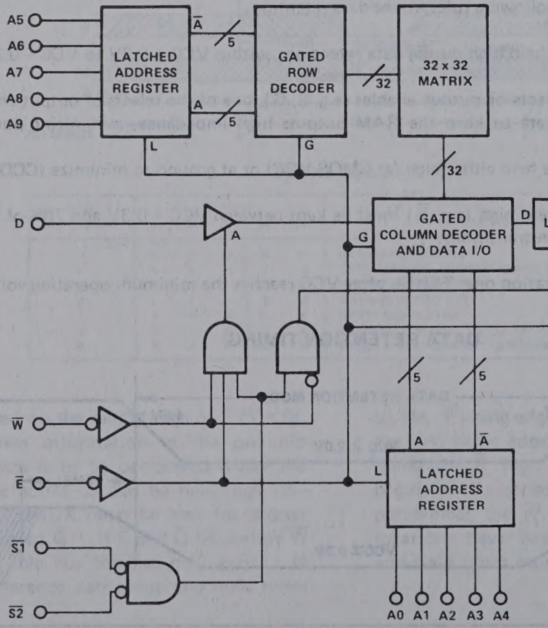
A - ADDRESS INPUT
$\overline{E}$ - CHIP ENABLE
$\overline{S}$ - CHIP SELECT
$\overline{W}$ - WRITE ENABLE
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol


$\overline{E}$
$\overline{W}$
$\overline{S1}$
$\overline{S2}$
+VCC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
D
Q
GND

3

Functional Diagram


A5
A6
A7
A8
A9
LATCHED ADDRESS REGISTER
$\overline{A}$
5
A
5
L
GATED ROW DECODER
G
32
32 x 32 MATRIX
32
D
A
GATED COLUMN DECODER AND DATA I/O
G
D
LATCH
Q
L
A
Q
$\overline{W}$
$\overline{E}$
$\overline{S1}$
$\overline{S2}$
5
5
A
$\overline{A}$
L
LATCHED ADDRESS REGISTER
A0
A1
A2
A3
A4

ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCH:
L HIGH → Q = D
Q LATCHES ON RISING EDGE OF L

ADDRESS REGISTERS AND DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6518B-2/HM-6518B-9

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

LECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
		MIN	MAX	TYPICAL		
ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		5	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
TELQV	Chip Enable Access Time		180	100	ns	④
TAVQV	Address Access Time		180	90	ns	④
TSLQX	Chip Select Output Enable Time	20	120	40	ns	④
TWLQX	Write Enable Output Disable Time		120	40	ns	④
TSHQX	Chip Select Output Disable Time		120	40	ns	④
TELEH	Chip Enable Pulse Negative Width	180		100	ns	④
TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
TAVEL	Address Setup Time	0		-10	ns	④
TELAX	Address Hold Time	40		20	ns	④
TDVWH	Data Setup Time	80		30	ns	④
TWHDX	Data Hold Time	0		0	ns	④
TWLSH	Chip Select Write Pulse Setup Time	100		50	ns	④
TWLEH	Chip Enable Write Pulse Setup Time	100		50	ns	④
TSLWH	Chip Select Write Pulse Hold Time	100		50	ns	④
TELWH	Chip Enable Write Pulse Hold Time	100		50	ns	④
TWLWH	Write Enable Pulse Width	100		50	ns	④
TELEL	Read or Write Cycle Time	280		150	ns	④

.C.

.C.

NOTES
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6518-2/HM-6518-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -(VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250	110	ns	④
	TAVQV	Address Access Time		250	100	ns	④
	TSLQX	Chip Select Output Enable Time	20	160	60	ns	④
	TWLQX	Write Enable Output Disable Time		160	60	ns	④
	TSHQX	Chip Select Output Disable Time		160	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		110	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	110		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	130		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		60	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	130		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		60	ns	④
	TWLWH	Write Enable Pulse Width	130		60	ns	④
	TELEL	Read or Write Cycle Time	350		160	ns	④

NOTES: ① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.

③ Capacitance sampled and guaranteed — not 100% tested.

④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6518-5

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage -(VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

.C.

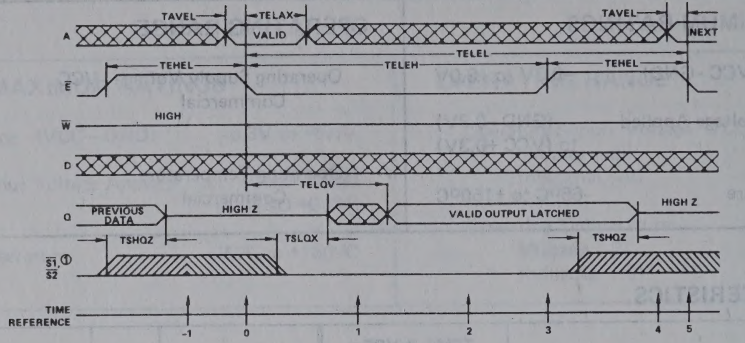
SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
		MIN	MAX	TYPICAL		
ICCSB	Standby Supply Current		100	10	µA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		100	1.0	µA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0			V	
II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VI ⩽ VCC
IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ⩽ VO ⩽ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz

.C.

SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access Time		300	160	ns	④
TAVQV	Address Access Time		310	160	ns	④
TSLQX	Chip Select Output Enable Time	20	200	60	ns	④
TWLQX	Write Enable Output Disable Time		200	60	ns	④
TSHQX	Chip Select Output Disable Time		200	60	ns	④
TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
TAVEL	Address Setup Time	10		0	ns	④
TELAX	Address Hold Time	50		30	ns	④
TDVWH	Data Setup Time	130		80	ns	④
TWHDX	Data Hold Time	0		0	ns	④
TWLSH	Chip Select Write Pulse Setup Time	160		100	ns	④
TWLEH	Chip Enable Write Pulse Setup Time	160		100	ns	④
TSLWH	Chip Select Write Pulse Hold Time	160		100	ns	④
TELWH	Chip Enable Write Pulse Hold Time	160		100	ns	④
TWLWH	Write Enable Pulse Width	160		100	ns	④
TELEL	Read or Write Cycle Time	450		250	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle


TAVEL
TELAX
VALID
TAVEL
NEXT
A
TEHEL
TELEH
TELEL
TEHEL
E
HIGH
W
D
TELQV
Q
PREVIOUS DATA
HIGH Z
VALID OUTPUT LATCHED
HIGH Z
TSHQZ
TSLQX
TSHQZ
S1,① S2
TIME REFERENCE
-1
0
1
2
3
4
5

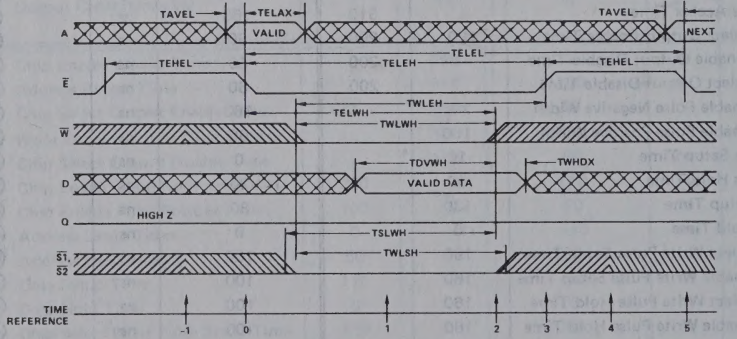
TRUTH TABLE

TIME REFERENCE	INPUTS E	S1①	W	A	D	OUTPUT Q	FUNCTION
-1	H	H	X	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	X	OUTPUT ENABLED
2	L	L	H	X	X	V	OUTPUT VALID
3	↗	L	H	X	X	V	OUTPUT LATCHED
4	H	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both S1 and S2 are low, and deselected if either S1 or S2 are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of E (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read S1, S2, and E must be low, W must be high. When E goes high the output data is latched into an on chip register. Taking either or both S1 or S2 high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking S1 and S2 low. On the falling edge of E the data will be unlatched.

Write Cycle


TAVEL
TELAX
VALID
TAVEL
NEXT
A
TEHEL
TELEH
TELEL
TEHEL
E
TWLEH
TELWH
TWLWH
W
TDVWH
TWHDX
D
VALID DATA
HIGH Z
Q
TSLWH
TWLSH
S1, S2
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS E	W	S①	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	V	Z	WRITE MODE HAS BEGUN
2	L	↗	L	X	V	Z	DATA IS WRITTEN
3	↗	X	X	X	X	Z	WRITE COMPLETED
4	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both S1 and S2 are low, and deselected if either S1 or S2 are high.

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse set-up time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

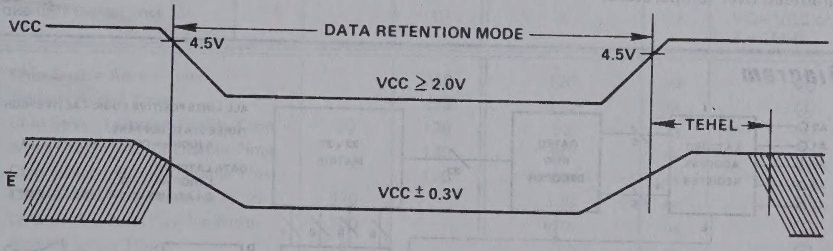
The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6551

256 x 4 CMOS RAM

Features

- LOW STANDBY POWER	50 µW MAX
- LOW OPERATING POWER	20mW/MHz MAX
- FAST ACCESS TIME	220nsec MAX
- DATA RETENTION VOLTAGE	2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT	
- HIGH OUTPUT DRVIE – 1 TTL LOAD	
- INTERNAL LATCHED CHIP SELECT	
- HIGH NOISE IMMUNITY	
- ON CHIP ADDRESS REGISTERS	
- LATCHED OUTPUTS	
- THREE STATE OUTPUTS	
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES	

Description

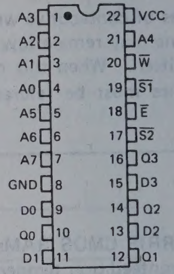
The HM-6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Pinout

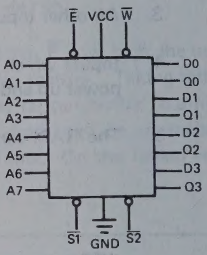
TOP VIEW



A3 1 · 22 VCC
A2 2 · 21 A4
A1 3 · 20 W̄
A0 4 · 19 S̄1
A5 5 · 18 Ē
A6 6 · 17 S̄2
A7 7 · 16 Q3
GND 8 · 15 D3
D0 9 · 14 Q2
Q0 10 · 13 D2
D1 11 · 12 Q1

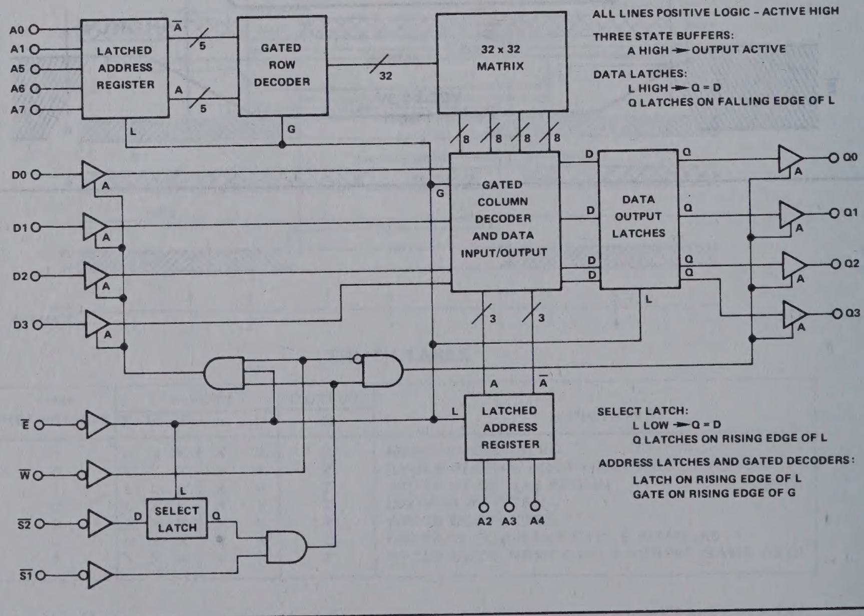
A – Address Input
Ē – Chip Enable
S̄ – Chip Select
W̄ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Ē
VCC
W̄
A0
A1
A2
A3
A4
A5
A6
A7
D0
Q0
D1
Q1
D2
Q2
D3
Q3
S̄1
GND
S̄2

Functional Diagram



A0
A1
A5
A6
A7
LATCHED ADDRESS REGISTER
Ā
A
5
5
GATED ROW DECODER
32
32 x 32 MATRIX
L
G
8
8
8
8
D0
D1
D2
D3
A
GATED COLUMN DECODER AND DATA INPUT/OUTPUT
DATA OUTPUT LATCHES
D
Q
L
Q0
Q1
Q2
Q3
3
3
A
Ā
LATCHED ADDRESS REGISTER
A2
A3
A4
Ē
W̄
S̄2
S̄1
SELECT LATCH
ALL LINES POSITIVE LOGIC - ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE
DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L
SELECT LATCH:
L LOW → Q = D
Q LATCHES ON RISING EDGE OF L
ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6551B-2/HM-6551B-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage - VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

LECTRICAL CHARACTERISTICS

C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
		MIN	MAX	TYPICAL		
ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz

C.

SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access Time		220	120	ns	④
TAVQV	Address Access Time		220	110	ns	④
TS1LQX	Chip Select 1 Output Enable Time	20	130	50	ns	④
TWLQZ	Write Enable Output Disable Time		130	50	ns	④
TS1HQZ	Chip Select 1 Output Disable Time		130	50	ns	④
TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
TAVEL	Address Setup Time	0		-10	ns	④
TS2LEL	Chip Select 2 Setup Time	0		-10	ns	④
TELAX	Address Hold Time	40		20	ns	④
TELS2X	Chip Select 2 Hold Time	40		20	ns	④
TDVWH	Data Setup Time	100		50	ns	④
TWHDX	Data Hold Time	0		0	ns	④
TWLS1H	Chip Select 1 Write Pulse Setup Time	120		60	ns	④
TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
TS1LWH	Chip Select 1 Write Pulse Hold Time	120		60	ns	④
TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
TWLWH	Write Enable Pulse Width	120		60	ns	④
TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6551-2/HM-6551-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -(VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		300	150	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	150	60	ns	④
	TWLQZ	Write Enable Output Disable Time		150	60	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		150	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TS2LEL	Chip Select 2 Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TELS2X	Chip Select 2 Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	150		100	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	180		120	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		120	ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	180		120	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		120	ns	④
	TWLWH	Write Enable Pulse Width	180		120	ns	④
	TELEL	Read or Write Cycle Time	400		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (GND +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
		MIN	MAX	TYPICAL		
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		100	1.0	μA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz

C.

TELQV	Chip Enable Access Time		350	200	ns	④
TAVQV	Address Access Time		360	200	ns	④
TS1LQX	Chip Select 1 Output Enable Time	20	180	80	ns	④
TWLQZ	Write Enable Output Disable Time		180	80	ns	④
TS1HQZ	Chip Select 1 Output Disable Time		180	80	ns	④
TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
TAVEL	Address Setup Time	10		0	ns	④
TS2LEL	Chip Select 2 Setup Time	10		0	ns	④
TELAX	Address Hold Time	70		40	ns	④
TELS2X	Chip Select 2 Hold Time	70		40	ns	④
TDVWH	Data Setup Time	170		120	ns	④
TWHDX	Data Hold Time	0		0	ns	④
TWLS1H	Chip Select 1 Write Pulse Setup Time	210		150	ns	④
TWLEH	Chip Enable Write Pulse Setup Time	210		150	ns	④
TS1LWH	Chip Select 1 Write Pulse Hold Time	210		150	ns	④
TELWH	Chip Enable Write Pulse Hold Time	210		150	ns	④
TWLWH	Write Enable Pulse Width	210		150	ns	④
TELEL	Read or Write Cycle Time	500		290	ns	④

NOTES:
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② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
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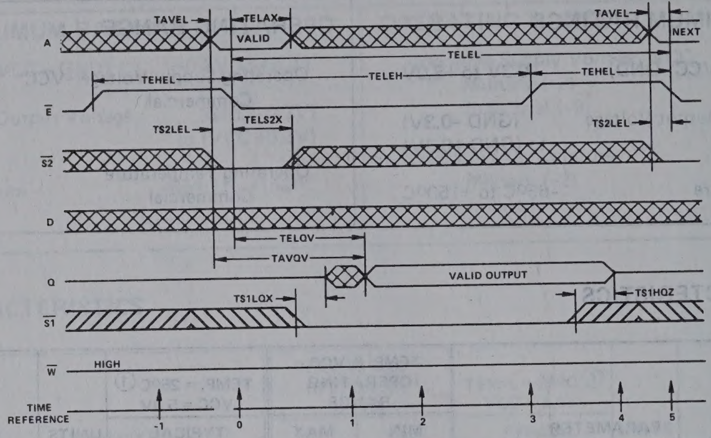
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle


TAVEL
TELAX
VALID
TAVEL
NEXT
A
TELEL
TEHEL
TELEH
TEHEL
E
TELS2X
TS2LEL
TS2LEL
S2
D
TELQV
TAVQV
Q
VALID OUTPUT
TS1LQX
TS1HQZ
S1
W
HIGH
TIME REFERENCE
-1
0
1
2
3
4
5

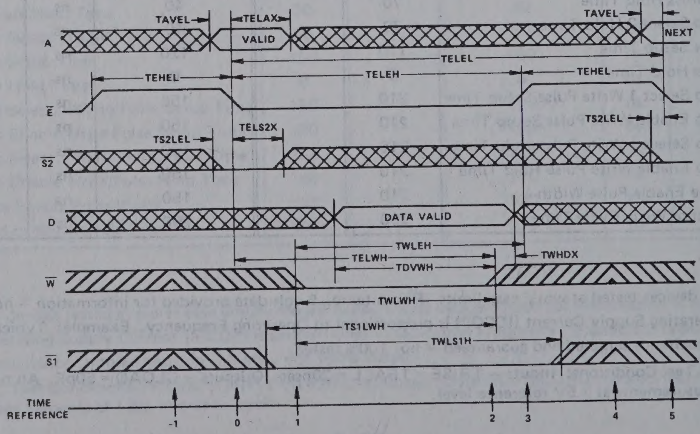
TRUTH TABLE

TIME REFERENCE	INPUTS E	INPUTS S1	INPUTS S2	INPUTS W	INPUTS A	INPUTS D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↓	X	L	H	V	X	Z	ADDRESSES AND S2 ARE LATCHED, CYCLE BEGINS
1	L	L	X	H	X	X	X	OUTPUT ENABLED BUT UNDEFINED
2	L	L	X	H	X	X	V	DATA OUTPUT VALID
3	↑	L	X	H	X	X	V	OUTPUTS LATCHED, VALID DATA, S2 UNLATCHES
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	L	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HM-6551 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing that minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HM-6551 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle


TAVEL
TELAX
VALID
TAVEL
NEXT
A
TELEL
TEHEL
TELEH
TEHEL
E
TS2LEL
TELS2X
TS2LEL
S2
D
DATA VALID
TWLEH
TELWH
TDVWH
TWHDX
W
TWLWH
TS1LWH
TWLS1H
S1
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	S2	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↓	X	L	X	V	X	Z	CYCLE BEGINS, ADDRESSES AND $\overline{S2}$ ARE LATCHED
1	L	L	X	↓	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↑	X	V	Z	DATA IN IS WRITTEN
3	↑	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	L	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH) various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

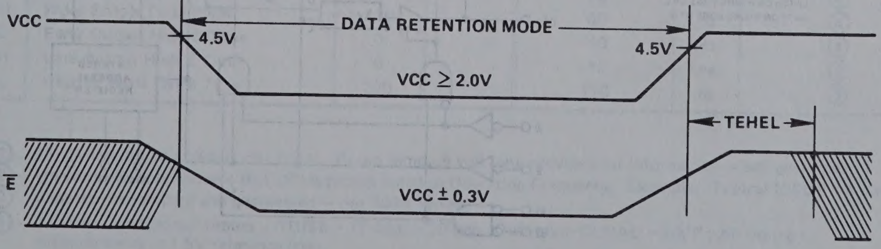
The HM-6551 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6561

256 x 4 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER 50µW MAX
- LOW OPERATING POWER 20 mW/MHz MAX
- FAST ACCESS TIME 220nsec MAX
- DATA RETENTION VOLTAGE 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 1 TTL LOAD
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

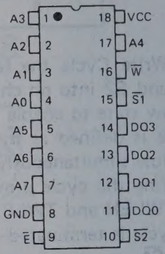
On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6561 is pin for pin replaceable with the HM-6661, a 256 x 4 CMOS PROM. This allows a single memory board design with any organization of RAM and PROMs.

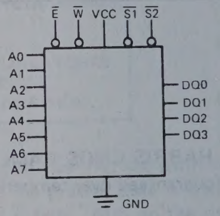
Pinout

TOP VIEW

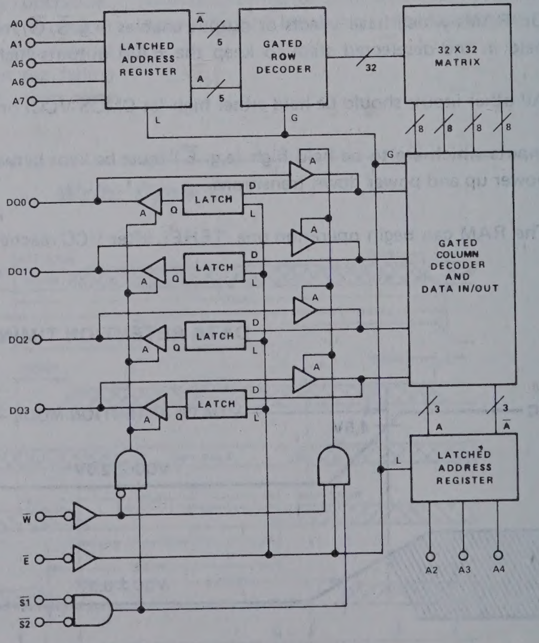

A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
$\overline{E}$ 9
18 VCC
17 A4
16 $\overline{W}$
15 $\overline{S1}$
14 DQ3
13 DQ2
12 DQ1
11 DQ0
10 $\overline{S2}$

A – Address Input
$\overline{E}$ – Chip Enable
$\overline{S}$ – Chip Select
$\overline{W}$ – Write Enable
DQ – Data In/Out

Logic Symbol


$\overline{E}$
$\overline{W}$
VCC
$\overline{S1}$
$\overline{S2}$
A0
A1
A2
A3
A4
A5
A6
A7
DQ0
DQ1
DQ2
DQ3
GND

Functional Diagram


A0
A1
A5
A6
A7
LATCHED ADDRESS REGISTER
$\overline{A}$
A
5
5
GATED ROW DECODER
32
32 X 32 MATRIX
8
8
8
8
L
G
G
A
D
LATCH
Q
L
DQ0
DQ1
DQ2
DQ3
GATED COLUMN DECODER AND DATA IN/OUT
3
3
A
$\overline{A}$
LATCHED ADDRESS REGISTER
L
$\overline{W}$
$\overline{E}$
$\overline{S1}$
$\overline{S2}$
A2
A3
A4

ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6561B-2/HM-6561B-9

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤VIO≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
.C.	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	50	ns	④
	TWLQZ	Write Enable Output Disable Time		120	50	ns	④
	TSHQZ	Chip Select Output Disable Time		120	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	120		50	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	120		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	120		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
	TWLWH	Write Enable Pulse Width	120		60	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

3

NOTES: ① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.

③ Capacitance sampled and guaranteed — not 100% tested.

④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6561-2/HM-6561-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC – GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		10	0.1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	µA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		300	150	ns	④
	TSLQX	Chip Select Output Enable Time	20	150	60	ns	④
	TWLQZ	Write Enable Output Disable Time		150	60	ns	④
	TSHQZ	Chip Select Output Disable Time		150	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	150		100	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	150		60	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	180		120	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		120	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	180		120	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		120	ns	④
	TWLWH	Write Enable Pulse Width	180		120	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	400		210	ns	④

NOTES: ① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.

③ Capacitance sampled and guaranteed — not 100% tested.

④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

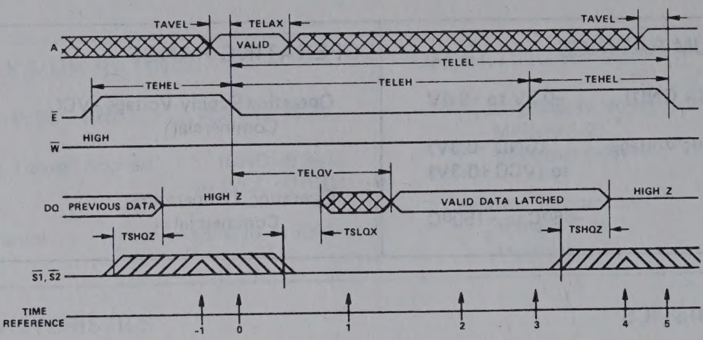
Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
		MIN	MAX	TYPICAL		
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		100	1	μA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0			V	
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
TELQV	Chip Enable Access Time		350	200	ns	④
TAVQV	Address Access Time		360	200	ns	④
TSLQX	Chip Select Output Enable Time	20	180	80	ns	④
TWLQZ	Write Enable Output Disable Time		180	80	ns	④
TSHQZ	Chip Select Output Disable Time		180	80	ns	④
TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
TAVEL	Address Setup Time	10		0	ns	④
TELAX	Address Hold Time	70		40	ns	④
TDVWH	Data Setup Time	170		120	ns	④
TWHDX	Data Hold Time	0		0	ns	④
TWLDV	Write Data Delay Time	200		60	ns	④
TWLSH	Chip Select Write Pulse Setup Time	210		150	ns	④
TWLEH	Chip Enable Write Pulse Setup Time	210		150	ns	④
TSLWH	Chip Select Write Pulse Hold Time	210		150	ns	④
TELWH	Chip Enable Write Pulse Hold Time	210		150	ns	④
TWLWH	Write Enable Pulse Width	210		150	ns	④
TWLSL	Early Output High Z Time	0		-10	ns	④
TSHWH	Late Output High Z Time	0		-10	ns	④
TELEL	Read or Write Cycle Time	500		290	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle


TAVEL
TELAX
TAVEL
A
VALID
TELEL
TEHEL
TELEH
TEHEL
E
HIGH
W
TELQV
DQ
PREVIOUS DATA
HIGH Z
VALID DATA LATCHED
HIGH Z
TSHQZ
TSLQX
TSHQZ
S1, S2
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

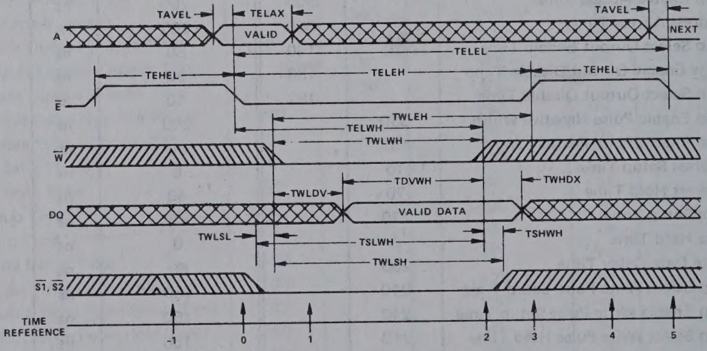
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↘	X	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	OUTPUT ENABLED
2	L	L	H	X	V	OUTPUT VALID
3	↗	L	H	X	V	OUTPUT LATCHED
4	H	H	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle


TAVEL
TELAX
TAVEL
A
VALID
NEXT
TELEL
TEHEL
TELEH
TEHEL
E
TWLEH
TELWH
TWLWH
W
TDVWH
TWHDX
TWLDV
DQ
VALID DATA
TWLSL
TSLWH
TSHWH
TWLSH
S1, S2
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	H	X	X	X	MEMORY DISABLED
0	↘	X	X	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	X	WRITE PERIOD BEGINS
2	L	L	↗	X	V	DATA IN IS WRITTEN
3	↗	X	H	X	X	WRITE IS COMPLETED
4	H	H	X	X	X	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	X	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ fall before $\overline{W}$ falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL and TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ falls before both $\overline{S1}$ and $\overline{S2}$ fall.

If one or both selects are high until $\overline{W}$ falls the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable, reading the data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
Case 1	Both $\overline{S1}$ and $\overline{S2}$ = low before $\overline{W}$ = low	TWLQZ TWLDV TDVWH	TWLWH TWLSL TSHWH
Case 2	$\overline{W}$ = low before both $\overline{S1}$ and $\overline{S2}$ = low	TWLWH TDVWH TWLSL TSHWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

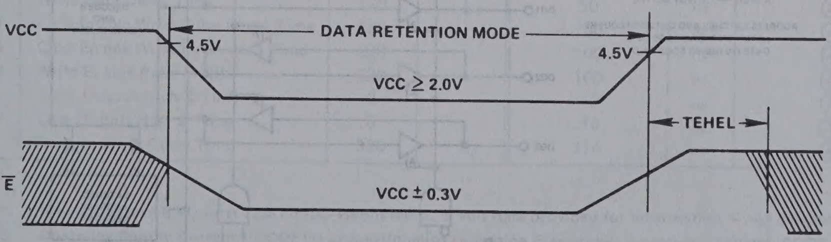
Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact, data may be modified as many times as desired with $\overline{E}$ remaining low.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6562
256 x 4 CMOS RAM

NOT RECOMMENDED FOR NEW DESIGNS SEE HM-6561

Features

LOW POWER STANDBY	50 μW MAX
LOW POWER OPERATION	20mW/MHz MAX
FAST ACCESS TIME	220nsec MAX
DATA RETENTION VOLTAGE	2.0 VOLTS MIN
TTL COMPATIBLE IN/OUT	
HIGH OUTPUT DRIVE – 1 TTL LOAD	
HIGH NOISE IMMUNITY	
ON CHIP ADDRESS REGISTER	
16 PIN PACKAGE FOR HIGH DENSITY	
THREE-STATE OUTPUTS	
MILITARY TEMPERATURE RANGE	
INDUSTRIAL TEMPERATURE RANGE	

Description

The HM-6562 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

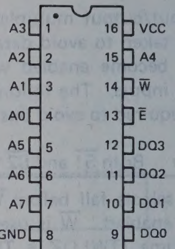
On chip latches are provided for address allowing for efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6562 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6611, 256 x 4 CMOS PROM, is pin for pin replaceable with the HM-6562. This allows a single memory board design with any organization of RAM and PROMs.

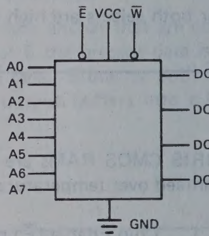
Pinout

TOP VIEW

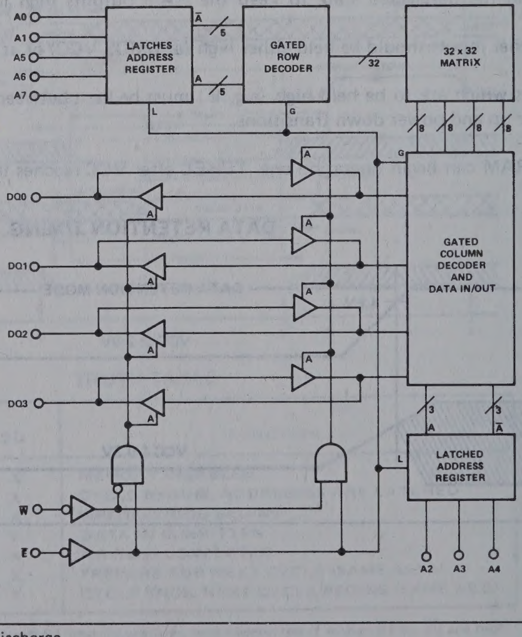

A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
16 VCC
15 A4
14 W̄
13 Ē
12 DQ3
11 DQ2
10 DQ1
9 DQ0

A – Address Input
Ē – Chip Enable
W̄ – Write Enable
DQ – Data In/Out

Logic Symbol


Ē
VCC
W̄
A0
A1
A2
A3
A4
A5
A6
A7
DQ0
DQ1
DQ2
DQ3
GND

Functional Diagram


A0
A1
A5
A6
A7
LATCHES ADDRESS REGISTER
Ā
A
5
5
L
GATED ROW DECODER
G
32
32 x 32 MATRIX
8
8
8
8
G
GATED COLUMN DECODER AND DATA IN/OUT
DQ0
DQ1
DQ2
DQ3
A
3
3
A
Ā
L
LATCHED ADDRESS REGISTER
W̄
Ē
A2
A3
A4

ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6562B-2/HM-6562B-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

LECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
C.	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VI ⩽ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽VIO⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TELQX	Chip Enable Output Enable Time	20	120	50	ns	④
	TWLQZ	Write Enable Output Disable Time		120	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		120	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
C.	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	120		50	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	220		100	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		100	ns	④
	TWLWH	Write Enable Pulse Width	220		100	ns	④
	TWLEL	Early Output High Z Time	0		-10	ns	④
	TEHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:

1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Specifications HM-6562-2/HM-6562-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽ VI ⩽ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	0.0	μA	GND ⩽VIO⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10	6	pF	VIO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	160	ns	④
	TAVQV	Address Access Time		300	150	ns	④
	TELQX	Chip Enable Output Enable Time	20	150	60	ns	④
	TWLQZ	Write Enable Output Disable Time		150	60	ns	④
	TEHQZ	Chip Enable Output Disable Time		150	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		160	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	50		30	ns	④
	TDVWH	Data Setup Time	150		100	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	150		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	300		160	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		160	ns	④
	TWLWH	Write Enable Pulse Width	300		160	ns	④
	TWLEL	Early Output High Z Time	0		-10	ns	④
	TEHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	400		210	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage -VCC Commercial	4.5V to 5.5V
Operating Temperature Commercial	0°C to 75°C

LECTRICAL CHARACTERISTICS

C.

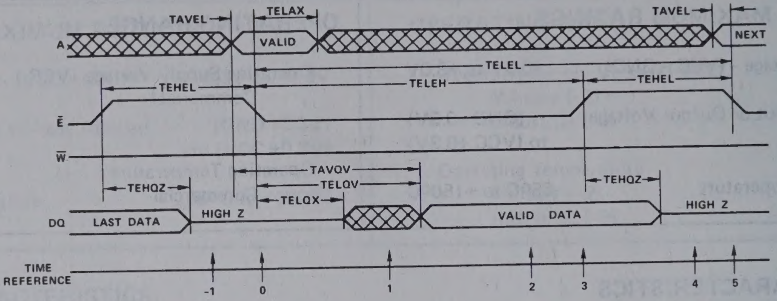
SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		100	1.0	μA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0			V	
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
IIOZ	Input Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VIO ≤ VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.0	V	
VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.5	V	IO = -0.2mA
CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
CIO	Input Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz

C.

SYMBOL	PARAMETER	MIN	MAX	TYPICAL	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access Time		350	200	ns	④
TAVQV	Address Access Time		360	200	ns	④
TELQX	Chip Enable Output Enable Time	20	180	80	ns	④
TWLQZ	Write Enable Output Disable Time		180	80	ns	④
TEHQZ	Chip Enable Output Disable Time		180	80	ns	④
TELEH	Chip Enable Pulse Negative Width	350		200	ns	④
TEHEL	Chip Enable Pulse Positive Width	150		90	ns	④
TAVEL	Address Setup Time	10		0	ns	④
TELAX	Address Hold Time	70		40	ns	④
TDVWH	Data Setup Time	170		120	ns	④
TWHDX	Data Hold Time	0		0	ns	④
TWLDV	Write Data Delay Time	180		80	ns	④
TWLEH	Chip Enable Write Pulse Setup Time	350		200	ns	④
TELWH	Chip Enable Write Pulse Hold Time	350		200	ns	④
TWLWH	Write Enable Pulse Width	350		200	ns	④
TWLEL	Early Output High Z Time	0		-10	ns	④
TEHWH	Late Output High Z Time	0		-10	ns	④
TELEL	Read or Write Cycle Time	500		290	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

Read Cycle


TAVEL
TELAX
TAVEL
A
VALID
NEXT
TELEL
TEHEL
TELEH
TEHEL
Ē
W̄
TAVQV
TELQV
TEHQZ
TELQX
TEHQZ
DQ
LAST DATA
HIGH Z
VALID DATA
HIGH Z
TIME REFERENCE
-1
0
1
2
3
4
5

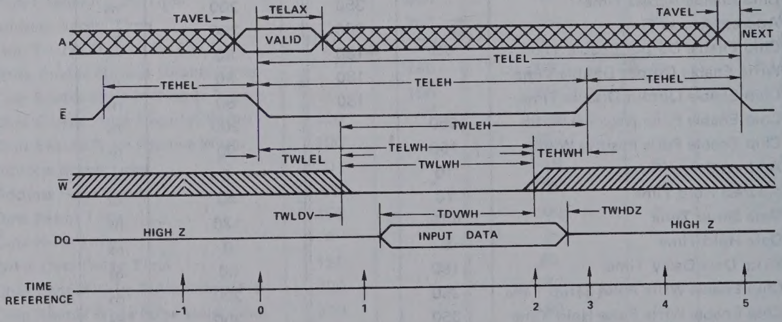
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	OUTPUT DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↑	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HM-6562 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data, $\overline{E}$ must be low and $\overline{W}$ should be high. The output data will be valid at access time.

$\overline{E}$ may be used to force the output buffers into a high impedance state.

Write Cycle


TAVEL
TELAX
TAVEL
A
VALID
NEXT
TELEL
TEHEL
TELEH
TEHEL
Ē
TWLEH
TELWH
TEHWH
TWLEL
TWLWH
W̄
TWLDV
TDVWH
TWHDZ
DQ
HIGH Z
INPUT DATA
HIGH Z
TIME REFERENCE
-1
0
1
2
3
4
5

TIME REFERENCE	INPUTS $\overline{E}$	INPUTS $\overline{W}$	INPUTS A	INPUTS DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↓	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↑	X	V	INPUT DATA IS WRITTEN
3	↑	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TLWDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before E. The RAM outputs will disable (three-state) after E rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

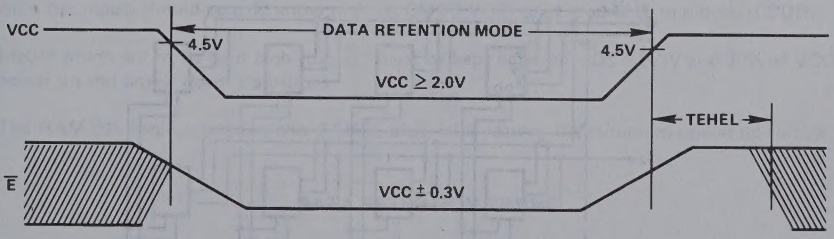
If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM5-6564

8K x 8, 16K x 4 CMOS RAM

Features

- LOW POWER STANDBY	4mW MAX
- LOW POWER OPERATION	280mW/MHz MAX
- DATA RETENTION	2.0V MIN
- TTL COMPATIBLE IN/OUT	
- THREE STATE OUTPUTS	
- FAST ACCESS TIME	350ns MAX
- FULL MILITARY TEMPERATURE AVAILABLE	-55°C to 125°C
- INDUSTRIAL TEMPERATURE STANDARD	-40°C to 85°C
- COMMERCIAL TEMPERATURE AVAILABLE	0°C to 75°C
- ON CHIP ADDRESS REGISTERS	
- ORGANIZABLE 8K x 8 or 16K x 4	
- 40 PIN DIP PINOUT - 2.000" x 0.900"	

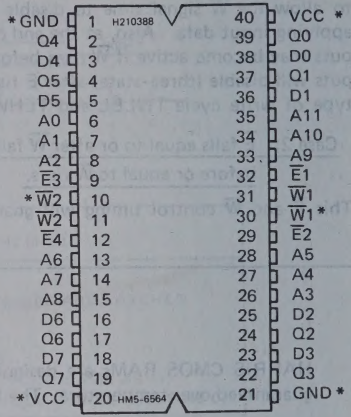
Description

The HM-6564 is a 64K bit CMOS RAM. It consists of 16 HM4-6504 4K x 1 CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HM-6564 is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HM-6564 RAM as either an 8K by 8 or a 16K by 4 array. The HM-6564 also contains decoupling capacitors to reduce noise and to minimize the need for additional external decoupling.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HM-6564 is intended for use in any application where a large amount of RAM is needed, and where power consumption and board space are prime concerns. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board. Example applications include digital avionic instrumentation, remote data acquisition, and portable or hand held digital communications devices.

Pinout

TOP VIEW



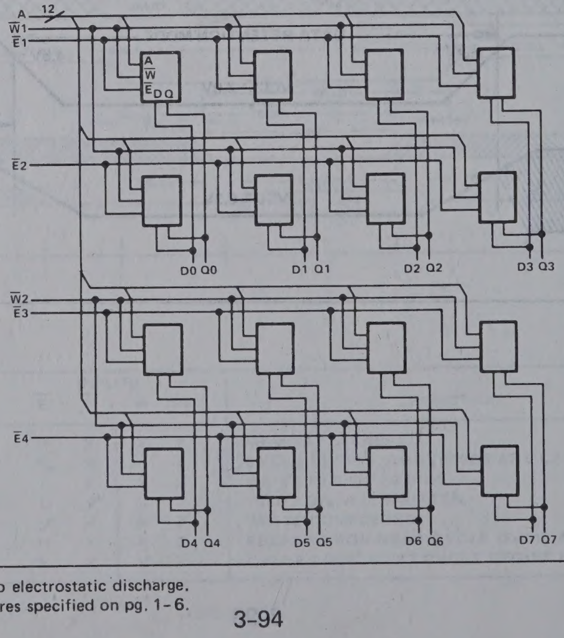
*GND	1	40	VCC *
Q4	2	39	Q0
D4	3	38	D0
Q5	4	37	Q1
D5	5	36	D1
A0	6	35	A11
A1	7	34	A10
A2	8	33	A9
$\overline{E}3$	9	32	$\overline{E}1$
*$\overline{W}2$	10	31	$\overline{W}1$
$\overline{W}2$	11	30	$\overline{W}1$ *
$\overline{E}4$	12	29	$\overline{E}2$
A6	13	28	A5
A7	14	27	A4
A8	15	26	A3
D6	16	25	D2
Q6	17	24	Q2
D7	18	23	D3
Q7	19	22	Q3
*VCC	20	21	GND *

*NOTES:

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Organization Guide

To Organize 8K x 8:

Connect:	$\overline{\mathrm{E}}$1 with $\overline{\mathrm{E}}$3	(Pins 9 + 32)
	$\overline{\mathrm{E}}$2 with $\overline{\mathrm{E}}$4	(Pins 12 + 29)
	$\overline{\mathrm{W}}$1 with $\overline{\mathrm{W}}$2	(Pins 11 +31)

To Organize 16K x 4:

Connect:	Q0 with Q4	(Pins 2 + 39)
	D0 with D4	(Pins 3 + 38)
	Q1 with Q5	(Pins 4 + 37)
	D1 with D5	(Pins 5 + 36)
	D2 with D6	(Pins 16 +25)
	Q2 with Q6	(Pins 17 + 24)
	D3 with D7	(Pins 18 + 23)
	Q3 with Q7	(Pins 19 + 22)
Optional	$\overline{\mathrm{W}}$1 may be common with $\overline{\mathrm{W}}$2	(Pins 11 + 31)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{\mathrm{E}}$1 and $\overline{\mathrm{E}}$2. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

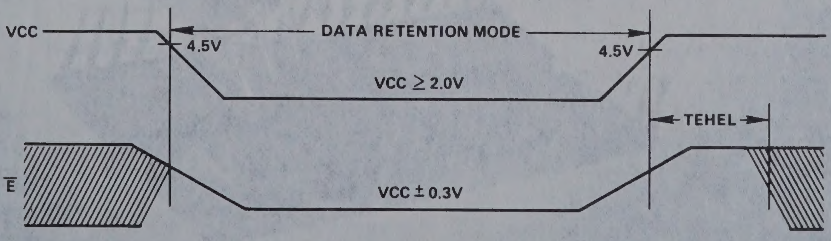
The leadless chip carrier packages used in the HM-6564 have conductive lids. These lids are electrically floating, not connected to VCC or GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{\mathrm{E}}$) must be held high during data retention; within VCC + 0.3V to VCC - 0.3V.
2. On RAMs which have selects or output enables (e.g. $\overline{\mathrm{S}}$, $\overline{\mathrm{G}}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{\mathrm{E}}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Board Size Tradeoffs

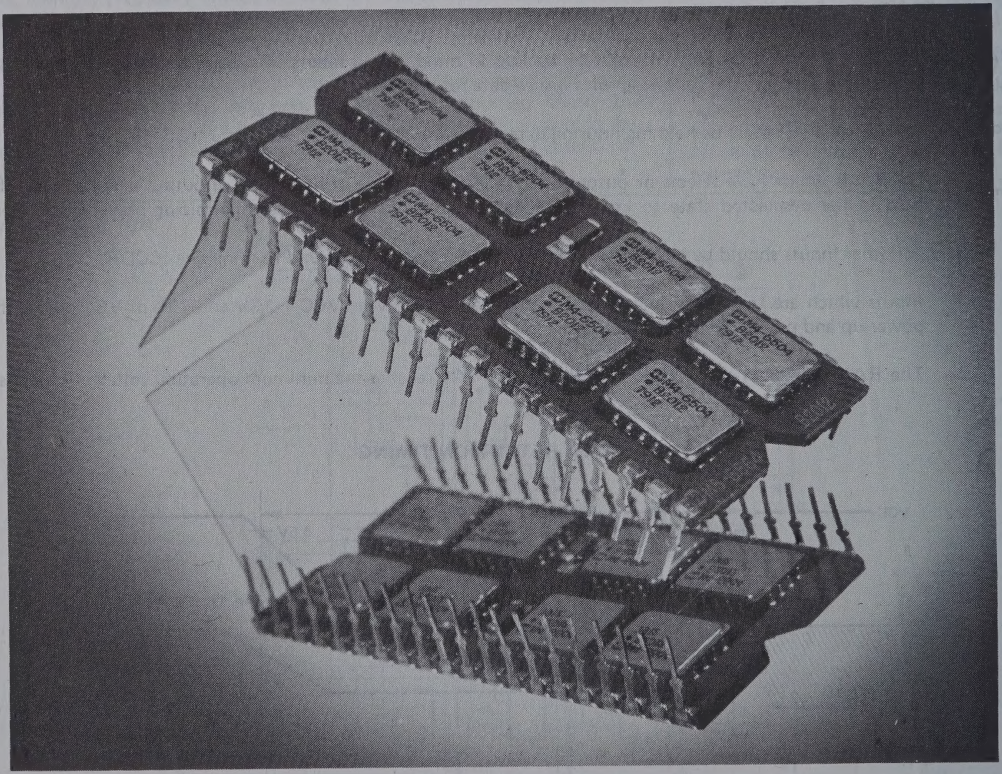
Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HM5-6564 RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OF 16 4K RAMs ON A PC BOARD V.S. THE HM5-6564

PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 sq. in.
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 sq. in.
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 sq. in.
HM5-6564	Two Sided Mounting Multilayer Alumina Substrate	2 sq. in.

The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local Harris office or sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.



HM5-6564 — 64K BIT CMOS RAM

Specifications HM5-6564-9 and HM5-6564-2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	+4.5V to +5.5V
Operating Temperature	
Industrial (-9)	-40°C to +85°C
Military (-2)	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		800	50	μA	IO = 0 VI = VCC or GND
ICCOP1	Operating Supply Current (8K x 8) ②		56	40	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCOP2	Operating Supply Current (16K x 4) ②		28	20	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		800	25	μA	IO = 0, VCC = 2.0, VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
IIA	Address Input Leakage	-20	+20	1	μA	GND⩽VI⩽VCC
IID1	Data Input Leakage (8K x 8)	-3	+3	.1	μA	GND⩽VI⩽VCC
IID2	Data Input Leakage (16K x 4)	-5	+5	.2	μA	GND⩽VI⩽VCC
IIE1	Enable Input Leakage (8K x 8)	-10	+10	.5	μA	GND⩽VI⩽VCC
IIE2	Enable Input Leakage (16K x 4)	-5	+5	.2	μA	GND⩽VI⩽VCC
IIW	Write Enable Input Leakage (Each)	-10	+10	.5	μA	GND⩽VI⩽VCC
IOZ1	Output Leakage (8K x 8)	-5	+5	.4	μA	GND⩽VO⩽VCC
IOZ2	Output Leakage (16K x 4)	-10	+10	1	μA	GND⩽VO⩽VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	2.0	V	
VOL	Output Low Voltage		0.4	.25	V	IO = 2.0mA
VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
CIA	Address Input Capacitance ③		200	170	pF	f = 1MHz, VI = VCC or GND
CID1	Data Input Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VI = VCC or GND
CID2	Data Input Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VI = VCC or GND
CIE1	Enable Input Capacitance (8K x 8) ③		160	100	pF	f = 1MHz, VI = VCC or GND
CIE2	Enable Input Capacitance (16K x 4) ③		80	50	pF	f = 1MHz, VI = VCC or GND
CIW	Write Enable Input Capacitance (Each) ③		100	80	pF	f = 1MHz, VI = VCC or GND
CO1	Output Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VO = VCC or GND
CO2	Output Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VO = VCC or GND
CVCC	Decoupling Capacitance	.25		.33	μF	f = 1MHz

NOTES:

① Each individual RAM in the leadless carrier is fully tested at worst case limits of temperature and voltage. The complete assembled HM-6564 array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed - not 100% tested.

ELECTRICAL CHARACTERISTICS

A.C.

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V			UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX		
TELQV	Chip Enable Access		350		250	300	ns	④
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		400		270	350	ns	④
TELQX	Output Enable	20	120		50	100	ns	④
TEHQZ	Output Disable		120		50	100	ns	④
TELEL	Read or Write Cycle	480		410	320		ns	④
TELEH	Chip Enable Low	350		300	250		ns	④
TEHEL	Chip Enable High	130		110	70		ns	④
TAVEL	Address Setup	50		50	20		ns	④
TELAX	Address Hold	50		50	20		ns	④
TWLWH	Write Enable Low	150		130	100		ns	④
TWLEH	Write Enable Setup	250		220	170		ns	④
TWLEL	Early Write Setup (Write Mode)	10		10	0		ns	④
TWHEL	Write Enable Read Setup	10		10	0		ns	④
TELWX	Early Write Hold (Write Mode)	100		100	70		ns	④
TDVWL	Data Setup	10		10	0		ns	④
TDVEL	Early Write Data Setup	10		10	0		ns	④
TWLDX	Data Hold	100		100	70		ns	④
TELDX	Early Write Data Hold	100		100	70		ns	④
TQVWL	Data Valid to Write (Read-Modify-Write)	0		0	0		ns	④

NOTES:

④ AC Test Conditions:

Inputs - Trise = Tfall ≤ 20ns.
Outputs - CLOAD = 100pF.
Timing measured at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE	
Operating Supply Voltage Commercial	+4.5V to +5.5V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C VCC = 5.0V ①	UNITS	TEST CONDITIONS
		MIN	MAX	TYPICAL		
ICCSB	Standby Supply Current		4.0	1.0	mA	IO = 0, VI = VCC or GND
ICCOP1	Operating Supply Current (8K x 8) ②		60	45	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCOP2	Operating Supply Current (16K x 4) ②		30	23	mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Curr.		4.0	0.1	mA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply V.	2.0		1.4	V	
IIA	Address Input Leakage	-20	+20	1	μA	GND≤VI≤VCC
IID1	Data Input Leakage (8K x 8)	-3	+3	.1	μA	GND≤VI≤VCC
IID2	Data Input Leakage (16K x 4)	-5	+5	.2	μA	GND≤VI≤VCC
IIE1	Enable Input Leakage (8K x 8)	-10	+10	.5	μA	GND≤VI≤VCC
IIE2	Enable Input Leakage (16K x 4)	-5	+5	.2	μA	GND≤VI≤VCC
IIW	Write Enable Input Leakage (Each)	-10	+10	.5	μA	GND≤VI≤VCC
IOZ1	Output Leakage (8K x 8)	-5	+5	.4	μA	GND≤VO≤VCC
IOZ2	Output Leakage (16K x 4)	-10	+10	1	μA	GND≤VO≤VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	.25	V	IO = 1.6mA
VOH	Output High Voltage	2.4		4.0	V	IO = -0.4mA
CIA	Address Input Capacitance ③		200	170	pF	f = 1MHz, VI = VCC or GND
CID1	Data Input Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VI = VCC or GND
CID2	Data Input Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VI = VCC or GND
CIE1	Enable Input Capacitance (8K x 8) ③		160	100	pF	f = 1MHz, VI = VCC or GND
CIE2	Enable Input Capacitance (16K x 4) ③		80	50	pF	f = 1MHz, VI = VCC or GND
CIW	Write Input Capacitance (Each) ③		100	80	pF	f = 1MHz, VI = VCC or GND
CO1	Output Capacitance (8K x 8) ③		50	30	pF	f = 1MHz, VO = VCC or GND
CO2	Output Capacitance (16K x 4) ③		100	60	pF	f = 1MHz, VO = VCC or GND
CVCC	Decoupling Capacitance	.25		.33	μF	f = 1MHz

NOTES:

① Each individual RAM in the leadless carrier is fully tested at worst case limits of temperature and voltage. The complete assembled HM-6564 array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed - not 100% tested.

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C VCC = 5.0V ①	UNITS	TEST CONDTIONS
			MIN	MAX	TYPICAL		
A.C.	TELQV	Chip Enable Access		450	350	ns	④
	TAVQV	Address Access (TAVQV=TELQV+TAVEL)		500	390	ns	④
	TELQX	Output Enable	20	150	80	ns	④
	TEHQZ	Output Disable		150	80	ns	④
	TELEL	Read or Write Cycle	600		450	ns	④
	TELEH	Chip Enable Low	450		350	ns	④
	TEHEL	Chip Enable High	150		100	ns	④
	TAVEL	Address Setup	50		20	ns	④
	TELAX	Address Hold	50		20	ns	④
	TWLWH	Write Enable Low	150		100	ns	④
	TWLEH	Write Enable Setup	250		170	ns	④
	TWLEL	Early Write Setup (Write Mode)	10		0	ns	④
	TWHEL	Write Enable Read Setup	10		0	ns	④
	TELWX	Early Write Hold (Write Mode)	100		70	ns	④
	TDVWL	Data Setup	10		0	ns	④
	TDVEL	Early Write Data Setup	10		0	ns	④
	TWLDX	Data Hold	100		70	ns	④
	TELDX	Early Write Data Hold	100		70	ns	④
	TQVWL	Data Valid to Write (Ready-Modify-Write)	0		0	ns	④

NOTES:

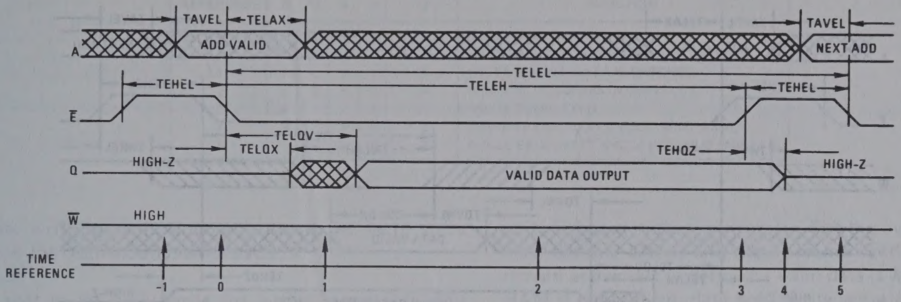
④ AC Test Conditions:

Inputs — Trise = Tfall ≤ 20ns.

Outputs — CLOAD = 100pF.

Timing measured at 1.5V reference level.

Read Cycle

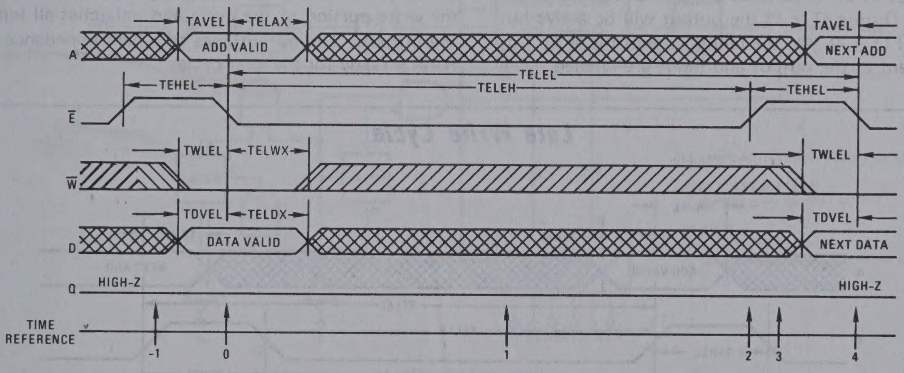

TAVEL
TELAX
TAVEL
A
ADD VALID
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
E
TELQV
TELQX
TEHQZ
Q
HIGH-Z
VALID DATA OUTPUT
HIGH-Z
W
HIGH
TIME REFERENCE
-1
0
1
2
3
4
5

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

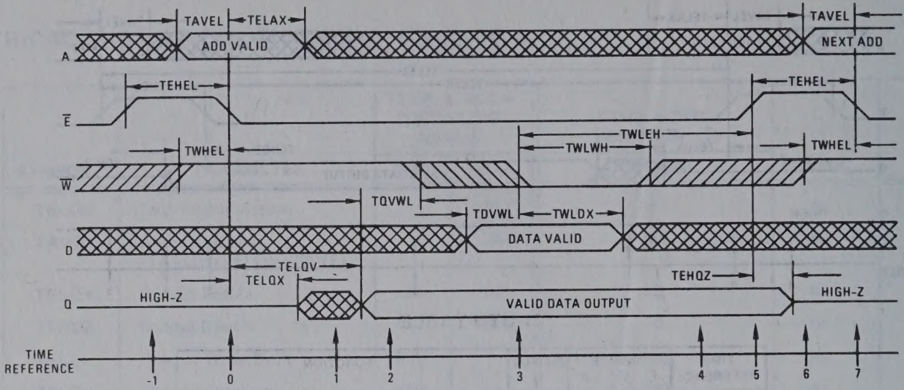

TAVEL
TELAX
TAVEL
A
ADD VALID
NEXT ADD
TELEL
TEHEL
TELEH
TEHEL
E
TWLEL
TELWX
TWLEL
W
TDVEL
TELDX
TDVEL
D
DATA VALID
NEXT DATA
Q
HIGH-Z
HIGH-Z
TIME REFERENCE
-1
0
1
2
3
4

TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle

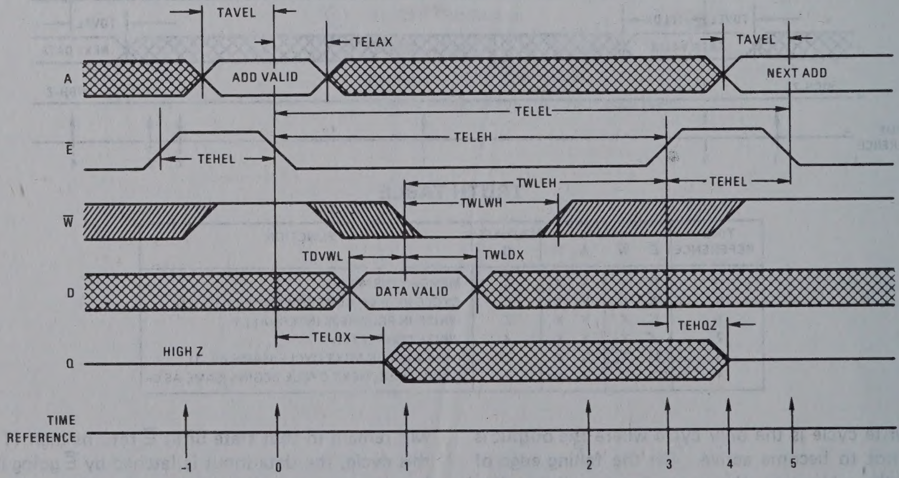

TAVEL
TELAX
TAVEL
A
ADD VALID
NEXT ADD
TEHEL
TEHEL
Ē
TWLEH
TWHEL
TWLWH
TWHEL
W̄
TQVWL
TDVWL
TWLDX
D
DATA VALID
TELQV
TELQX
TEHQZ
Q
HIGH-Z
VALID DATA OUTPUT
HIGH-Z
TIME REFERENCE
-1
0
1
2
3
4
5
6
7

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T= 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and the output. The output goes to a high impedance and the RAM is ready for the next cycle.

Late Write Cycle


TAVEL
TELAX
TAVEL
A
ADD VALID
NEXT ADD
TELEL
TELEH
Ē
TEHEL
TWLEH
TEHEL
TWLWH
W̄
TDVWL
TWLDX
D
DATA VALID
TEHQZ
TELQX
Q
HIGH Z
TIME REFERENCE
-1
0
1
2
3
4
5

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↓	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↑	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

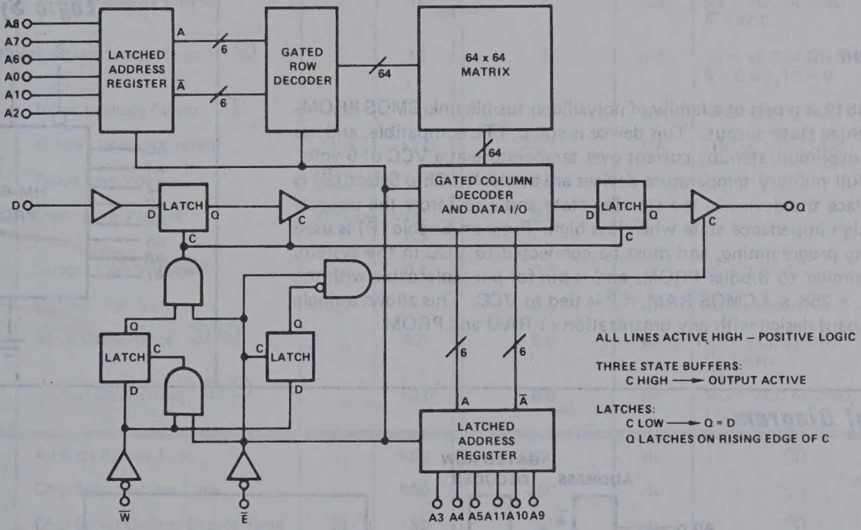
The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

HM-6504 (One of Sixteen)


A8
A7
A6
A0
A1
A2
LATCHED ADDRESS REGISTER
A
Ā
6
6
GATED ROW DECODER
64
64 x 64 MATRIX
64
GATED COLUMN DECODER AND DATA I/O
D
LATCH
D
Q
C
C
LATCH
D
Q
C
C
Q
LATCH
Q
C
D
LATCH
C
Q
D
W̄
Ē
6
6
A
Ā
LATCHED ADDRESS REGISTER
A3 A4 A5 A11 A10 A9
ALL LINES ACTIVE HIGH – POSITIVE LOGIC
THREE STATE BUFFERS:
C HIGH → OUTPUT ACTIVE
LATCHES:
C LOW → Q = D
Q LATCHES ON RISING EDGE OF C

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

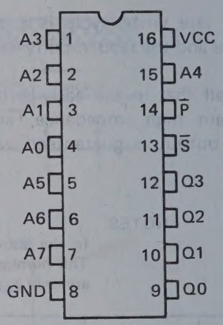
HM-6611
1024-BIT FIELD PROGRAMMABLE CMOS PROM

Features

- FUSED LINK PROM
- FIELD-PROGRAMMABLE
- ORGANIZED 256 x 4
- LOW POWER STANDBY 500 μW MAX.
- LOW POWER ENABLED 50 mW MAX.
- CMOS RAM PINOUT EXCEPT FOR $\overline{P}$
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FULLY STATIC OPERATION
- FAST ACCESS TIME 450nsec MAX
- HIGH NOISE IMMUNITY
- HIGH RELIABILITY
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- COMMERCIAL TEMPERATURE RANGE

Pinout

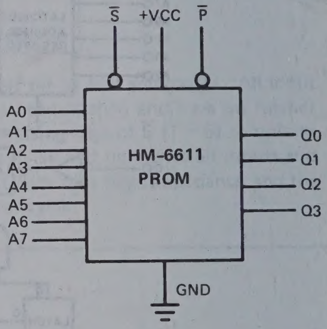
TOP VIEW


A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
16 VCC
15 A4
14 $\overline{P}$
13 $\overline{S}$
12 Q3
11 Q2
10 Q1
9 Q0

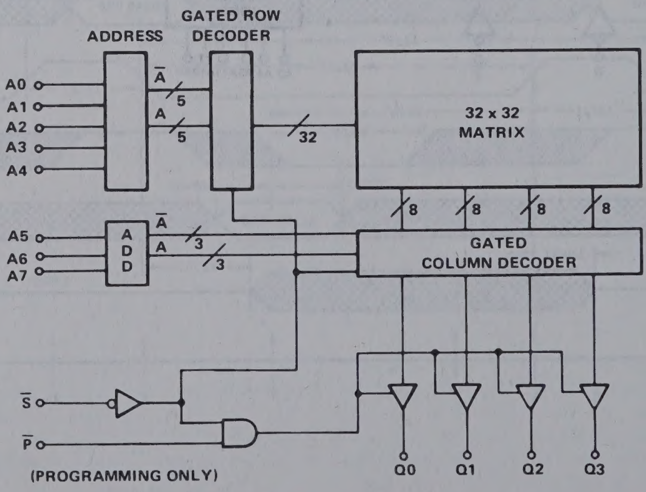
Description

The HM-6611 is a part of a family of polysilicon fusible link CMOS PROMs featuring three state outputs. This device is static, TTL compatible, and has a 100 μA maximum standby current over temperature at a VCC of 5 volts. 10V and full military temperature devices are available. Chip Select ($\overline{S}$) is used to place the device in the standby state and also forces the outputs into the high impedance state when it is high. Program Enable ($\overline{P}$) is used only during programming, and must be connected to VCC in the system. Pinout is similar to Bipolar PROMs and is pin for pin replaceable with the HM-6562, a 256 x 4 CMOS RAM, if $\overline{P}$ is tied to VCC. This allows a single memory board design with any organization of RAM and PROM.

Logic Symbol


$\overline{S}$
+VCC
$\overline{P}$
A0
A1
A2
A3
A4
A5
A6
A7
HM-6611
PROM
Q0
Q1
Q2
Q3
GND

Functional Diagram


ADDRESS
GATED ROW DECODER
A0
A1
A2
A3
A4
$\overline{A}$
A
5
5
32
32 x 32 MATRIX
8
8
8
8
A5
A6
A7
ADD
$\overline{A}$
A
3
3
GATED COLUMN DECODER
$\overline{S}$
$\overline{P}$
(PROGRAMMING ONLY)
Q0
Q1
Q2
Q3

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6611-2/HM-6611-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC – GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage –VCC

Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V

Operating Temperature

Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	5	μA	VI = VCC or GND $\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		10	2	mA	VI = VCC or GND $\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-1.0	+1.0	0.0	μA	GND⩽VI⩽VCC
	IOZ	Output Leakage Current	-1.0	+1.0	±0.1	μA	GND⩽VO⩽VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC – 2.0	VCC + 0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.3	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = –1.0mA
	CI	Input Capacitance ③ ④		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0	6.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		450	300	ns	⑤
	TSLQV	Chip Select Access Time		500	350	ns	⑤
	TSLQX	Chip Select Output Enable Time	20	150	50	ns	⑤
	TSHQZ	Chip Select Output Disable Time		150	50	ns	⑤

NOTES:

① All devices tested at worst case limits. Room temperature 5 volt data provided for information – not guaranteed.

② ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.

③ Except $\overline{P}$. Program Enable is used only during programming and its characteristics are accounted for in the programming specifications.

④ Capacitance is sampled and guaranteed, but not 100% tested.

⑤ AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – CLOAD = 50pF; Timing measured at 1.5V reference level.

Specifications HM-6611-5

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC Commercial	4.5 to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		① TEMP. = 25°C VCC = 5.0V	UNITS	TEST CONDITIONS
			MIN	MAX	TYPICAL		
D.C.	ICCSB	Standby Supply Current		1.0	0.2	mA	VI = VCC or GND $\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		20	5	mA	VI = VCC or GND $\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-5.0	+5.0	±0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	±0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC - 2.0	VCC + 0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.3	V	IO = 1.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.5mA
	CI	Input Capacitance ③ ④		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0	6.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		650	400	ns	⑤
	TSLQV	Chip Select Access Time		800	500	ns	⑤
	TSLQX	Chip Select Output Enable Time	20	200	50	ns	⑤
	TSHQZ	Chip Select Output Disable Time		200	50	ns	⑤

NOTES:

① All devices tested at worst case limits. Room temperature 5 volt data provided for information - not guaranteed.

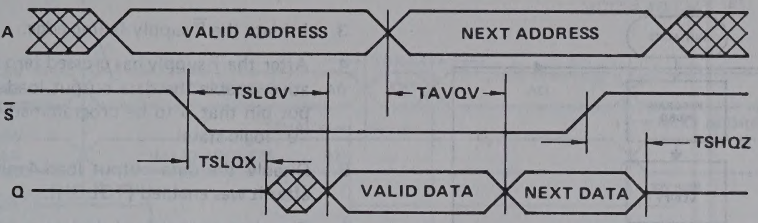
② ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.

③ Except $\overline{P}$. Program Enable is used only during programming and its characteristics are accounted for in the programming specifications.

④ Capacitance is sampled and guaranteed, but not 100% tested.

⑤ AC test conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - CLOAD = 50pF; Timing measured at 1.5V reference level.

Read Cycle



TRUTH TABLE

INPUTS S̄	 A	OUTPUT Q	FUNCTION
H	X	Z	DEVICE DESELECTED, OUTPUT HIGH IMPEDANCE
L	V	V	DEVICE SELECTED, DATA OUTPUT VALID FOR ADDRESS PRESENT

The timing waveforms shown describe only one possible method of operation. The device will output valid data corresponding to the address input one chip select access time (TSLQV) after it is selected. If the device is already selected and the address is changed to a new valid address the corresponding data will be available at the outputs no later than one address access time (TAVQV) later. Thus, this device can be selected each time a data word is desired, or it can be left selected to access a number of data words. If the system data bus allows, the device may be permanently selected for ease of use.

Programming

BACKGROUND INFORMATION

The HM-6611 is a 256 x 4 CMOS Programmable Read-Only Memory. It is programmed by the controlled application of programming pulses to selected memory cells. These pulses permanently alter the logic state of the memory cell. The memory array is manufactured with each cell set to the high or "1" logic state. The user may select any memory cell and permanently change its logic state to a "0" or low by programming.

Programming is accomplished by addressing the word to be programmed, applying the programming pulses, and verifying the data programmed. The verification is performed at high voltage (VCC) during the programming sequence, and at low voltage after all programming is completed.

PROGRAMMING SYSTEM CHARACTERISTICS:

1. Power source for the device to be programmed (VCC) variable from +3.0 to +11.0 volts, current capability of 500mA average and 1 amp dynamic currents.
2. Programming power supply is a negative 20.0V supply (±1.0V), switchable between -20V, 0V, +3.5V, and +10.5V. This supply must be able to deliver 400 mA average, and 1A peak currents at -20V. Less than 1mA output current is required at 0V, +3.5V, and at +10.5V. The slew rate between +10.5V and -20V must be controlled within 100μsec to 400μsec.
3. Data output load devices (switchable) capable of sinking 10mA from the output pin without rising more than 0.6 volts above ground. Open collector, open drain or discrete devices with resistive pull-ups of 4.7K 47K is the recommended implementation.
4. Data output sensing devices capable of sensing valid logic levels (VOH $\geq$ 70% VCC, VOL $\leq$ 20% VCC).
5. Address buffers able to maintain high state voltages of $\geq$ 70% of VCC at both high and low VCC,* and low state voltages $\leq$ 20% VCC at both high and low VCC.
6. Timing and control logic suitable to sequence the required functions.

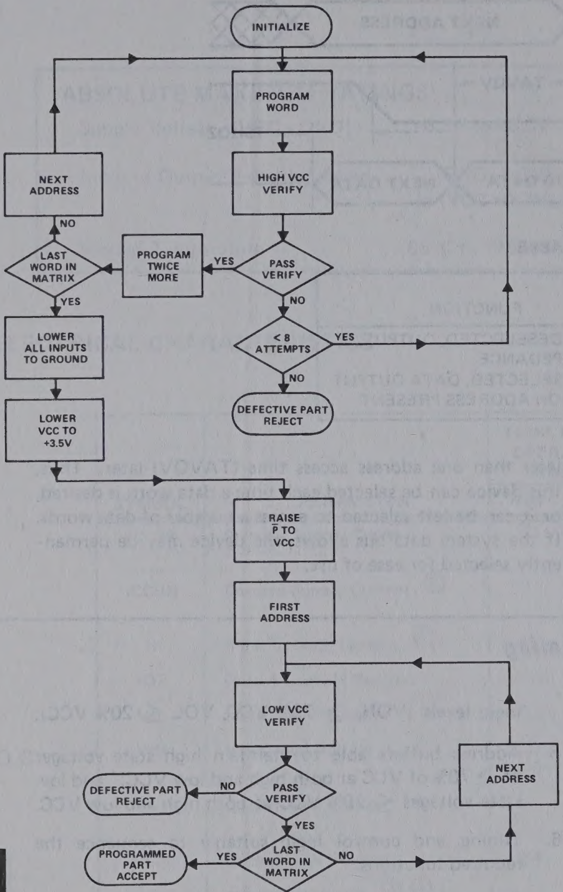
*Never allow any input to rise more than 0.3 volts above VCC.

PROGRAMMING PROCEDURE:

OVERALL:

1. Address and program word.
2. Verify data output at high VCC (10.5V ± .5V)
   a. If device fails to verify, repeat program – verify sequence (reject device as defective after 8 programming attempts at any one word).
   b. If device passes verify, repeat programming sequence twice more then return to step 1 to program the next word.
   c. If device passes verify at the last location to be programmed continue to step 3.
3. Lower VCC to 3.5 ± 0.5V and verify each location in the matrix.
   a. If any location fails to verify, reject the device as defective.
   b. If all locations pass verify, the part is properly programmed.

PROGRAMMING SEQUENCE FLOW CHART


INITIALIZE
PROGRAM WORD
HIGH VCC VERIFY
PASS VERIFY
YES
NO
PROGRAM TWICE MORE
LAST WORD IN MATRIX
NO
NEXT ADDRESS
YES
< 8 ATTEMPTS
YES
NO
DEFECTIVE PART REJECT
LOWER ALL INPUTS TO GROUND
LOWER VCC TO +3.5V
RAISE P TO VCC
FIRST ADDRESS
LOW VCC VERIFY
PASS VERIFY
NO
DEFECTIVE PART REJECT
YES
LAST WORD IN MATRIX
YES
PROGRAMMED PART ACCEPT
NO
NEXT ADDRESS

PROGRAMMING STEPS:

INITIALIZE:

VCC = +10.5V ± .5V
$\overline{P}$ = VCC
$\overline{S}$ = GND (not used during programming)

1. Setup the address of the word to be programmed.
2. Wait 500 nanoseconds or more (TAVPL).
3. Initiate the $\overline{P}$ supply falling edge.
4. After the $\overline{P}$ supply has crossed zero (ground) going negative, enable the data output load devices of each output pin that is to be programmed (to become a low or "0" logic state).
5. Disable the data output load 4 milliseconds (±1msec) after it was enabled (TQLQH).
6. The data output load devices must be disabled before the $\overline{P}$ supply is allowed to cross zero (ground) on its rising edge.
7. Invert A0 for 500 nanoseconds, then return A0 to its original logic state .
8. Wait 500 nanoseconds or more (TPHQV).
9. Compare the output data with the desired data.
   a. If any one bit fails to verify, program again starting at step 3. After 8 programming attempts at any one location, reject the device as defective. It is acceptable to repulse all desired bits if any one bit does not program.
   b. If all four bits verify, program the word twice more (steps 3 thru 8 twice). Then return to step 1 to address the program the next word.

After steps 1 thru 9 are completed for each word to be programmed:

10. Lower all inputs to ground.
11. Lower VCC to +3.5 volts ± .5 volts.
12. Raise $\overline{P}$ to VCC.*
13. Setup the address of the word to be verified. (High or "1" or VIH inputs must be > 2.35 and < VCC +0.3 volts).*
14. Wait 1 microsecond.
15. Compare the output data with the desired data.
    a. If any bit fails to verify, reject the device as defective.
    b. If all four bits verify, return to step 13 to verify the next word.

After steps 13 thru 15 are completed for each word in the matrix, the device has been properly programmed.

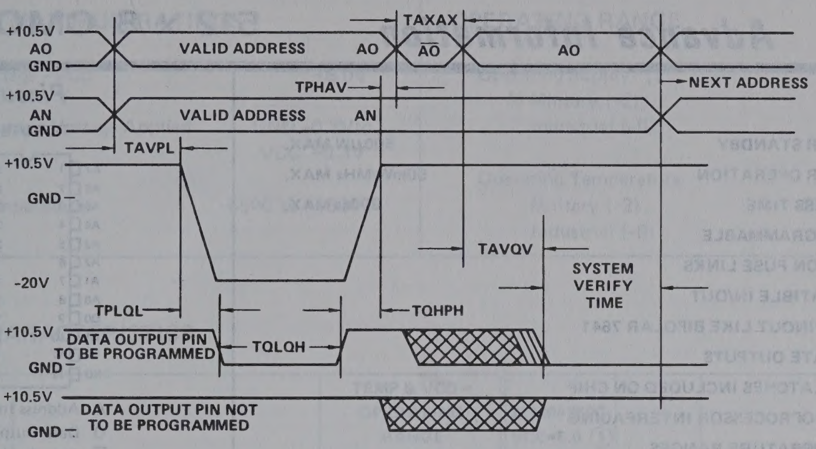
* Never allow any input to rise more than 0.3 volts above VCC.

PROGRAM CYCLE TIMING TABLE

SYMBOL	PARAMETER	MIN	MAX	UNITS
TAVPL	Address to Program Setup Time	500		ns
TPLQL	Program Enable to Data Time	100		µs
TAVQV	Address to Output Valid	500		ns
TQLQH	Data Low Pulse Width	3.0	5.0	ms
TQHPH	Data High to Program Disable Time	100		µs
TAXAX	A0 Inverted Time	500		ns
TPHQV	Program Disable to Read Time	500		ns
TPHAV	Program Disable to Address Invert (A0)	0		ns

PROGRAMMING CYCLE

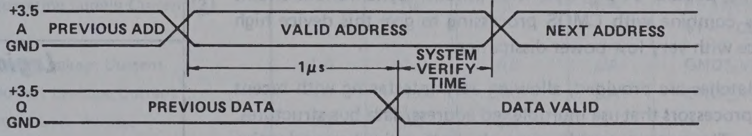
VCC = 10.5V ± .5V



TAXAX
+10.5V
AO
GND
VALID ADDRESS
AO
AO
AO
TPHAV
NEXT ADDRESS
+10.5V
AN
GND
VALID ADDRESS
AN
TAVPL
+10.5V
GND
TAVQV
SYSTEM VERIFY TIME
-20V
TPLQL
TQHPH
+10.5V
DATA OUTPUT PIN TO BE PROGRAMMED
TQLQH
GND
+10.5V
DATA OUTPUT PIN NOT TO BE PROGRAMMED
GND

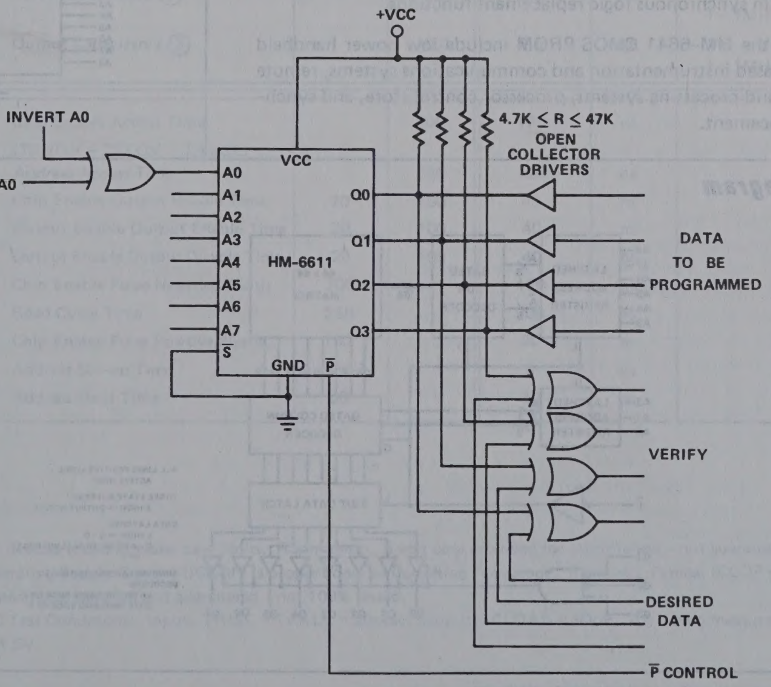
LOW VOLTAGE VERIFY CYCLE

VCC = 3.5V ± 0.5V



+3.5
A
GND
PREVIOUS ADD
VALID ADDRESS
NEXT ADDRESS
1μs
SYSTEM VERIFY TIME
+3.5
Q
GND
PREVIOUS DATA
DATA VALID

EXAMPLE PROGRAMMING CIRCUIT



+VCC
INVERT A0
A0
VCC
A0
A1
A2
A3
A4
A5
A6
A7
S̄
HM-6611
Q0
Q1
Q2
Q3
GND
P̄
4.7K ≤ R ≤ 47K
OPEN COLLECTOR DRIVERS
DATA TO BE PROGRAMMED
VERIFY
DESIRED DATA
P̄ CONTROL

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6641

512 x 8 CMOS PROM

Advance Information

Features

- LOW POWER STANDBY 500μW MAX.
- LOW POWER OPERATION 50mW/MHz MAX.
- FAST ACCESS TIME 200ns MAX.
- FIELD PROGRAMMABLE
- POLYSILICON FUSE LINKS
- TTL COMPATIBLE IN/OUT
- POPULAR PINOUT LIKE BIPOLAR 7641
- THREE STATE OUTPUTS
- ADDRESS LATCHES INCLUDED ON CHIP
- EASY MICROPROCESSOR INTERFACING
- WIDE TEMPERATURE RANGES

Description

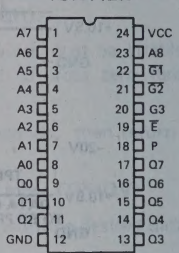
The HM-6641 is a 512 x 8 CMOS polysilicon fuse link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6641 in high speed pipelined architecture systems, and also in synchronous logic replacemant functions.

Applications for the HM-6641 CMOS PROM include low power handheld microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

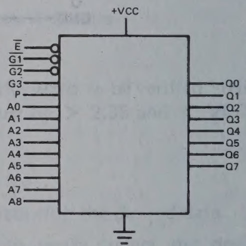
Pinout

TOP VIEW

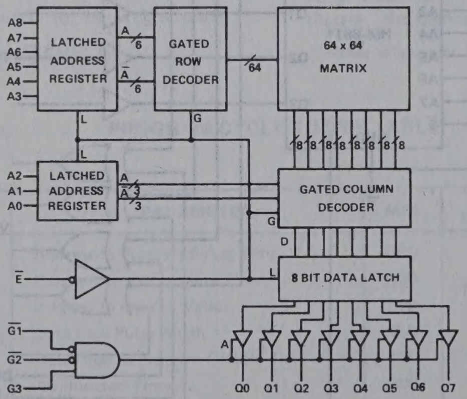

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 VCC
23 A8
22 $\overline{G1}$
21 $\overline{G2}$
20 G3
19 $\overline{E}$
18 P
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

A Address Input
Q Data Output
$\overline{E}$ Chip Enable
$\overline{G}$ Output Enable
P Program Enable
(P = Gnd. except when programming)

Logic Symbol


+VCC
$\overline{E}$
$\overline{G1}$
$\overline{G2}$
G3
P
A0
A1
A2
A3
A4
A5
A6
A7
A8
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

Functional Diagram


A8
A7
A6
A5
A4
A3
LATCHED ADDRESS REGISTER
A
6
$\overline{A}$
6
GATED ROW DECODER
64
64 x 64 MATRIX
L
G
L
8
A2
A1
A0
LATCHED ADDRESS REGISTER
A
$\overline{A}$
3
3
GATED COLUMN DECODER
G
D
$\overline{E}$
L
8 BIT DATA LATCH
A
$\overline{G1}$
$\overline{G2}$
G3
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

ALL LINES POSITIVE LOGIC -
ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

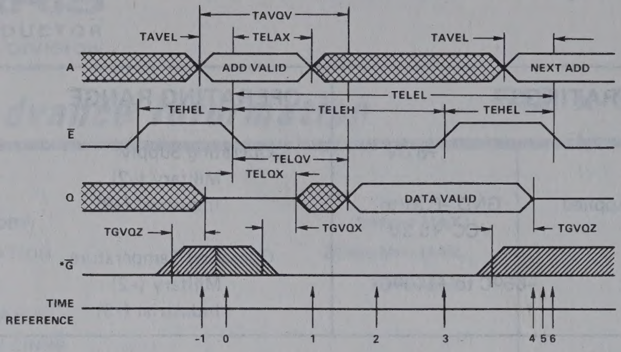
LECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	MAX	TEMP=25°C VCC=5.0 ① TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = GND OR VCC
ICCOP	Operating Supply Current ②		10	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
IOZ	Output Leakage Current	-1.0	+1.0	±0.5	μA	GND≤VO≤VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.1	V	IOL = 3.2mA
VOH	Output High Voltage	2.4		4.25	V	IOH = -1.0mA
CI	Input Capacitance ③		8.0	5.0	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		10.0	8.0	pF	VO = VCC OR GND f = 1MHz
TELQV	Chip Enable Access Time		200	120	ns	④
TAVQV	(TAVQV = TELQV + TAVEL) Address Access Time		220	120	ns	④
TELQX	Chip Enable Output Enable Time	20	100	40	ns	④
TGVQX	Output Enable Output Enable Time	20	100	40	ns	④
TGVQZ	Output Enable Output Disable Time	20	100	40	ns	④
TELEH	Chip Enable Pulse Negative Width	200		120	ns	④
TELEL	Read Cycle Time	350		200	ns	④
TEHEL	Chip Enable Pulse Positive Width	150		80	ns	④
TAVEL	Address Set-up Time	20		0	ns	④
TELAX	Address Hold Time	60		40	ns	④

NOTES:

① All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs-TRISE = TFALL = 20nsec; Outputs -CLOAD = 50pF. All timing measurements at 1.5V.

Read Cycle



*G HAS SAME TIMING AS $\overline{G}$ EXCEPT SIGNAL IS INVERTED

TRUTH TABLE

TIME REFERENCE	INPUTS E	G	A	OUTPUTS O	FUNCTION
-1	H	H	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS-ADDRESSES ARE LATCHED
1	L	L	X	X	OUTPUT ENABLED
2	L	L	X	V	OUTPUT VALID
3	↑	L	X	V	OUTPUT LATCHED
4	H	H	X	Z	READ ACCOMPLISHED AND OUTPUT DISABLED
5	H	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
6	↓	H	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6641 read cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$(T = 0). Minimum address setup and hold tie requirements must be met. After the required hold time,the addresses may change state without affecting device operation. To read data $\overline{G1}$ and $\overline{G2}$ must be low, and G3 must be high. After access time, $\overline{E}$ may be taken high to latch the data outputs and begin TEHEL. Taking either or both $\overline{G1}$ or $\overline{G2}$ high or G3 low will force the output buffers to a high impedance state. The output data may be re-enabled at any time taking $\overline{G1}$ and $\overline{G2}$ low and G3 high. On the falling edge of $\overline{E}$ the data will be unlatched. P should be grounded except when in the programming mode.

Programming

INTRODUCTION

The HM-6641 is a 512 word, by 8 bit field programmable read only memory utilizing polycrystalline silicon fusible links as programmable memory elements. Selected memory locations are permanently changed from their manufactured state, of all low (VOL) to a logical high (VOH), by the controlled application of programming potentials and pulses. Careful adherence to the following programming specifications will result in high programming yield. Both high VCC (6.0 volts) and low VCC (4.0 volts) verify cycles are specified to assure the integrity of the programmed fuse. This programming specification, although complete, does not preclude rapid programming. The worst case programming time required is 37.4 seconds, and typical programming time can be approximately 4 seconds per device.

The chip ($\overline{E}$) and output enable ($\overline{G}$) are used during the programming procedure. On PROM's which have more than one output enable control $\overline{G1}$ is to be used. The other output enables must be held in the active, or enabled, state throughout the entire programming sequence. The programmer designer is advised that all pins of the programmer's socket should be at ground potential when the PROM is inserted into the socket. VCC must be applied to the PROM before any input or output pin is allowed to rise*.

OVERALL PROGRAMMING PROCEDURE

1. The address of the first bit to be programmed is presented, and latched by the chip enable ($\overline{E}$) falling edge. The output is disabled by taking the output enable ($\overline{G}$) high.
2. VCC is raised to the programming voltage level, 12.5V.
3. The data output pin corresponding to the bit to be programmed is pulled low. All other bits in the word are pulled up to VCC (at the programming level).
4. A 500 μs pulse is applied to the programming control pin (P).
5. The data output pin is returned to VCC, and the VCC pin is returned to 6.0 volts.

6. The address of the bit is again presented, and latched by a second chip enable falling edge.

7. The data outputs are enabled, and read, to verify that the bit was successfully programmed.
   a). If verified, two post programming pulses are applied (the bit is programmed twice more). Then the next bit to be programmed is addressed and programmed .
   b). If not verified, the program/verify sequence is repeated up to 8 times total, at the programming voltage level, 12.5 volts.

8. After all bits to be programmed have been verified at 6.0 volts, the VCC is lowered to 4.0 volts and all bits are verified.
   a). If all bits verify, the device is properly programmed.
   b). If any bit fails to verify, the device is rejected.

PROGRAMMING SYSTEM REQUIREMENTS

1. The power supply for the device to be programmed must be able to be set to four voltages; 4.0V, 6.0V, +12.5V. This supply must be able to supply 500mA average, and 1A dynamic, currents to the PROM during programming. The power supply rise fall times when switching between voltages must be no quicker than 1μ s.

2. The address drivers must be able to maintain input voltage levels ≥70% VCC for VIH, and ≤ 20% VCC for VIL. The programming system designer has a choice between buffers that will track VCC up and down (e.g. open collector buffers with pull up resistors) or buffers used for VIH only at 4.0V and 6.0V and returned to VIL when the system is at programing voltages.*

3. The control input buffers have the same 70% and 20% VCC requirements as the address buffers. Notice that chip enable ($\overline{\text{E}}$) does not require a pull up to programming voltage levels, but that the output enable ($\overline{\text{G}}$) must have a pull up to track VCC up and down. The program control (P) must switch from ground to programming VCC level.*

4. The data input buffers must be able to sink up to 3mA from the PROM's output pins without rising more than 0.7 volts above ground, be able to hold the other outputs high with a current source capability of 0.5mA to 2.0mA, and not interfere with the reading and verifying of the data output of the PROM. Notice that a bit to be programmed is changed from a low state (VOL) to high (VOH) by pulling low on the output pin. A suggested implementation is open collector TTL buffers (or inverters) with 4.7KΩ pull up resistors to VCC.*

*Note: Never allow any input or output pin to rise more than 0.3 volts above VCC, or fall more than 0.3 volts below ground.

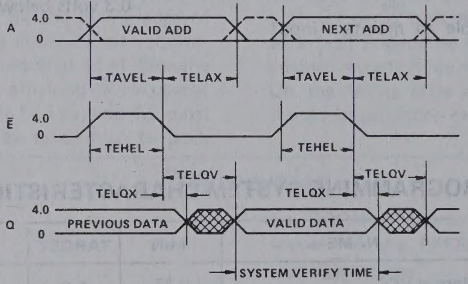
PROGRAMMING SYSTEM CHARACTERISTICS

PARAMETER	NAME	MIN	TARGET	MAX	UNITS
VCCN	Normal VCC	5.75	6.0	6.25	volts
VCC PGM	Programming Voltage	12.0	12.5	13.0	volts
VCC LV	Low Voltage Verify VCC	3.75	4.0	4.25	volts
ICC	System ICC Capability	500			mA
ICC Peak	Transient ICC Capability	1.0			A
	For PROM Input Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	20% VCC	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	.01			mA
IOH	Output Source Current (At VOH)	0.1			mA
	For PROM Data Output Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	0.7	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	3.0			mA
IOH	Output Source Current (at VOH)	0.5	1.0	2.0	mA

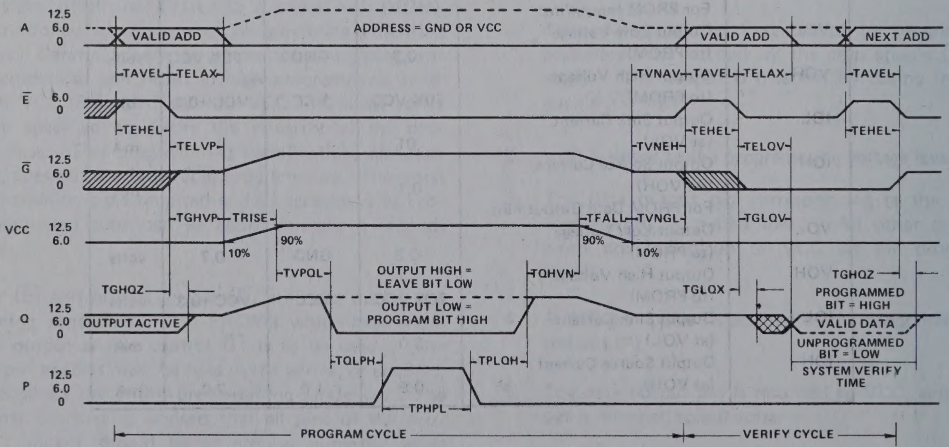
PROGRAMMING SYSTEM TIMING

SYMBOLS	PARAMETER	MIN	MAX	UNITS
TAVEL	Address Set-up Time	500		ns
TELAX	Address Hold Time	500		ns
TEHEL	Chip Enable High Time	500		ns
TELVP	Chip Enable Low to VCC Rising Delay	500		ns
TGHVP	Output Enable High to VCC Rising Delay	500		ns
TGHQZ	Output Disable Time		200	ns
TRISE	VCC Rise Time (to PGM Voltage)	1.0		μs
TVPQL	VCC High (PGM) to Output Low Delay	500		ns
TQLPH	Programming Data Setup Time	500		ns
TPHPL	Programming Pulse Width	450	550	μs
TPLQH	Programming Data Hold Time	500		ns
TQHVN	Output High to VCC Normal Delay	500		ns
TFALL	VCC Fall Time (to Normal VCC)	1.0		μs
TVNAV	VCC Normal to Address Delay	500		ns
TVNEH	VCC Normal to Chip Enable High Delay	500		ns
TVNGL	VCC Normal to Output Enable Low Delay	500		ns
TELQV	Chip Enable Access Time		500	ns
TGLQV	Output Enable Access Time		500	ns
TGLQX	Output Enable Time		200	ns

LOW VOLTAGE VERIFY CYCLE


A
4.0
0
VALID ADD
NEXT ADD
TAVEL
TELAX
TAVEL
TELAX
Ē
4.0
0
TEHEL
TEHEL
TELQV
TELQV
TELQX
TELQX
Q
4.0
0
PREVIOUS DATA
VALID DATA
SYSTEM VERIFY TIME

PROGRAM AND VERIFY CYCLE


A
12.5
6.0
0
VALID ADD
ADDRESS = GND OR VCC
VALID ADD
NEXT ADD
TAVEL
TELAX
TVNAV
TAVEL
TELAX
TAVEL
Ē
6.0
0
TEHEL
TELVP
TVNEH
TEHEL
TELQV
TEHEL
Ḡ
12.5
6.0
0
VCC
12.5
6.0
TGHVP
TRISE
10%
90%
TFALL
TVNGL
90%
10%
TGLQV
TVPQL
OUTPUT HIGH = LEAVE BIT LOW
TQHVN
TGHQZ
TGLQX
TGHQZ
PROGRAMMED BIT = HIGH
Q
12.5
6.0
0
OUTPUT ACTIVE
OUTPUT LOW = PROGRAM BIT HIGH
VALID DATA
UNPROGRAMMED BIT = LOW
SYSTEM VERIFY TIME
TQLPH
TPLQH
P
12.5
6.0
0
TPHPL
PROGRAM CYCLE
VERIFY CYCLE

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6661

1024-BIT FIELD PROGRAMMABLE CMOS PROM

DISCONTINUED

Features

- FUSED LINK PROM
- FIELD-PROGRAMMABLE
- ORGANIZED 256 x 4
- LOW POWER STANDBY 500μW MAX
- LOW POWER OPERATION 25mW/MHz MAX
- CMOS RAM PINOUT EXCEPT FOR $\overline{P}$
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- SYNCHRONOUS OPERATION
- FAST ACCESS TIME 400ns MAX
- HIGH NOISE IMMUNITY
- HIGH RELIABILITY
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 10 VOLT VERSION AVAILABLE

Description

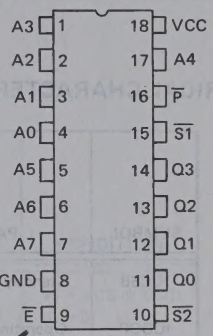
The HM-6661 is a 256 x 4 static CMOS PROM fabricated using self-aligned silicon gate technology. Synchronous circuit techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

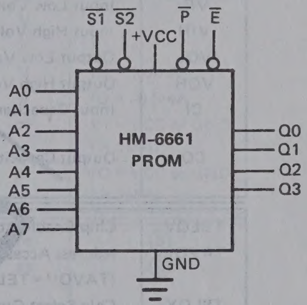
The HM-6661 employs polysilicon fuses as static memory elements. It is also pin for pin replaceable with the HM-6561, a 256 x 4 CMOS RAM, if $\overline{P}$ is tied to VCC. This allows a single memory board design with any organization of RAM and PROM.

Pinout

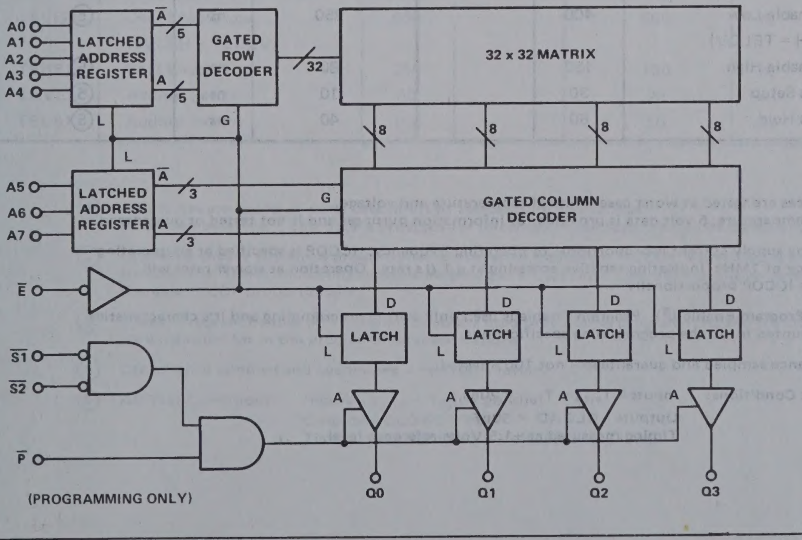
TOP VIEW


A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
$\overline{E}$ 9
18 VCC
17 A4
16 $\overline{P}$
15 $\overline{S1}$
14 Q3
13 Q2
12 Q1
11 Q0
10 $\overline{S2}$

Logic Symbol


$\overline{S1}$
$\overline{S2}$
+VCC
$\overline{P}$
$\overline{E}$
A0
A1
A2
A3
A4
A5
A6
A7
HM-6661
PROM
Q0
Q1
Q2
Q3
GND

Functional Diagram


A0
A1
A2
A3
A4
LATCHED ADDRESS REGISTER
$\overline{A}$
5
A
5
GATED ROW DECODER
32
32 x 32 MATRIX
L
G
L
8
8
8
8
A5
A6
A7
LATCHED ADDRESS REGISTER
$\overline{A}$
3
A
3
G
GATED COLUMN DECODER
$\overline{E}$
D
LATCH
L
A
$\overline{S1}$
$\overline{S2}$
$\overline{P}$
(PROGRAMMING ONLY)
Q0
Q1
Q2
Q3

ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES AND GATED DECODERS
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HM-6661-2/-9

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage (VCC - GND)	-0.3V to +12.0V	Operating Supply Voltage	+4.5V to +5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature	
		Industrial (-9)	40°C to +85°C
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL	UNITS	CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	5	μA	VI = VCC or GND IO = 0
	ICCOP	Operating Supply ②		8	5	mA	VI = VCC or GND IO = 0, f = 1MHz
	II	Input Leakage ③	-1	+1	0.0	μA	GND<VI<VCC
	IOZ	Output Leakage	-1	+1	0.0	μA	GND<VO<VCC
	VIL	Input Low Voltage	-0.3	0.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3		V	
	VOL	Output Low Voltage		0.4	0.3	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -1.0mA
	CI	Input Capacitance ③④		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③④		10.0	8.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access		400	250	ns	⑤
	TAVQV	Address Access (TAVQV = TELQV + TAVEL)		430	260	ns	⑤
	TSLQX	Chip Select Output Enable	20	150	50	ns	⑤
	TSHQZ	Chip Select Output Disable		150	50	ns	⑤
	TELEL	Read Cycle Time (TELEL = TELEH + TEHEL)	550		330	ns	⑤
	TELEH	Chip Enable Low (TELEH = TELQV)	400		250	ns	⑤
	TEHEL	Chip Enable High	150		80	ns	⑤
	TAVEL	Address Setup	30		10	ns	⑤
	TELAX	Address Hold	80		40	ns	⑤

DISCONTINUED

NOTES:

① All devices are tested at worst case limits of temperature and voltage.
Room temperature, 5 volt data is provided for information purposes and is not tested or guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1 μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Except Program Enable ($\overline{P}$). Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.

④ Capacitance sampled and guaranteed – not 100% tested.

⑤ AC Test Conditions: Inputs – T_{rise} = T_{fall} = 20ns.
Outputs – CLOAD = 50pF
Timing measured at +1.5 Volts reference level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +12.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	+4.5V to +5.5V
Operating Temperature Commercial (-5)	0°C to +75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V	UNITS	CONDITIONS
			MIN	MAX	TYP		
D.C.	ICCSB	Standby Supply Current		1.0	0.2	mA	VI = VCC or GND IO = 0
	ICCOP	Operating Supply ②		10	5	mA	VI = VCC or GND IO = 0, f = 1MHz
	II	Input Leakage ③	-5	+5	0.5	μA	GND < VI < VCC
	IOZ	Output Leakage	-10	+10	0.5	μA	GND < VO < VCC
	VIL	Input Low Voltage	-0.3	0.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3		V	
	VOL	Output Low Voltage			0.3	V	IO = 1.0mA
	VOH	Output High Voltage	2.4		4.0	V	IO = -0.5mA
	CI	Input Capacitance ③④		8.0	5.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③④		10.0	8.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access		600	500	ns	⑤
	TAVQV	Address Access (TAVQV = TELQV + TAVEL)		650	520	ns	⑤
	TSLQX	Chip Select Output Enable	20	200	50	ns	⑤
	TSHQZ	Chip Select Output Disable		200	50	ns	⑤
	TELEL	Read Cycle Time (TELEL = TELEH + TEHEL)	850		650	ns	⑤
	TELEH	Chip Enable Low (TELEH = TELQV)	600		500	ns	⑤
	TEHEL	Chip Enable High	250		150	ns	⑤
	TAVEL	Address Setup	50		20	ns	⑤
	TELAX	Address Hold	150		50	ns	⑤

DISCONTINUED

① All devices are tested at worst case limits of temperature and voltage.
Room temperature, 5 volt data is provided for information purposes and is not tested or guaranteed.

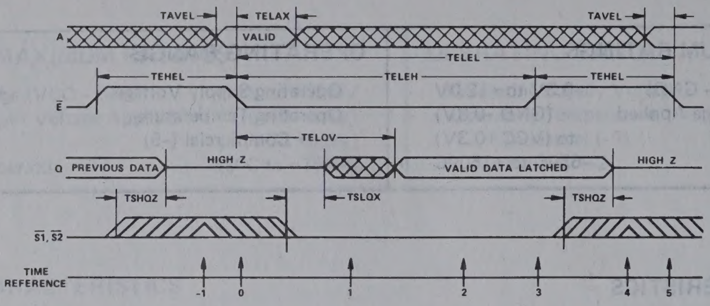
② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1 μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Except Program Enable (P̄). Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.

④ Capacitance sampled and guaranteed - not 100% tested.

⑤ AC Test Conditions: Inputs - $T_{rise} = T_{fall} = 20ns$.
Outputs - CLOAD = 50pF
Timing measured at +1.5 Volts reference level.

Read Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	A	OUTPUT DQ	FUNCTION
-1	H	H	X	Z	MEMORY DISABLED
0	↓	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	X	OUTPUT ENABLED
2	L	L	X	V	OUTPUT VALID
3	↑	L	X	V	OUTPUT LATCHED
4	H	H	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTE: Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low and deselected if either $\overline{S1}$ or $\overline{S2}$ are high

DISCONTINUED

The HM-6661 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low. The output data will be valid at access time (TELQV).

The HM-6661 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Programming

BACKGROUND INFORMATION

The HM-6661 is a 256 x 4 CMOS Programmable Read-Only Memory. It is programmed by the controlled application of programming pulses to selected memory cells. These pulses permanently alter the logic state of the memory cell. The memory array is manufactured with each cell set to the high or "1" logic state. The user may select any memory cell and permanently change its logic state to a "0" or low by programming.

Programming is accomplished by addressing the word to be programmed, applying the programming pulses, and verifying the data programmed. The verification is performed at high voltage (VCC) during the programming sequence, and at low voltage after all programming is completed.

PROGRAMMING SYSTEM CHARACTERISTICS:

1. Power source for the device to be programmed (VCC) variable from +3.0 to +11.0 volts, current capability of 500mA average and 1 amp dynamic currents.
2. Programming power supply is a negative 20.0V supply (±1.0V), switchable between -20V, 0V, +3.5V, and +10.5V. This supply must be able to deliver 400 mA average, and 1A peak currents at -20V. Less than 1mA output current is required at 0V, +3.5V, and at +10.5V. The slew rate between +10.5V and -20V must be controlled within 100μsec to 400μsec.
3. Data output load devices (switchable) capable of sinking 10mA from the output pin without rising more than 0.6 volts above ground. Open collector, open drain or discrete devices with resistive pull-ups of 4.7K to 47K is the recommended implementation.
4. Data output sensing devices capable of sensing valid logic levels (VOH $\geq$ 70% VCC, VOL $\leq$ 20% VCC).
5. Address buffers able to maintain high state voltages of $\geq$ 70% of VCC at both high and low VCC,* and low state voltages $\leq$ 20% VCC at both high and low VCC.
6. Timing and control logic suitable to sequence the required functions.

*Never allow any input to rise more than 0.3 volts above VCC.

PROGRAMMING PROCEDURE:

OVERALL:

1. Address and program word.
2. Verify data output at high VCC (10.5V ± .5V)
   a. If device fails to verify repeat program — verify sequence (reject device as defective after 8 programming attempts at any one word).
   b. If device passes verify repeat programming sequence twice more then return to step 1 to program the next word.
   c. If device passes verify at the last location to be programmed continue to step 3.
3. Lower VCC to 3.5 ± 0.5V and verify each location in the matrix.
   a. If any location fails to verify reject the device as defective.
   b. If all locations pass verify the part is properly programmed.

PROGRAMMING STEPS:

Initialize:
VCC = +10.5V ± .5V
Ē = P̄ = VCC
S̄1 = S̄2 = Gnd. (Not used during programming)

1. Set up the Address of the word to be programmed.
2. Wait 500ns or more (TAVEL).
3. Take chip enable (Ē) low; the falling edge latches the address.
4. Wait 500ns or more (TELPL).
5. Initiate the P̄ supply falling edge.
6. After the program enable voltage has crossed zero (Gnd) going negative (TPLQL), take low the data output load devices of each output pin that is to be programmed (to become a low or "0" logic state).
7. Take the data output loads back high 4ms ± 25% after they went low (TQLQH).
8. The program enable (P̄) must not rise back to ground before the data output load devices are all high (TQHPH).
9. After the program enable is high wait 500ns (TPHEH).
10. Pulse the chip enable (Ē) high for 500ns or more (TEHEL).
11. Take the chip enable (Ē) low to enable the device and read the output data to verify the programming after 1000ns (TELQV).
    a. If any one bit which was programmed fails to verify as a low or VOL, program again starting at step 5. After 8 programming attempts at any one location reject the device as defective. It is acceptable to re-pulse (TQLQH) all bits within a word if any bits do not program.
    b. If all 4 bits verify, apply two more programming pulses (steps 5 thru 11 twice). Then return to step 1 to address and program the next word.

After steps 1 thru 11 are completed for each word to be programmed:

12. Lower all inputs to ground.
13. Lower VCC to +3.5 volts ±0.5 volts.
14. Raise program enable (P̄) to VCC.*
15. Set up the address of the word to be verified. (High or "1" inputs must be >2.35 V and <VCC + 0.3V).*
16. Wait at least 500ns (TAVEL).
17. Take the chip enable (Ē) low to access the data.
18. Wait 1000ns (TELQV).
19. Compare the output data with the desired data.
    a. If any bit fails to verify reject the device as defective.
    b. If all four bits verify return to step 15 to address and verify the next word.

DISCONTINUED

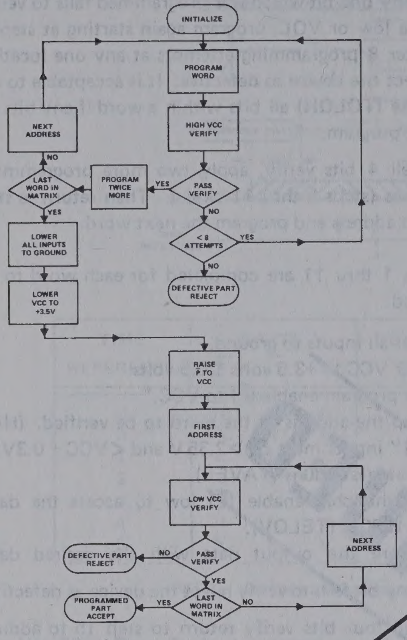
After steps 15 thru 19 are completed for each word in the matrix the device has been properly programmed and verified.

* Never allow any input or output pin to raise more than 0.3 volts above the VCC applied to the part at that moment. See the absolute maximum ratings section in the specifications.

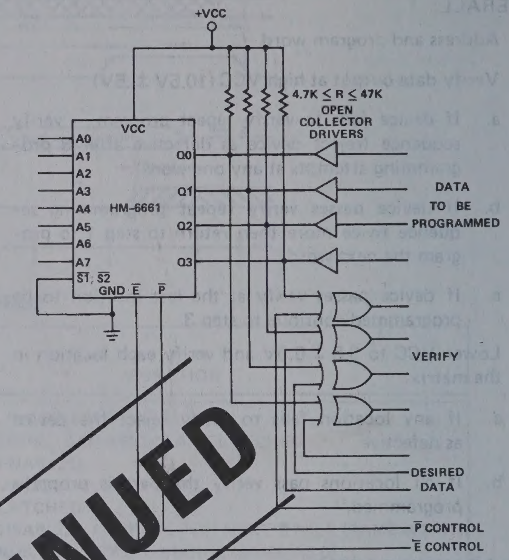
PROGRAMMING CYCLE TIMING TABLE

SYMBOL	PARAMETER	MIN	MAX	UNITS
TAVEL	Address Setup Time	500		ns
TELPL	Enable Low to Program Low Time	500		ns
TPLQL	Program Low to Data Low Time	100		µs
TQLQH	Data Low Pulse Width	3.0	5.0	ms
TQHPH	Data High to Program High Time	100		µs
TPHEH	Enable High Pulse Width	500		ns
TELQV	Verify Access Time		1.0	µs
TELEH	Verify Enable Low Time	1.0		µs

PROGRAMMING SEQUENCE FLOW CHART

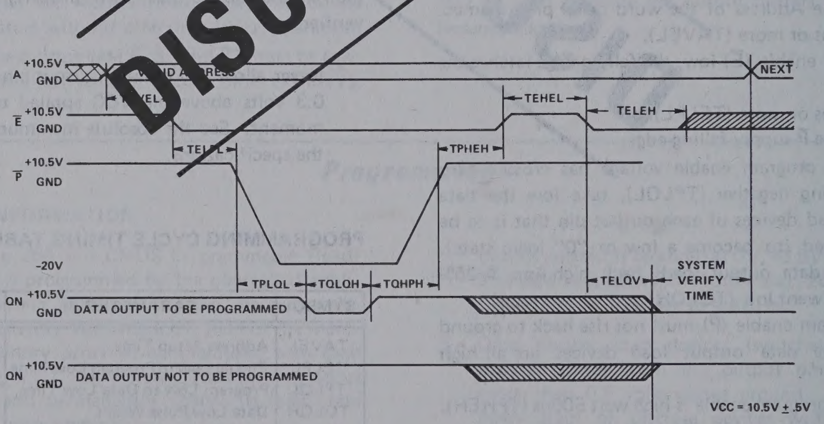

INITIALIZE
PROGRAM WORD
HIGH VCC VERIFY
PASS VERIFY
YES
NO
PROGRAM TWICE MORE
< 8 ATTEMPTS
DEFECTIVE PART REJECT
NEXT ADDRESS
LAST WORD IN MATRIX
LOWER ALL INPUTS TO GROUND
LOWER VCC TO +3.5V
RAISE P̄ TO VCC
FIRST ADDRESS
LOW VCC VERIFY
PASS VERIFY
DEFECTIVE PART REJECT
NEXT ADDRESS
LAST WORD IN MATRIX
PROGRAMMED PART ACCEPT

EXAMPLE PROGRAMMING CIRCUIT

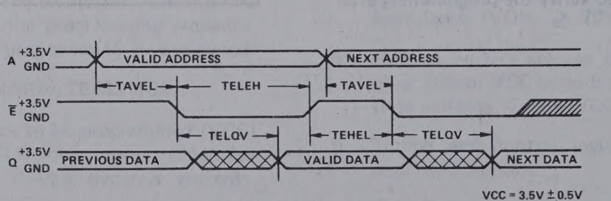

+VCC
4.7K ≤ R ≤ 47K
OPEN COLLECTOR DRIVERS
VCC
A0
A1
A2
A3
A4
A5
A6
A7
S̄1; S̄2
HM-6661
Q0
Q1
Q2
Q3
GND Ē P̄
DATA TO BE PROGRAMMED
VERIFY
DESIRED DATA
P̄ CONTROL
Ē CONTROL

DISCONTINUED

PROGRAMMING CYCLE


A
+10.5V
GND
VALID ADDRESS
NEXT
TAVEL
TEHEL
TELEH
Ē
+10.5V
GND
TELPL
TPHEH
P̄
+10.5V
GND
-20V
TPLQL
TQLQH
TQHPH
TELQV
SYSTEM VERIFY TIME
QN
+10.5V
GND
DATA OUTPUT TO BE PROGRAMMED
QN
+10.5V
GND
DATA OUTPUT NOT TO BE PROGRAMMED
VCC = 10.5V ± .5V

LOW VOLTAGE VERIFY CYCLE


A
+3.5V
GND
VALID ADDRESS
NEXT ADDRESS
TAVEL
TELEH
TAVEL
Ē
+3.5V
GND
TELQV
TEHEL
TELQV
Q
+3.5V
GND
PREVIOUS DATA
VALID DATA
NEXT DATA
VCC = 3.5V ± 0.5V

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6716

2K x 8 CMOS UV EPROM

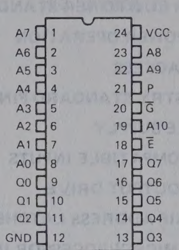
Preview

Features

• SUPER LOW POWER STANDBY	500µW MAX.
• LOW POWER OPERATION	50mW/MHz MAX.
• FAST ACCESS	350ns MAX.
• INDUSTRY STANDARD PINOUT	
• SINGLE SUPPLY	5 VOLT VCC
• TTL COMPATIBLE INPUTS	
• HIGH OUTPUT DRIVE	2 STD. TTL LOADS
• ON CHIP ADDRESS LATCHES	
• EASY MICROPROCESSOR INTERFACING	
• WIDE TEMPERATURE RANGE	

Pinout

TOP VIEW

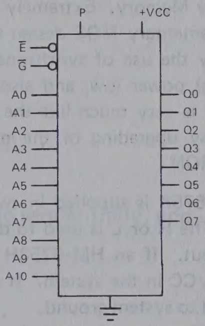

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 VCC
23 A8
22 A9
21 P
20 $\overline{G}$
19 A10
18 $\overline{E}$
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

A Address Input
Q Data Output
$\overline{E}$ Chip Enable
$\overline{G}$ Output Enable
P Program Enable

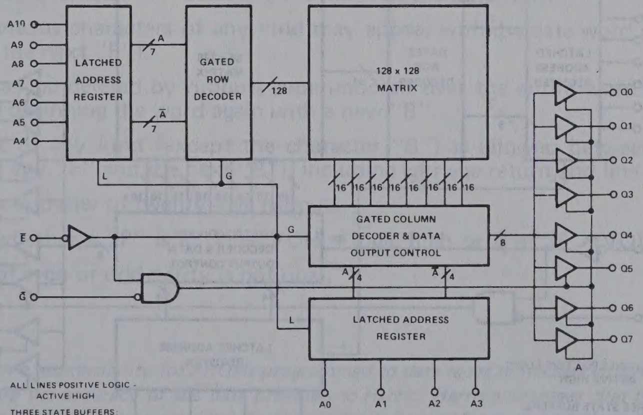
Description

The HM-6716 is a CMOS 2048 x 8 ultra-violet Erasable Programmable Read Only Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6716 is very much like the industry standard 2716. This pinout also allows easy upgrading of the memory array from the HM-6758, 1024 by 8 UV EPROM.

Logic Symbol


P
+VCC
$\overline{E}$
$\overline{G}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

Functional Diagram


A10
A9
A8
A7
A6
A5
A4
LATCHED ADDRESS REGISTER
L
G
A 7
$\overline{A}$ 7
GATED ROW DECODER
128
128 x 128 MATRIX
16 16 16 16 16 16 16 16
GATED COLUMN DECODER & DATA OUTPUT CONTROL
8
A 4
$\overline{A}$ 4
LATCHED ADDRESS REGISTER
E
G
L
A
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
A0
A1
A2
A3

ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6758

1K x 8 CMOS UV EPROM

Preview

Features

• SUPER LOW POWER STANDBY	500μW MAX.
• LOW POWER OPERATION	50mW/MHz MAX.
• FAST ACCESS	350ns MAX.
• INDUSTRY STANDARD PINOUT	
• SINGLE SUPPLY	5 VOLT VCC
• TTL COMPATIBLE INPUTS	
• HIGH OUTPUT DRIVE	2 STD. TTL LOADS
• ON CHIP ADDRESS LATCHES	
• EASY MICROPROCESSOR INTERFACING	
• WIDE TEMPERATURE RANGE	

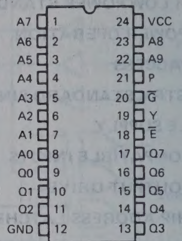
Description

The HM-6758 is a CMOS 1024 x 8 ultra-violet Erasable Programmable Read Only Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6758 is very much like the industry standard 2758. This pinout also allows easy upgrading of the memory array to the HM-6716, 2048 by 8 UV EPROM.

The HM-6758 is supplied in two versions, the HM-6758H and the HM-6758L. The H or L is used to designate the logic level to be connected to the Y input. If an HM-6758H is procured the user must connect the Y input to VCC in the system. If an HM-6758L is used the Y input must be connected to system ground.

Pinout

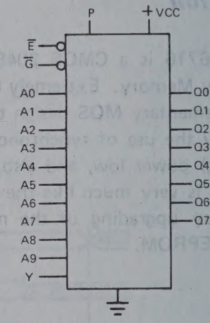
TOP VIEW



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
GND 12
24 VCC
23 A8
22 A9
21 P
20 $\overline{G}$
19 Y
18 $\overline{E}$
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

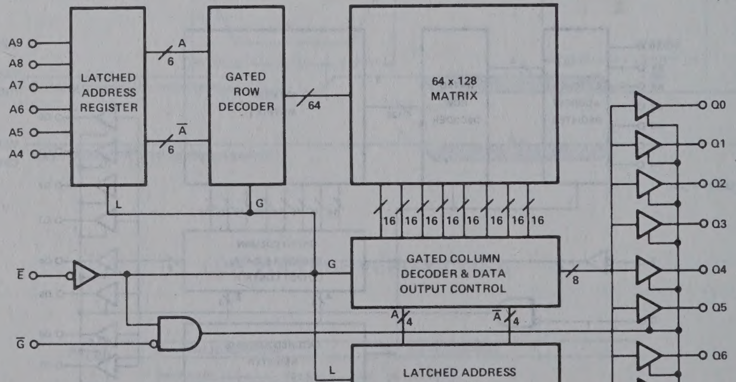
A	Address Input	$\overline{G}$	Output Enable
Q	Data Output	P	Program Enable
$\overline{E}$	Chip Enable	Y	Hard Wired Input

Logic Symbol



P
+VCC
$\overline{E}$
$\overline{G}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
Y
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

Functional Diagram



A9
A8
A7
A6
A5
A4
LATCHED ADDRESS REGISTER
A
6
$\overline{A}$
6
GATED ROW DECODER
64
64 x 128 MATRIX
L
G
16 16 16 16 16 16 16 16
$\overline{E}$
$\overline{G}$
G
GATED COLUMN DECODER & DATA OUTPUT CONTROL
8
A 4
$\overline{A}$ 4
L
LATCHED ADDRESS REGISTER
A0
A1
A2
A3
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
A

ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

Data Entry Formats for Harris Custom Programming*

For Harris to custom program to a user data pattern specification, the user must supply the data in one of the following formats:

1. Master PROM of same organization and pinout as device ordered. Two pieces required, three preferred.
2. Paper tape in Binary or ASCII BPNF.

* BINARY PAPER TAPE FORMAT

- A minimum of six inches of leader.
- A rubout (all eight locations punched).
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N"), with no interruptions or extraneous characters of any kind.
- Specify whether a punched hole is a VOH = "1" = logic high or is a VOL = "0" = logic low.
- A minimum trailer of six inches of tape.

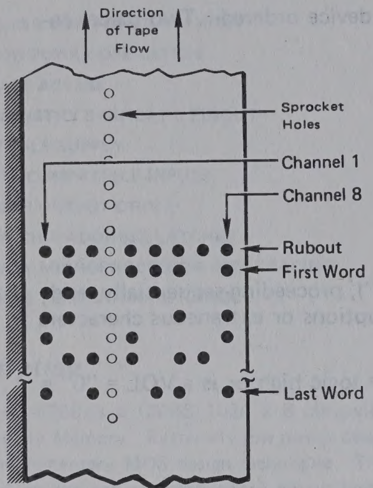
* ASCII BPNF FORMAT

- A minimum leader of twenty rubouts (all eight locations punched).
- Any characters desired (none necessary) except "B".
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N").
- Data words consist of:
    1. The character "B" denoting the beginning of a data word.
    2. A sequence of characters, only "P" or "N", one character for each bit in the word.
    3. The character "F" denoting the finish of the data word.
- No extraneous characters of any kind may appear within a data word (between any "B" and the next "F").
- Errors may be deleted by rubouts superimposed over the entire word including the "B", and beginning the word again with a new "B".
- Any text of any kind (except the character "B") is allowed between data words (between any "F" and the next "B"), including carriage return and line feed.
- A minimum trailer of twenty-five rubouts.
- Specify whether a "P" is a "1" = VOH = logic high or is a "0" = VOL = logic low.
- The use of even or odd parity is optional.

---

* *Harris can not assume responsibility for PROMs programmed to data tapes or masters which contain errors. The user must insure the accuracy of the data provided to Harris. Harris guarantees that the programmed PROMs will contain the information provided if either of the following formats are followed.*

BINARY PAPER TAPE EXAMPLE


Direction of Tape Flow
Sprocket Holes
Channel 1
Channel 8
Rubout
First Word
Last Word

Punched Hole = "0" = VOL = Logic Low

Word				PROM Output Data ①								
				Channel	8	7	6	5	4	3	2	1
AX ··· A2	A1	A0		Output	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ···· 0	0	0	First		0	1	0	0	0	1	0	1
0 ···· 0	0	1	Second		1	1	1	0	1	0	0	0
0 ···· 0	1	0	Third		0	1	0	1	1	1	0	0
0 ···· 0	1	1	Fourth		0	1	1	1	0	1	1	0
0 ···· 1	0	0	Fifth		1	0	0	1	0	0	0	1
1 ···· 1	1	1	Last		0	1	0	0	1	0	1	0

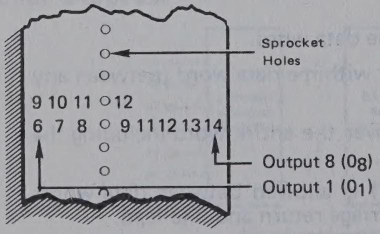
NOTES:

① PROMs with 4 bit wide data outputs require punching only first 4 channels on tape (Channels 1 thru 4).

② On HARRIS PROMs O_X (Example: O_1) designates a respective output pin on the device. O_1 (Output 1) is always LSB.

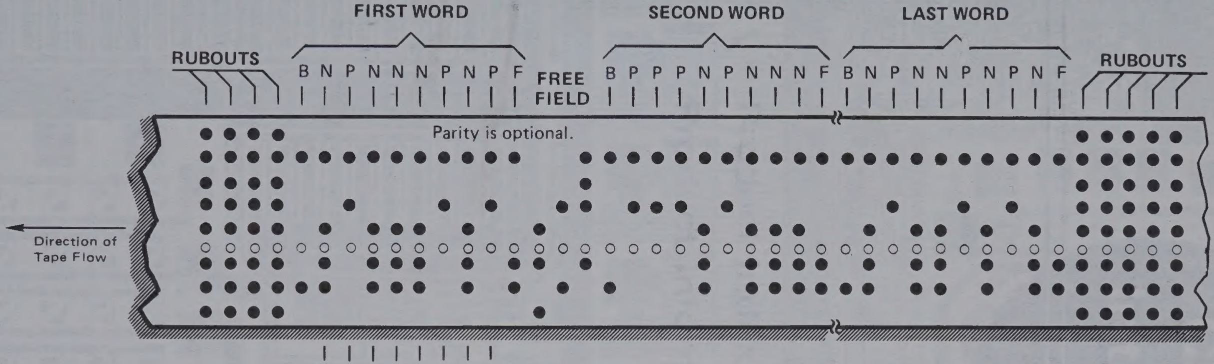
DEVICE OUTPUT PACKAGE PINS

EXAMPLE:


Sprocket Holes
9 10 11 12
6 7 8 9 11 12 13 14
Output 8 (O8)
Output 1 (O1)

Package	Device Type
16 Pin CMOS	HM-6611
20 Pin Bipolar	HM-7649

ASCII BPNF PAPER TAPE EXAMPLE


FIRST WORD
SECOND WORD
LAST WORD
RUBOUTS
B N P N N N P N P F
FREE FIELD
B P P P N P N N N F
B N P N N P N P N F
RUBOUTS
Parity is optional.
Direction of Tape Flow

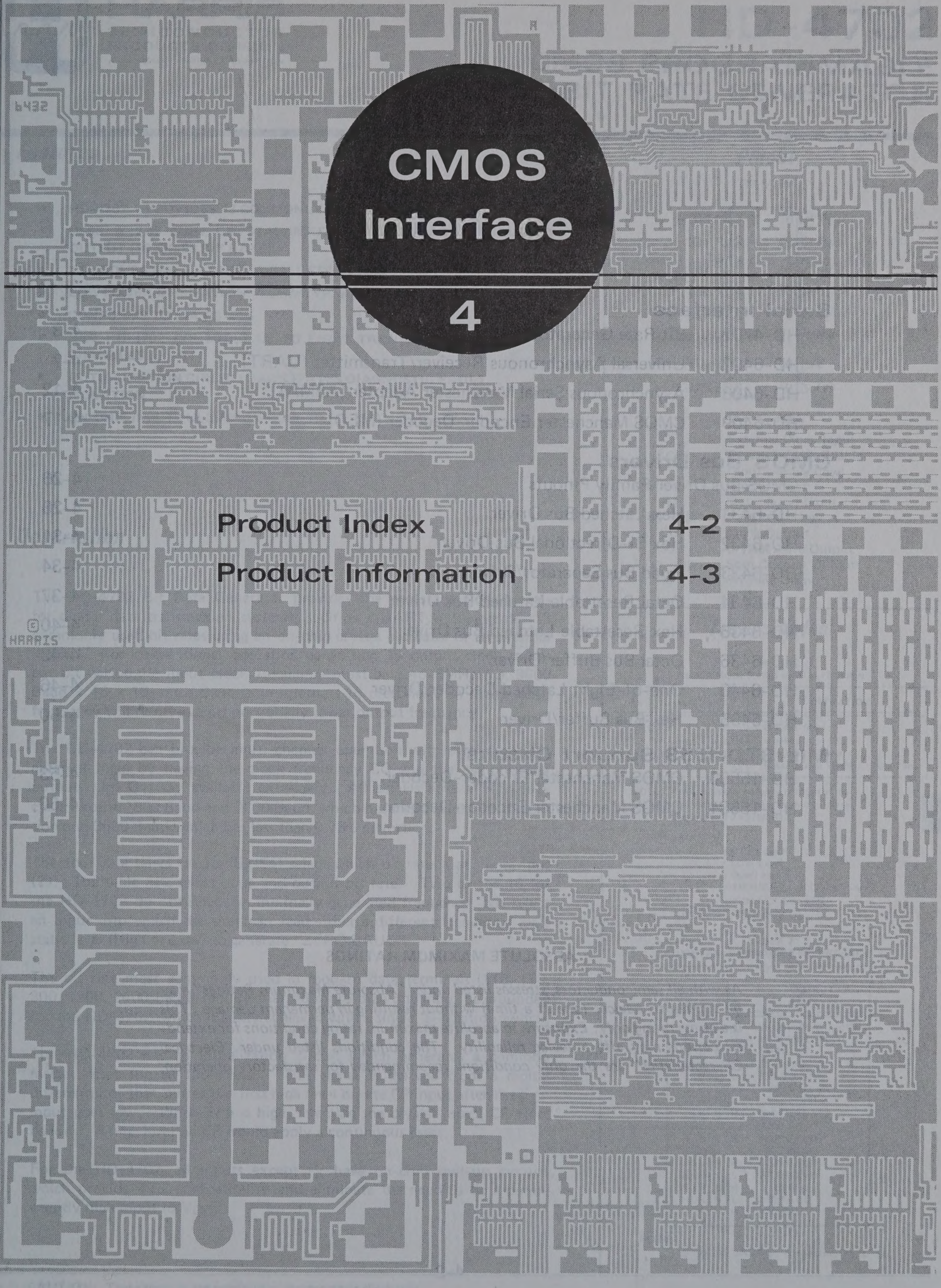
EXAMPLE	PACKAGE TYPE	DEVICE OUTPUT PINS
HM-6611	16 Pin Pkg.	12 11 10 9 (MOS)
HM-7649	20 Pin Pkg.	14 13 12 11 9 8 7 6

Truth Table
Character "D" = "1" = VOH = Logic High
Character "V" = "0" = VOL = Logic Low

Word					PROM Outputs Data ①							
AX ···· A2	A1	A0			O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ····· 0	0	0	First		0	1	0	0	0	1	0	1
0 ····· 0	0	1	Second		1	1	1	0	1	0	0	0
1 ····· 0	1	0	Last		0	1	0	0	1	0	1	0

NOTES:

① In the ASCII BPNF format, MSB data is punched after "B". On devices with 8 outputs, O_8 (Output 8) data is punched after "B". On devices with 4 outputs, O_4 (Output 4) data is punched after "B".



CMOS Interface

4

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ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

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HD-4702
CMOS PROGRAMMABLE BIT RATE GENERATOR

Features

- HD-4702 – PROVIDES 13 COMMONLY USED BIT RATES
- USES A 2.4576MHz CRYSTAL/INPUT FOR STANDARD FREQUENCY OUTPUT (16 TIMES BIT RATE)
- TTL COMPATIBLE – OUTPUT WILL SINK 1.6mA
- LOW POWER DISSIPATION 4.5mW TYP. @ 2.4576MHz
- CONFORMS TO EIA RS-404
- ONE HD-4702 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- ON-CHIP INPUT PULL-UP CIRCUIT

Description

The HD-4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud and 2000 Baud, which has less than 0.39% distortion and 3600 Baud, which has less than 0.78% distortion.

The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). The table lists select code and output bit rate. Two of the 16 for the HD-4702 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

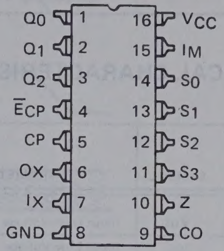
The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single 5-position switch.

The HD-4702 has an initialization circuit which generates a common master reset for all flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\bar{E}_{CP}$ input goes low. When $\bar{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

For the HD-4702, all inputs except I_X have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to V_{CC}.

Pinout

TOP VIEW



PIN NAMES

CP	External Clock Input
$\bar{E}_{CP}$	External Clock Enable Input (Active Low)
IX	Crystal Input
IM	Multiplexed Input
S_0 - S_3	Rate Select Inputs
CO	Clock Output
OX	Crystal Drive Output
Q_0 - Q_2	Scan Counter Outputs
Z	Bit Rate Output

Truth Tables

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	E_{CP}	CP	OPERATION
⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During 1st CP = HIGH Time

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't care
⎍ = 1st HIGH Level Clock Pulse after ECP goes LOW
⎍⎍ = Clock Pulse

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	OUTPUT RATE (Z)
L	L	L	L	MUX INPUT (I_M) ①
L	L	L	H	MUX INPUT (I_M)
L	L	H	L	50 BAUD
L	L	H	H	75 BAUD
L	H	L	L	134.5 BAUD
L	H	L	H	200 BAUD
L	H	H	L	600 BAUD
L	H	H	H	2400 BAUD
H	L	L	L	9600 BAUD
H	L	L	H	4800 BAUD
H	L	H	L	1800 BAUD
H	L	H	H	1200 BAUD
H	H	L	L	2400 BAUD
H	H	L	H	300 BAUD
H	H	H	L	150 BAUD
H	H	H	H	110 BAUD

NOTE:
① 19200 BAUD by connecting Q_2 to I_M.

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+8.0V
Input or Output Voltage Applied		(GND -0.3V) to (V_{CC} +0.3V)
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range		
Industrial	HD-4702-9	-40°C to +85°C
Military	HD-4702-2	-55°C to +125°C
Operating Voltage Range		+4 to +7V

ELECTRICAL CHARACTERISTICS

D.C.: V_{CC} = 5V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 5V; T_A = 25°C.

D.C.

SYMBOL	PARAMETER	HD-4702-2			HD-4702-9			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
V_{IH}	Input High Voltage	VCC 70%			VCC 70%			V		
V_{IL}	Input Low Voltage			VCC 30%			VCC 30%	V		
V_{OH1}	Output High Voltage	VCC -.05			VCC -.05			V	$I_{OH} \leq -1\mu A$	
V_{OL1}	Output Low Voltage			0.05			0.05	V	$I_{OL} \leq +1\mu A$	
I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{CC}$, All other pins = 0V	
I_{IL}	INPUT ① LOW CURRENT (all other inputs)		-30	-100		-30	-100	μA		
I_{ILX}	INPUT LOW CURRENT (I_X inputs)	-1		+1	-1		+1	μA	V_I = 0, All other pins = V_{CC}	
I_{OHX}	OUTPUT HIGH CURRENT (O_X)	-0.1			-0.1			mA	$V_{OUT} = V_{CC}$ -.5	Input at 0 or V_{CC} per Logic Function or Truth Table
I_{OH1}	OUTPUT HIGH CURRENT (all other outputs)	-1.0			-1.0			mA	V_{OUT} = 2.5V	
I_{OH2}	OUTPUT HIGH CURRENT (all other outputs)	-0.3			-0.3			mA	$V_{OUT} = V_{CC}$ -.5	
I_{OLX}	OUTPUT LOW CURRENT (O_X)	0.1			0.1			mA	V_{OUT} = .4V	
I_{OL}	OUTPUT LOW CURRENT (all other outputs)	1.6			1.6			mA	V_{OUT} = .4V	
I_{CC}	SUPPLY ① CURRENT (STATIC)			500 150			1500 1000	μA μA	$\overline{E}_{CP} = V_{CC}$, CP = 0, All other inputs = GND $\overline{E}_{CP} = V_{CC}$, CP = 0, All other inputs = V_{CC}	

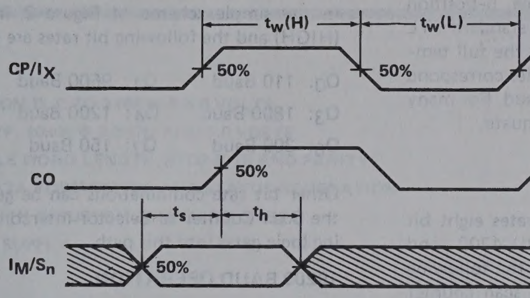
A.C.

SYMBOL	PARAMETER	HD-4702-2			HD-4702-9			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			300 250			300 250	ns ns	$C_L \leq 7pF$ on O_X ②
t_{PLH} t_{PHL}	Propagation Delay, CP to CO			215 195			215 195	ns ns	C_L = 15pF, Input Transition Times ≤ 20ns
t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CO to Z			75 65			75 65	ns ns	
t_{TLH} t_{THL}	Output Transition Time (except O_X)			80 40			80 40	ns ns	
t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			350 275			350 275	ns ns	$C_L \leq 7pF$ on O_X ②
t_{PLH} t_{PHL}	Propagation Delay, CP to CO			260 220			260 220	ns ns	C_L = 50pF, Input Transition Times ≤ 20ns
t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CO to Z			85 75			85 75	ns ns	
t_{TLH} t_{THL}	Output Transition Time (except O_X)			160 75			160 75	ns ns	
t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	350 0			350 0			ns ns	$C_L \leq 7pF$ on O_X ②
t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO	350 0			350 0			ns ns	C_L = 15pF, Input Transition Times ≤ 20ns
$t_{wCP(L)}$ $t_{wCP(H)}$	Minimum Clock Pulse-Width Low and High ③ ④	120 120			120 120			ns ns	
$t_{wCP(L)}$ $t_{wCP(H)}$	Minimum I_X Pulse Width, Low and High ④	160 160			160 160			ns ns	

NOTES:

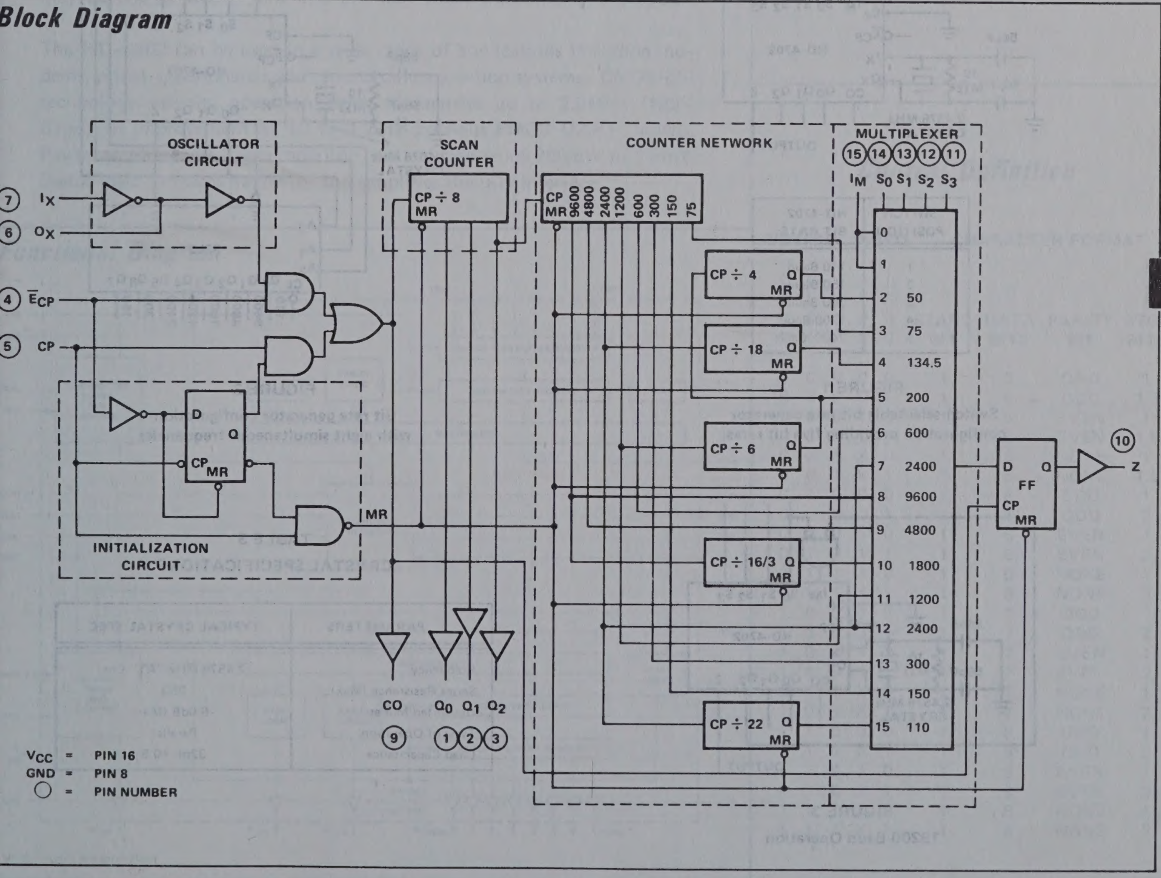
① Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
② Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_w) do not vary with load capacitance.
③ The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 350ns long to guarantee reset of all Counters.
④ It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15μs.
⑤ For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.

Switching Waveforms


t_W(H)
t_W(L)
CP/I_X
50%
50%
50%
CO
50%
t_s
t_h
I_M/S_n
50%

NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

Block Diagram


OSCILLATOR CIRCUIT
⑦ I_X
⑥ O_X
④ $\overline{E}_{CP}$
⑤ CP
D
Q
CP
MR
INITIALIZATION CIRCUIT
MR
SCAN COUNTER
CP ÷ 8
MR
CO
Q_0
Q_1
Q_2
⑨ ① ② ③
COUNTER NETWORK
CP
MR
9600
4800
2400
1200
600
300
150
75
CP ÷ 4 Q MR
CP ÷ 18 Q MR
CP ÷ 6 Q MR
CP ÷ 16/3 Q MR
CP ÷ 22 Q MR
MULTIPLEXER
⑮ ⑭ ⑬ ⑫ ⑪
I_M S_0 S_1 S_2 S_3
0
1
2 50
3 75
4 134.5
5 200
6 600
7 2400
8 9600
9 4800
10 1800
11 1200
12 2400
13 300
14 150
15 110
D Q
FF
CP
MR
⑩
Z
V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBER

SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the HD-4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

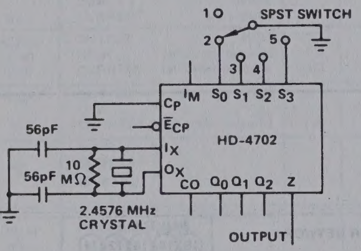
Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs, As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702 to interrogate sequentially the state of eight different frequency signals. The 93L34 8 Bit Addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud	Q_1: 9600 Baud	Q_2: 4800 Baud
Q_3: 1800 Baud	Q_4: 1200 Baud	Q_5: 2400 Baud
Q_6: 300 Baud	Q_7: 150 Baud	

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

19200 BAUD OPERATION

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702 can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the HD-4702 (See Figure 3).


1
SPST SWITCH
2
5
3
4
I_M S_0 S_1 S_2 S_3
CP
$\bar{E}_{CP}$
HD-4702
I_X
O_X
CO Q_0 Q_1 Q_2 Z
56pF
56pF
10 MΩ
2.4576 MHz CRYSTAL
OUTPUT

SWITCH POSITION	HD-4702 BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

FIGURE 1

Switch selectable bit rate generator configuration providing five bit rates.

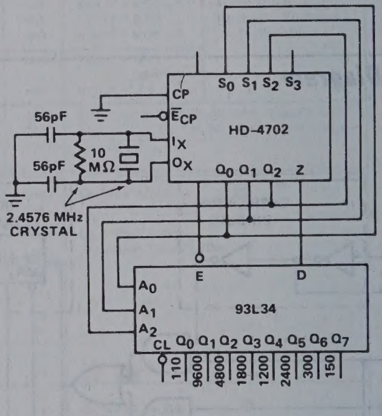

CP
S_0 S_1 S_2 S_3
$\bar{E}_{CP}$
HD-4702
I_X
O_X
Q_0 Q_1 Q_2 Z
56pF
56pF
10 MΩ
2.4576 MHz CRYSTAL
E
D
A_0
A_1
A_2
93L34
CL Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7
110
9600
4800
1800
1200
2400
300
150

FIGURE 2

Bit rate generator configuration with eight simultaneous frequencies

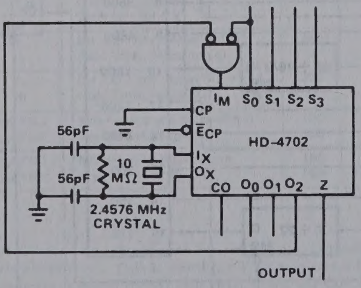

I_M S_0 S_1 S_2 S_3
CP
$\bar{E}_{CP}$
HD-4702
I_X
O_X
CO Q_0 Q_1 Q_2 Z
56pF
56pF
10 MΩ
2.4576 MHz CRYSTAL
OUTPUT

FIGURE 3

19200 Baud Operation

TABLE 3

CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5

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HD-6402

CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)

Features

- OPERATION FROM D. C TO 2.0MHz @ 5.0 VOLTS
- LOW POWER-TYP. 10mW @ 2.0MHz AND 5.0 VOLTS
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART'S
- SINGLE POWER SUPPLY

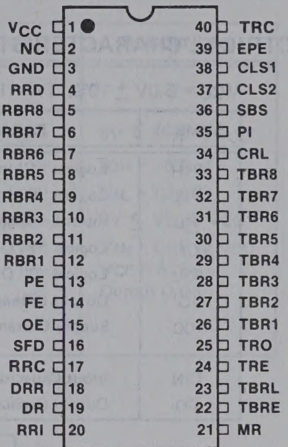
Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 2.0MHz (125K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

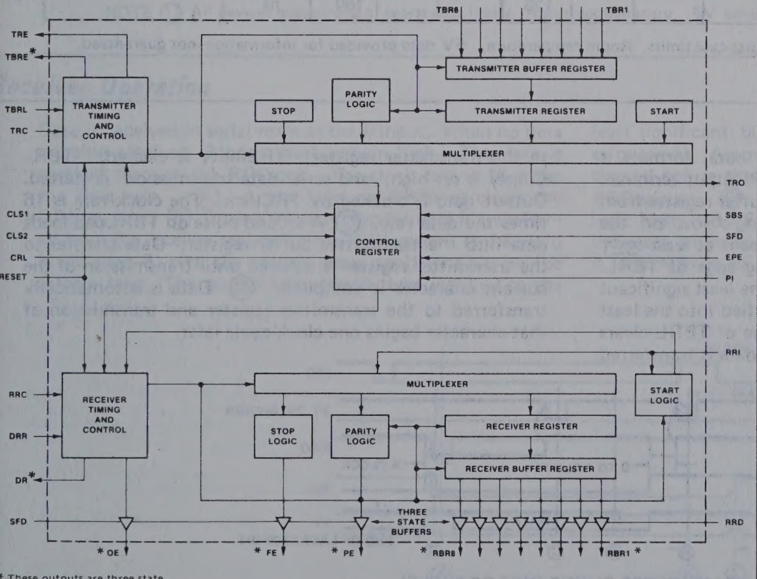
Pinout

TOP VIEW



V_{CC} 1
NC 2
GND 3
RRD 4
RBR8 5
RBR7 6
RBR6 7
RBR5 8
RBR4 9
RBR3 10
RBR2 11
RBR1 12
PE 13
FE 14
OE 15
SFD 16
RRC 17
DRR 18
DR 19
RRI 20
40 TRC
39 EPE
38 CLS1
37 CLS2
36 SBS
35 PI
34 CRL
33 TBR8
32 TBR7
31 TBR6
30 TBR5
29 TBR4
28 TBR3
27 TBR2
26 TBR1
25 TRO
24 TRE
23 TBRL
22 TBRE
21 MR

Functional Diagram



TBR8
TBR1
TRE
TBRE*
TBRL
TRC
TRANSMITTER TIMING AND CONTROL
TRANSMITTER BUFFER REGISTER
PARITY LOGIC
STOP
TRANSMITTER REGISTER
START
MULTIPLEXER
TRO
SBS
SFD
EPE
PI
CLS1
CLS2
CRL
RESET
CONTROL REGISTER
RRI
MULTIPLEXER
START LOGIC
RRC
DRR
DR*
RECEIVER TIMING AND CONTROL
STOP LOGIC
PARITY LOGIC
RECEIVER REGISTER
RECEIVER BUFFER REGISTER
SFD
THREE STATE BUFFERS
RRD
* OE
* FE
* PE
* RBR8
RBR1 *

* These outputs are three state

Control Definition

CONTROL WORD					CHARACTER FORMAT			
CLS2	CLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6402-9	-40°C to +85°C
Military HD-6402-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%. T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	0V ≤ V_{IN} ≤ V_{CC}
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-1.0		1.0	μA	0V ≤ V_O ≤ V_{CC}
I_{CC}	Supply Current		1.0	100	μA	V_{IN} = GND or V_{CC}; V_{CC} = 5.5V, Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested

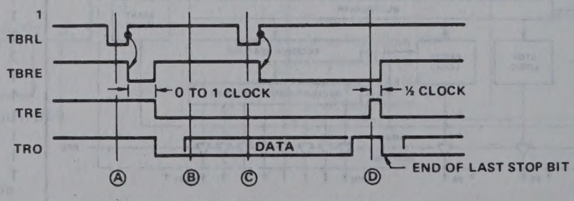
A.C.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		3.0	D.C.		2.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	150			150			ns	C_L = 50pF
t_{MR}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	50			50			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	60			60			ns	
t_{EN}	Output Enable Time			125			160	ns	

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. Ⓐ Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. Ⓑ The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared, TBR-Empty is set high, and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

Specifications HD-6402C-9

BSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (Industrial -9)	-40°C to +85°C

LECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 5%. T_A = Industrial

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-10.0		+10.0	μA	0V ≤ V_{IN} ≤ V_{CC}
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-10.0		+10.0	μA	0V ≤ V_O ≤ V_{CC}
I_{CC}	Supply Current		1.0	800	μA	V_{IN} = GND or V_{CC} V_{CC} = 5.25V Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested.

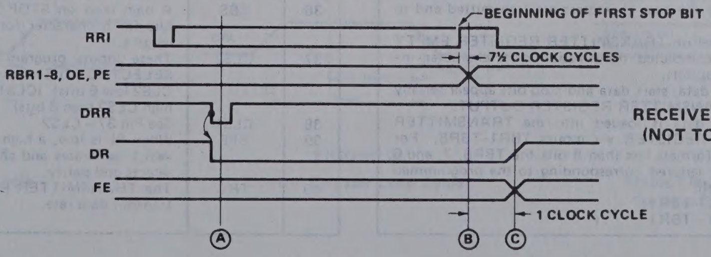
A.C.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 5% T_A = Industrial				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	200			225			ns	C_L = 50pF See Switching Time Waveforms 1, 2, 3
t_{MR}	Pulse Width MR	500			600			ns	
t_{SET}	Input Data Setup Time	60			75			ns	
t_{HOLD}	Input Data Hold Time	75			90			ns	
t_{EN}	Output Enable Time			150			190	ns	

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

eceiver Operation

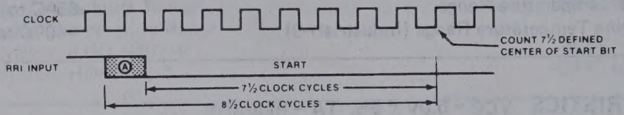
Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Ⓐ A low level on DRReset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. Ⓒ 1 clock cycle later DReady is reset to a logic high, and FError is evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



RECEIVER TIMING (NOT TO SCALE)

Start Bit Detection

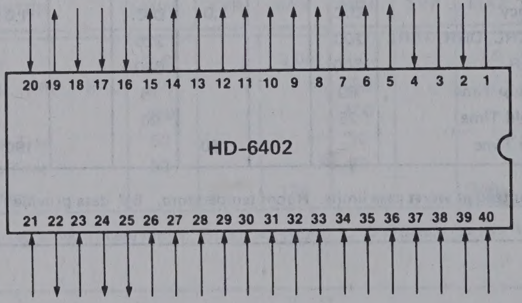
The receiver uses a 16X clock for timing. Ⓐ The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symetrical square wave, the center of the start bit will be located within $\pm\frac{1}{2}$ clock cycle, $\pm\frac{1}{32}$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Pin Assignment And Functions

PIN	SYMBOL	DESCRIPTION
1	VCC	Positive Voltage Supply
2	NC	No Connection
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 - RBR8
7	RBR6	See Pin 5 - RBR8
8	RBR5	See Pin 5 - RBR8
9	RBR4	See Pin 5 - RBR8
10	RBR3	See Pin 5 - RBR8
11	RBR2	See Pin 5 - RBR8
12	RBR1	See Pin 5 - RBR8
13	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.

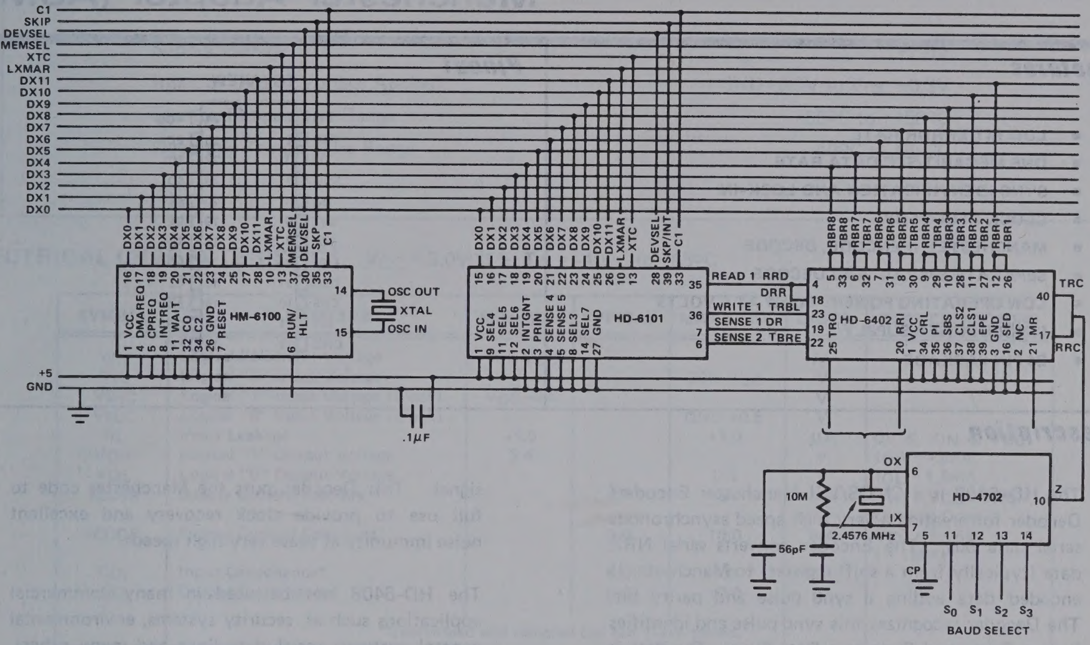
PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the received buffer register.
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	DRR	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the receiver buffer register. **This input must be pulsed at least once after power up.**



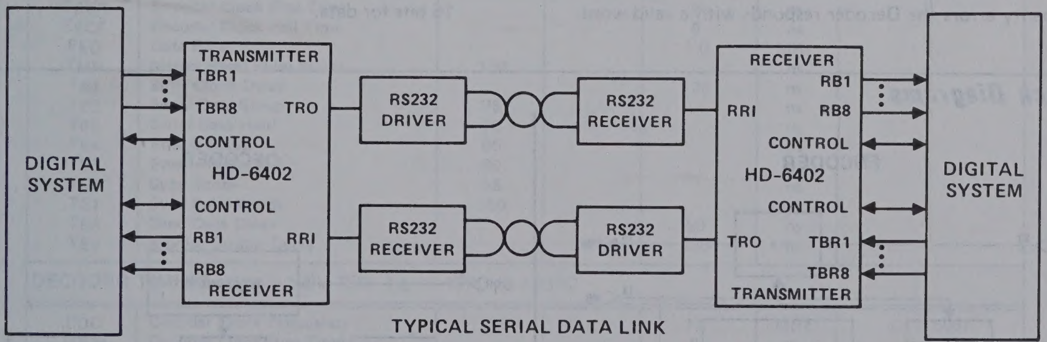
PIN	SYMBOL	DESCRIPTION
22	TBRE	A high level on TRANMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL indicates data transfer to the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 - TBR1
28	TBR3	See Pin 26 - TBR1

PIN	SYMBOL	DESCRIPTION
29	TBR4	See Pin 26 - TBR1
30	TBR5	See Pin 26 - TBR1
31	TBR6	See Pin 26 - TBR1
32	TBR7	See Pin 26 - TBR1
33	TBR8	See Pin 26 - TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI	A high level on PARITY INHIBIT inhibits parity generation. Parity checking and forces PE output low.
36	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits)
38	CLS1	See Pin 37 - CLS2
39	EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

Interfacing With The 6402


C1
SKIP
DEVSEL
MEMSEL
XTC
LXMAR
DX11
DX10
DX9
DX8
DX7
DX6
DX5
DX4
DX3
DX2
DX1
DX0
HM-6100
VCC
DMAREQ
CPREQ
INTREQ
WAIT
CO
C2
GND
RESET
RUN/HLT
OSC OUT
XTAL
OSC IN
+5
GND
.1µF
HD-6101
VCC
SEL4
SEL5
SEL6
INTGNT
PRIN
SENSE 4
SENSE 5
SEL3
SEL7
GND
SKP/INT
READ 1 RRD
DRR
WRITE 1 TBRL
SENSE 1 DR
SENSE 2 TBRE
HD-6402
RBR8
RBR1
TBR8
TBR1
TRO
RRI
CRL
PI
SBS
CLS2
CLS1
EPE
SFD
NC
MR
TRC
RRC
HD-4702
OX
IX
Z
CP
10M
2.4576 MHz
56pF
S0
S1
S2
S3
BAUD SELECT

The bit rate generator is shown supplying the transmit and receive clocks for the UART.


DIGITAL SYSTEM
TRANSMITTER
TBR1
TBR8
TRO
CONTROL
HD-6402
CONTROL
RB1
RRI
RB8
RECEIVER
RS232 DRIVER
RS232 RECEIVER
RS232 RECEIVER
RS232 DRIVER
RECEIVER
RB1
RRI
RB8
CONTROL
HD-6402
CONTROL
TRO
TBR1
TBR8
TRANSMITTER
DIGITAL SYSTEM

TYPICAL SERIAL DATA LINK

Switching Waveforms

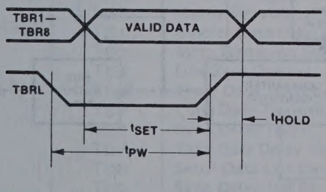

TBR1—TBR8
VALID DATA
TBRL
tSET
tHOLD
tPW

FIGURE 1

Data Input Cycle

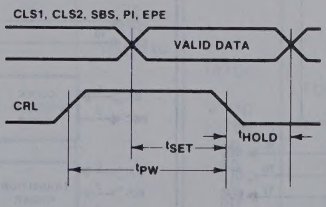

CLS1, CLS2, SBS, PI, EPE
VALID DATA
CRL
tSET
tHOLD
tPW

FIGURE 2

Control Register Load Cycle

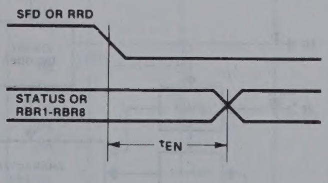

SFD OR RRD
STATUS OR RBR1-RBR8
tEN

FIGURE 3

Status Flag Output Enable Time or Data Output Enable Time

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

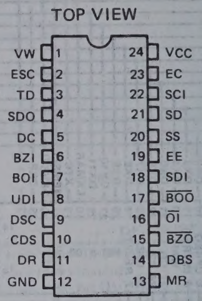
HD-6408

CMOS Asynchronous Serial Manchester Adapter (ASMA)

Features

- LOW BIT ERROR RATE
- ONE MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- SINGLE POWER SUPPLY
- 24 PIN PACKAGE

Pinout

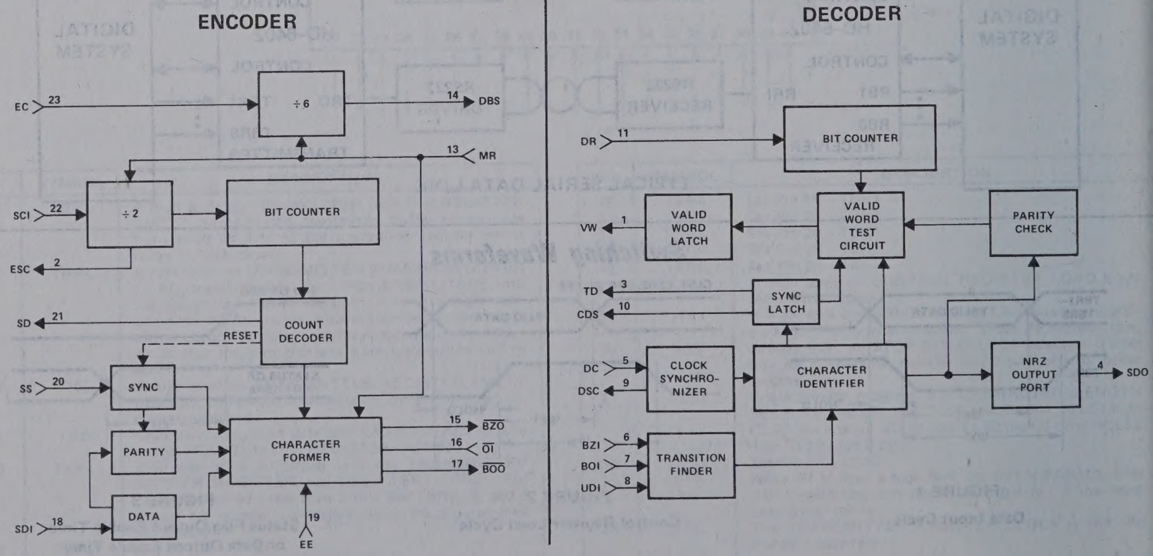

TOP VIEW
VW 1
ESC 2
TD 3
SDO 4
DC 5
BZI 6
BOI 7
UDI 8
DSC 9
CDS 10
DR 11
GND 12
24 VCC
23 EC
22 SCI
21 SD
20 SS
19 EE
18 SDI
17 BOO
16 OI
15 BZO
14 DBS
13 MR

Description

The HD-6408 is a CMOS/LSI Manchester Encoder/Decoder for creating a very high speed asynchronous serial data bus. The Encoder converts serial NRZ data (typically from a shift register) to Manchester II encoded data adding a sync pulse and parity bit. The Decoder recognizes this sync pulse and identifies it as a Command Sync or a Data Sync. The data is then decoded and shifted out in the NRZ code (typically into a shift register). Finally, the parity bit is checked. If there were no Manchester or parity errors the Decoder responds with a valid word signal. This Decoder puts the Manchester code to full use to provide clock recovery and excellent noise immunity at these very high speeds.

The HD-6408 can be used in many commercial applications such as, security systems, environmental control systems, serial data links and many others. It utilizes a single 12X clock and achieves data rates of up to one million bits per second with a very minimum overhead of only 4 bits out of 20, leaving 16 bits for data.

Block Diagrams


ENCODER
EC 23
÷ 6
14 DBS
13 MR
SCI 22
÷ 2
BIT COUNTER
ESC 2
SD 21
COUNT DECODER
RESET
SS 20
SYNC
PARITY
CHARACTER FORMER
15 BZO
16 OI
17 BOO
SDI 18
DATA
19 EE
DECODER
DR 11
BIT COUNTER
VW 1
VALID WORD LATCH
VALID WORD TEST CIRCUIT
PARITY CHECK
TD 3
CDS 10
SYNC LATCH
DC 5
DSC 9
CLOCK SYNCHRO-NIZER
CHARACTER IDENTIFIER
NRZ OUTPUT PORT
4 SDO
BZI 6
BOI 7
UDI 8
TRANSITION FINDER

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HD-6408-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = -40°C to +85°C

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
I_{IL}	Input Leakage	-1.0		+1.0	μA	0V ⩽ V_{IN} ⩽ V_{CC}
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
I_{CCSB}	Supply Current Standby		0.5	2	mA	V_{IN} = V_{CC} = 5.25V Outputs Open
I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.25V, f = 1MHz
C_{IN}	Input Capacitance*		5.0	7.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed and sampled but not 100% tested.

ENCODER TIMING V_{CC} = 5.0V ±5% T_A = -40°C to +85°C

A.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
F_{EC}	Encoder Clock Frequency			12	MHz	C_L = 50pF
F_{ESC}	Send Clock Frequency			2.0	MHz	
T_{ECR}	Encoder Clock Rise Time			8	ns	
T_{ECF}	Encoder Clock Fall Time			8	ns	
F_{ED}	Data Rate			1.0	MHz	
T_{MR}	Master Reset Pulse Width	150			ns	
T_{E1}	Shift Clock Delay			125	ns	
T_{E2}	Serial Data Setup	75			ns	
T_{E3}	Serial Data Hold	75			ns	
T_{E4}	Enable Setup	90			ns	
T_{E5}	Enable Pulse Width	80			ns	
T_{E6}	Sync Setup	55			ns	
T_{E7}	Sync Pulse Width	150			ns	
T_{E8}	Send Data Delay			50	ns	
T_{E9}	Bipolar Output Delay			130	ns	

DECODER TIMING V_{CC} = 5.0V ±5% T_A = -40°C to +85°C

A.C.

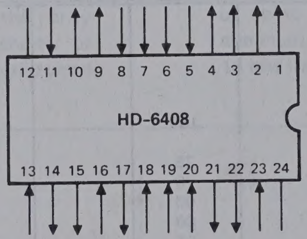
SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
F_{DC}	Decoder Clock Frequency			12	MHz	C_L = 50pF
T_{DCR}	Decoder Clock Rise Time			8	ns	
T_{DCF}	Decoder Clock Fall Time			8	ns	
F_{DD}	Data Rate			1.0	MHz	
T_{DR}	Decoder Reset Pulse Width	150			ns	
T_{DRS}	Decoder Reset Setup Time	75			ns	
T_{MR}	Master Reset Pulse Width	150			ns	
T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	①
T_{D2}	Sync Transition Span		18T_{DC}		ns	①
T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
T_{D4}	Short Data Transition Span		6T_{DC}		ns	①
T_{D5}	Long Data Transition Span		12T_{DC}		ns	①
T_{D6}	Sync Delay (ON)		40	110	ns	
T_{D7}	Take Data Delay (ON)		50	110	ns	
T_{D8}	Serial Data Out Delay		70	80	ns	
T_{D9}	Sync Delay (OFF)		90	110	ns	
T_{D10}	Take Data Delay (OFF)		90	110	ns	
T_{D11}	Valid Word Delay		90	110	ns	

NOTE ① : 15T_{DC} +10 = [15 (Decoder Clock Period)] +10ns T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

Pin Assignment and Functions

PIN	SYMBOL	SECTION	DESCRIPTION
1	VW	Decoder	Output high indicates receipt of a VALID WORD.
2	ESC	Encoder	ENCODER SHIFT CLOCK is an output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	TD	Decoder	TAKE DATA output is high during receipt of data after identification of a sync pulse.
4	SDO	Decoder	SERIAL DATA OUT delivers received data in correct NRZ format.
5	DC	Decoder	DECODER CLOCK input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	BZI	Decoder	A high input should be applied to BIPOLAR ZERO IN when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	BOI	Decoder	A high input should be applied to BIPOLAR ONE IN when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	UDI	Decoder	With pin 6 high and pin 7 low, this pin enters UNIPOLAR DATA IN to the transition finder circuit. If not used this input must be held low.
9	DSC	Decoder	DECODER SHIFT CLOCK output delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	CDS	Decoder	COMMAND/DATA SYNC output high occurs during output of decoded data which was preceded by a Command synchronizing character. A low output indicates a Data synchronizing character.
11	DR	Decoder	A high input to DECODER RESET during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	GND	Both	GROUND supply pin.



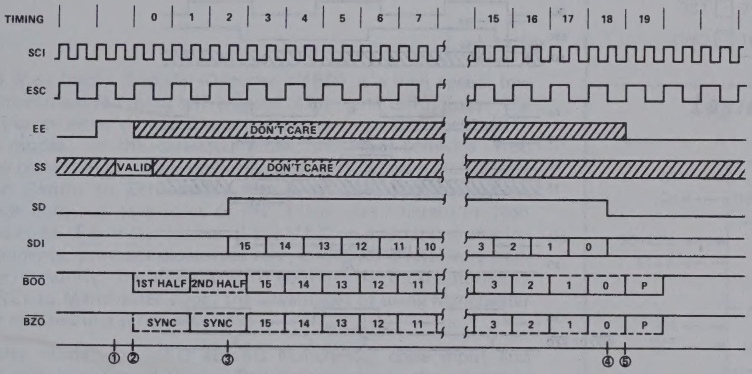
PIN	SYMBOL	SECTION	DESCRIPTION
13	MR	Both	A high on MASTER RESET clears the 2:1 counters in both the encoder and decoder and the ÷ 12 counter.
14	DBS	Encoder	DIVIDE BY SIX is an output from 6:1 divider which is driven by the ENCODER CLOCK.
15	$\overline{\text{BZO}}$	Encoder	$\overline{\text{BIPOLAR}}$ $\overline{\text{ZERO}}$ $\overline{\text{OUT}}$ is an active low output designed to drive the zero or negative sense of a bipolar line driver.
16	$\overline{\text{OI}}$	Encoder	A low on $\overline{\text{OUTPUT INHIBIT}}$ forces pin 15 and 17 high, their inactive states.
17	$\overline{\text{BOO}}$	Encoder	$\overline{\text{BIPOLAR}}$ $\overline{\text{ONE}}$ $\overline{\text{OUT}}$ is an active low output designed to drive the one or positive sense of a bipolar line driver.
18	SDI	Encoder	SERIAL DATA IN accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	EE	Encoder	A high on ENCODER ENABLE initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	SS	Encoder	SYNC SELECT actuates a Command sync for an input high and Data sync for an input low.
21	SD	Encoder	SEND DATA is an active high output which enables the external source of serial data.
22	SCI	Encoder	SEND CLOCK IN is 2X the Encoder data rate.
23	EC	Encoder	ENCODER CLOCK is the input to the 6:1 divider.
24	VCC	Both	Positive supply pin.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SClock input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SClock by dividing the DClock.

The Encoder's cycle begins when EE is high during a falling edge of ESC ①. This cycle lasts for one word length or twenty ESC periods. At the next low-to-high transition of the ESC, a high at SS input actuates a Command sync or a low will produce a Data sync for that word ②. When the Encoder is ready to accept data, the SD output will go high and remain high for sixteen ESC periods ③ – ④. During these sixteen periods the data should be clocked into the SDInput with every high-to-low transition of the ESC ③ – ④. After the sync and Manchester II encoded data are transmitted through the $\overline{\text{BOO}}$ and $\overline{\text{BZO}}$ outputs, the Encoder adds on an additional bit which is the (odd) parity for that word ⑤. At any time a low on $\overline{\text{OI}}$ will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MR. Any time after or during this pulse, a low-to-high transition on SCI clears the internal counters an initializes the Encoder for a new word.



Decoder Operation

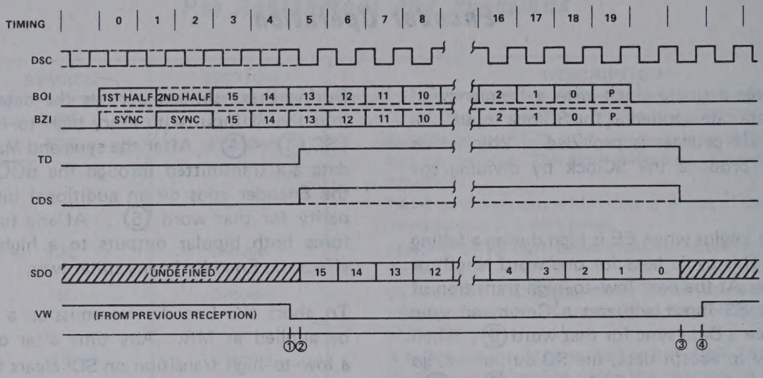
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DClock input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BOI and BZI inputs will accept data from a differential output comparator. The UDI input can only accept noninverted Manchester II coded data (e.g. from $\overline{\text{BZO}}$ of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by the CDS output. If the sync character was a command, this output will go high ② and remain high for sixteen DSC periods ③, otherwise it will remain low. The TD output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SDO.

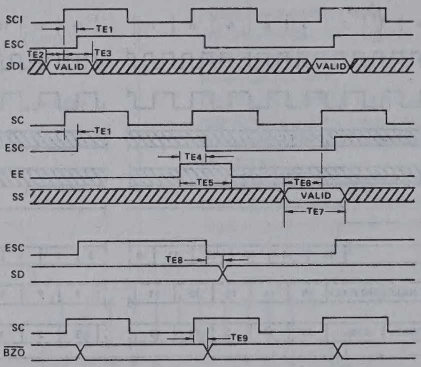
The decoded data available at SDO is in a NRZ format. The DSC is provided so that the decoded bits can get shifted into an external register on every low-to-high transition for this clock ② – ③.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VW output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

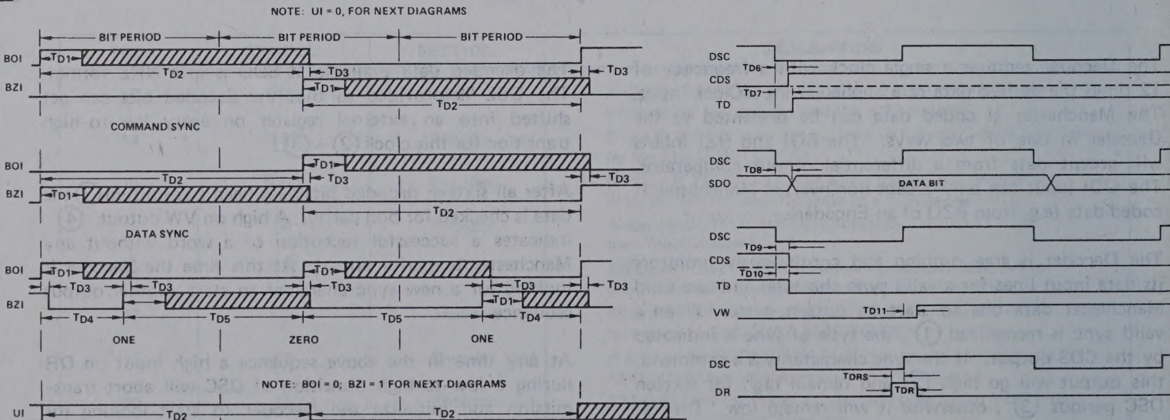
At any time in the above sequence a high input on DR during a low-to-high transition of DSC will abort transmission and initialize the Decoder to start looking for a new sync character.


TIMING
0
1
2
3
4
5
6
7
8
16
17
18
19
DSC
BOI
1ST HALF
2ND HALF
15
14
13
12
11
10
2
1
0
P
BZI
SYNC
SYNC
TD
CDS
SDO
UNDEFINED
15
14
13
12
4
3
2
1
0
VW
(FROM PREVIOUS RECEPTION)
①②
③ ④

Encoder Timing


SCI
ESC
SDI
TE1
TE2
TE3
VALID
VALID
SC
ESC
EE
SS
TE1
TE4
TE5
TE6
TE7
VALID
ESC
SD
TE8
SC
BOO OR BZO
TE9

Decoder Timing


NOTE: UI = 0, FOR NEXT DIAGRAMS
BIT PERIOD
BIT PERIOD
BIT PERIOD
BOI
BZI
TD1
TD2
TD3
COMMAND SYNC
DATA SYNC
TD4
TD5
ONE
ZERO
ONE
NOTE: BOI = 0; BZI = 1 FOR NEXT DIAGRAMS
UI
COMMAND SYNC
DATA SYNC
ONE
ZERO
ONE
ONE
DSC
CDS
TD
TD6
TD7
DSC
SDO
TD8
DATA BIT
DSC
CDS
TD
VW
TD9
TD10
TD11
DSC
DR
TDRS
TDR

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6409

CMOS Manchester Encoder-Decoder (MED)

Features

- CONVERTER OR REPEATER MODE
- INDEPENDENT MANCHESTER ENCODER AND DECODER OPERATION
- ONE MEGABIT/SEC DATA RATE
- LOW BIT ERROR RATE
- DIGITAL PLL CLOCK RECOVERY
- ON CHIP OSCILLATOR
- SINGLE POWER SUPPLY
- LOW OPERATING POWER: 25mW AT 5 VOLTS
- FULL INDUSTRIAL TEMPERATURE RANGE
- 20 PIN PACKAGE

Description

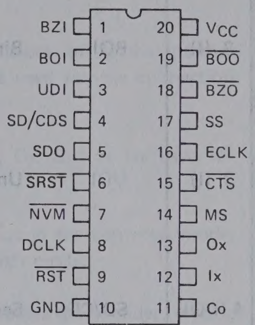
The HD-6409 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Non Return to Zero code (NRZ) into Manchester code and decodes Manchester code into Non Return to Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Non Return to Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This is to minimize the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 25mW of power.

Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative.

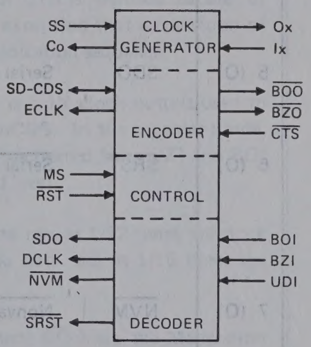
Pinout

TOP VIEW



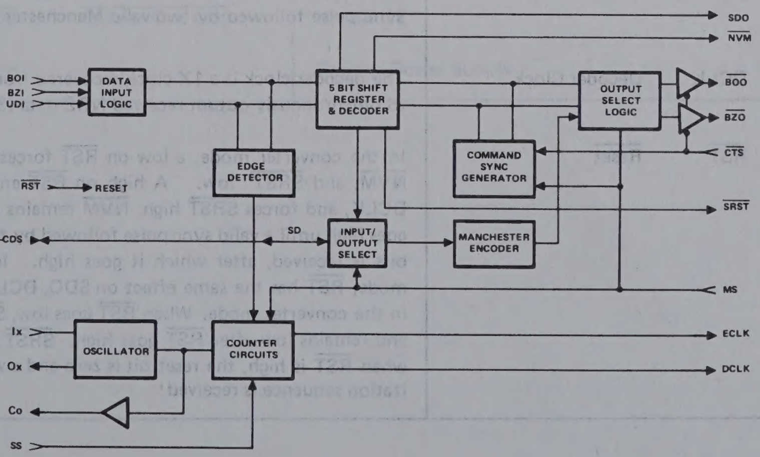
BZI 1
BOI 2
UDI 3
SD/CDS 4
SDO 5
SRST 6
NVM 7
DCLK 8
RST 9
GND 10
20 VCC
19 BOO
18 BZO
17 SS
16 ECLK
15 CTS
14 MS
13 Ox
12 Ix
11 Co

Logic Symbol



SS
Co
CLOCK GENERATOR
Ox
Ix
SD-CDS
ECLK
ENCODER
BOO
BZO
CTS
MS
RST
CONTROL
SDO
DCLK
NVM
SRST
DECODER
BOI
BZI
UDI

Functional Diagram



SDO
NVM
BOI
BZI
UDI
DATA INPUT LOGIC
5 BIT SHIFT REGISTER & DECODER
OUTPUT SELECT LOGIC
BOO
BZO
CTS
EDGE DETECTOR
COMMAND SYNC GENERATOR
RST
RESET
SRST
SD
SD-CDS
INPUT/ OUTPUT SELECT
MANCHESTER ENCODER
MS
Ix
OSCILLATOR
Ox
COUNTER CIRCUITS
ECLK
DCLK
Co
SS

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

Pin Assignment And Functions

PIN	MNEMONIC NAME		DESCRIPTION
1 (I)	BZI	Bipolar Zero Input	Used in conjunction with pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder. BZI and BOI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high.
2 (I)	BOI	Bipolar One Input	Used in conjunction with pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder. BOI and BZI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low.
3 (I)	UDI	Unipolar Data Input	An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) is used to input Manchester II encoded data to the decoder. When using pin 1 (BZI) and pin 2 (BOI) for data input, UDI must be held low.
4 (I/O)	SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
5 (O)	SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when $\overline{\text{RST}}$ is low.
6 (O)	$\overline{\text{SRST}}$	$\overline{\text{Serial Reset}}$	In the converter mode, $\overline{\text{SRST}}$ follows $\overline{\text{RST}}$. In the repeater mode, when $\overline{\text{RST}}$ goes low, $\overline{\text{SRST}}$ goes low and remains low after $\overline{\text{RST}}$ goes high. $\overline{\text{SRST}}$ goes high only when $\overline{\text{RST}}$ is high, the reset bit is zero, and a valid synchronization sequence is received.
7 (O)	$\overline{\text{NVM}}$	$\overline{\text{Nonvalid Manchester}}$	A low on $\overline{\text{NVM}}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. $\overline{\text{NVM}}$ is set low by a low on $\overline{\text{RST}}$, and remains low after $\overline{\text{RST}}$ goes high until valid sync pulse followed by two valid Manchester bits is received.
8 (O)	DCLK	Decoder Clock	The decoder clock is a 1X clock recovered from BZI and BOI to synchronously output received NRZ data (SDO).
9 (I)	$\overline{\text{RST}}$	$\overline{\text{Reset}}$	In the converter mode, a low on $\overline{\text{RST}}$ forces SDO, DCLK, $\overline{\text{NVM}}$, and $\overline{\text{SRST}}$ low. A high on $\overline{\text{RST}}$ enables SDO and DCLK, and forces $\overline{\text{SRST}}$ high. $\overline{\text{NVM}}$ remains low after $\overline{\text{RST}}$ goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, $\overline{\text{RST}}$ has the same effect on SDO, DCLK and $\overline{\text{NVM}}$ as in the converter mode. When $\overline{\text{RST}}$ goes low, $\overline{\text{SRST}}$ goes low and remains low after $\overline{\text{RST}}$ goes high. $\overline{\text{SRST}}$ goes high only when $\overline{\text{RST}}$ is high, the reset bit is zero and a valid synchronization sequence is received.

(I) - Input

(O) - Output

Pin Assignment And Functions (Continued)

PIN	MNEMONIC	NAME	DESCRIPTION
10 (I)	GND	Ground	Ground
11 (O)	Co	Clock Output	Buffered output of clock input Ix. May be used as clock signal for other peripherals.
12 (I)	Ix	Clock Input	Ix is the input for an external clock or, if the internal oscillator is used, Ix and Ox are used for the connection of the crystal.
13 (I)	Ox	Clock Drive	If the internal oscillator is used, Ox and Ix are used for the connection of the crystal.
14 (I)	MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
15 (I)	$\overline{\text{CTS}}$	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{\text{BOO}}$, $\overline{\text{BZO}}$ high and ECLK low. A high to low transition of $\overline{\text{CTS}}$ initiates transmission of a Command sync pulse. A low on $\overline{\text{CTS}}$ enables $\overline{\text{BOO}}$, $\overline{\text{BZO}}$, and ECLK. In the repeater mode, the function of $\overline{\text{CTS}}$ is identical to that of the converter mode with the exception that a transition of $\overline{\text{CTS}}$ does not initiate a synchronization sequence.
16 (O)	ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.
17 (I)	SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
18 (O)	$\overline{\text{BZO}}$	Bipolar Zero Output	$\overline{\text{BZO}}$ and its logical complement $\overline{\text{BOO}}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
19 (O)	$\overline{\text{BOO}}$	Bipolar One Out	see pin 18
20 (I)	V_{CC}	V_{CC}	Positive Power Supply

(I) - Input
(O) - Output

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Storage Temperature Range	-65°C to +150°C
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3	Operating Temperature Range	
		Industrial HD-6409-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

DC

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}	–		V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
V_{IHR}	Logical "1" Input Voltage ($\overline{\text{Reset}}$)	60% V_{CC}			V	
V_{TLR}	Logical "0" Input Voltage ($\overline{\text{Reset}}$)			40% V_{CC}	V	
V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
I_{IL}	Input Leakage	-1.0		+1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4			V	I_{OH} = 2.0mA
V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = -2.0mA
I_{CCQ}	Supply Current Quiescent		50	100	µA	$V_{IN} = V_{CC}$ = 5.5V, Outputs open
I_{CCOP}	Supply Current Operating *		5.0	12.0	mA	V_{CC} = 5.5V, f_{co} = 16MHz
C_{IN}	Input Capacitance *		5.0	7.0	pF	
C_{OUT}	Output Capacitance *		8.0	15.0	pF	
f_c	Clock Frequency		16		MHz	I_x or X_{tal}
t_c	Clock Period		$1/f_c$		s	
t_1	Bipolar Pulse Width	t_c -10			ns	
t_2	Sync Transition Span		1.5 x CR x t_c ①②		ns	
t_3	One-Zero Overlap			t_c -10	ns	
t_4	Short Data Transition Span		0.5 x CR x t_c ①②		ns	
t_5	Long Data Transition Span		CR x t_c		ns	
t_6	Output Rise & Fall Time			50	ns	CL = 20pF for Co, 50pF otherwise
	Clock Out Rise & Fall Time			(5 x f_c)	1/s	
t_7	Input Rise & Fall Time			(5 x f_c)	1/s	

AC

CONVERTER MODE

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	TEST CONDITIONS
ENCODER SECTION						
t_{CE1}	SD Setup Time			70	ns	
t_{CE2}	SD Hold Time			0	ns	
t_{CE3}	SD to $\overline{\text{BZO}}$ Prop Delay		2		DBP ③	
t_{CE4}	$\overline{\text{CTS}}$ Low to ECLK, $\overline{\text{BOO}}$, $\overline{\text{BZO}}$ Enabled			29	t_c	
t_{CE5}	$\overline{\text{CTS}}$ High to ECLK, $\overline{\text{BOO}}$, $\overline{\text{BZO}}$ Disabled			41	t_c	
DECODER SECTION						
t_{CD1}	UDI to SDO, $\overline{\text{NVM}}$	2.5		3	DBP ③	
t_{CD2}	DCLK to SDO, $\overline{\text{NVM}}$			40	ns	
t_{CD3}	$\overline{\text{RST}}$ Low to DCLK, SDO, $\overline{\text{SRST}}$, $\overline{\text{NVM}}$ Low		0.5	1.5	DBP ③	CL = 50pF
t_{CD4}	$\overline{\text{RST}}$ High to DCLK, SDO $\overline{\text{NVM}}$ Enable		0.5	1.5	DBP ③	CL = 50pF

REPEATER MODE

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	TEST CONDITIONS
t_{R1}	UDI to $\overline{\text{BOO}}$, $\overline{\text{BZO}}$		1		DBP ③	
t_{R2}	ECLK to $\overline{\text{BZO}}$			40	ns	
t_{R3}	ECLK to $\overline{\text{SRST}}$			70	ns	
t_{R4}	UDI to SDO, $\overline{\text{NVM}}$	2.5		3	DBP ③	

NOTES:

① CR - Clock Rate, either 16X or 32X the data rate.

② $t_c = 1/f_c$

③ DBP - Data Bit Period, i.e. for CR = 16X, one DBP = 16 clock cycles

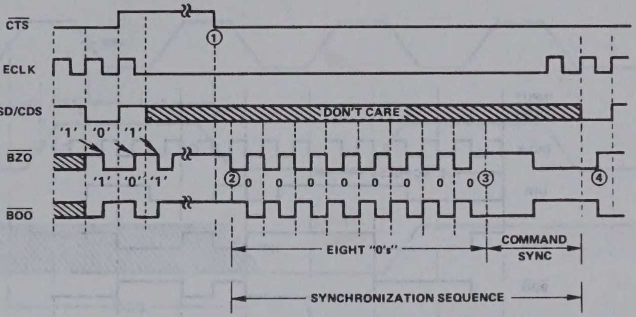
* Guaranteed and sampled but not 100% tested.

Converter Mode

ENCODER OPERATION

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock I_X for internal timing. $\overline{\text{CTS}}$ is used to control the encoder outputs, ECLK, $\overline{\text{BOO}}$ and $\overline{\text{BZO}}$. A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on $\overline{\text{CTS}}$ enables encoder outputs ECLK, $\overline{\text{BOO}}$ and $\overline{\text{BZO}}$, while a high on $\overline{\text{CTS}}$ forces $\overline{\text{BZO}}$, $\overline{\text{BOO}}$ high and holds ECLK low. When $\overline{\text{CTS}}$ goes from high to low ①, a synchronization sequence is transmitted out on $\overline{\text{BOO}}$ and $\overline{\text{BZO}}$. A synchronization sequence consists of eight Manchester "0" bits followed by a Command sync pulse. ② A Command sync pulse is a three bit wide pulse with the first 1½ bits high followed by 1½ bits low. ③ Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on $\overline{\text{BOO}}$ and $\overline{\text{BZO}}$ following the Command sync pulse. ④ Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. Manchester data out is inverted.



DECODER OPERATION

The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as this permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

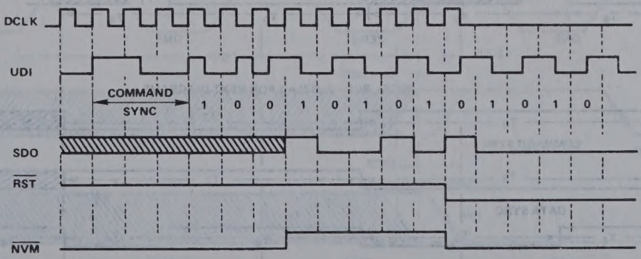
The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs will accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data, i.e. $\overline{\text{Bipolar Zero Out}}$ of an encoder. The decoder continuously monitors this Manchester data for a valid sync pattern. Note that while the MED encoder section can generate only a Command sync pattern, the decoder can recognize either a Command or Data sync pattern. A Data sync is a logically inverted Command sync.

There is a three bit delay between UDI, BOI or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the $\overline{\text{RST}}$ pin. When $\overline{\text{RST}}$ is low, SDO, DCLK and $\overline{\text{NVM}}$ are forced low. When $\overline{\text{RST}}$ is high, SDO is transmitted out synchronously with the recovered clock DCLK. The $\overline{\text{NVM}}$ output remains low after a low to high transition on $\overline{\text{RST}}$ until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is provided so that the decoded bits can be shifted into an external register on every low to high transition of this clock.

Three bit periods after an invalid Manchester bit is received on UDI, or BOI and BZI, $\overline{\text{NVM}}$ goes low synchronously with the questionable data output on SDO. Further, the decoder does not reestablish proper data decoding until another sync pattern is recognized.



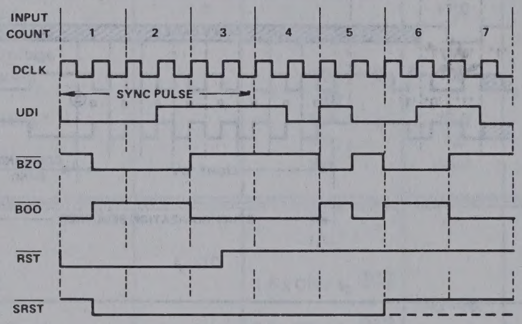
Repeater Mode

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In will accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only non-inverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

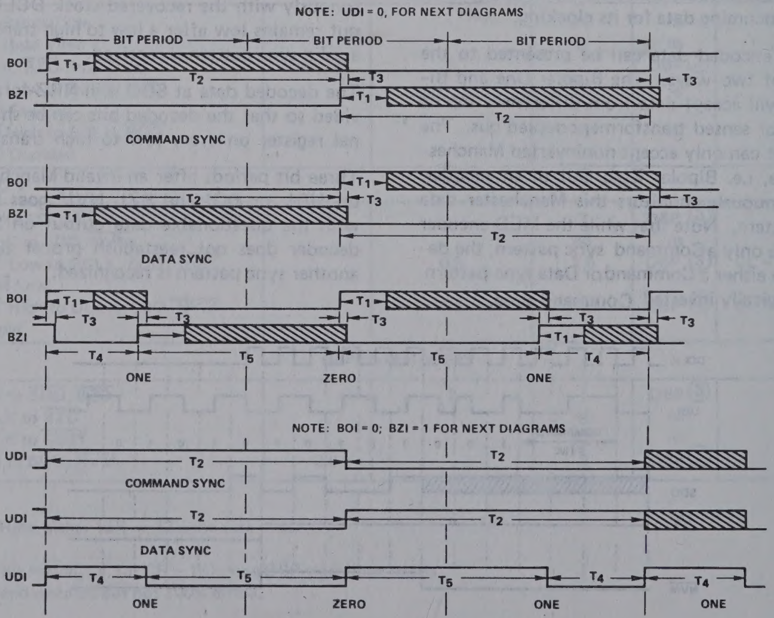
The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs $\overline{\text{BOO}}$ and $\overline{\text{BZO}}$. The 2X ECLK is transmitted out of the repeater synchronously with $\overline{\text{BOO}}$ and $\overline{\text{BZO}}$.

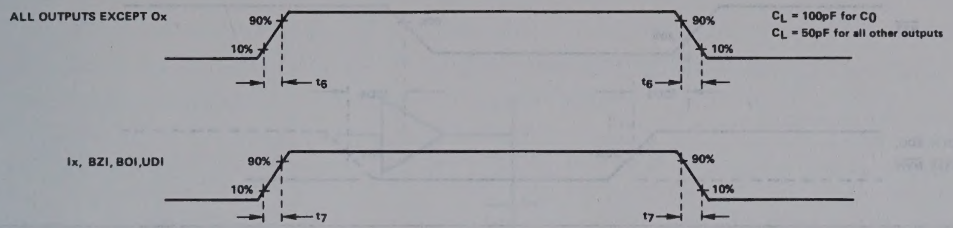
A low on $\overline{\text{CTS}}$ enables ECLK, $\overline{\text{BOO}}$, and $\overline{\text{BZO}}$. In contrast to the converter mode, a transition on $\overline{\text{CTS}}$ does not initiate a synchronization sequence of eight 0's and a Command sync. The repeater mode does recognize a Command or Data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a Command sync and low indicating a Data sync.

When $\overline{\text{RST}}$ is low, the outputs SDO, DCLK, and NVM are low, and SRST is set low. SRST remains low after $\overline{\text{RST}}$ goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. With $\overline{\text{RST}}$ high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.

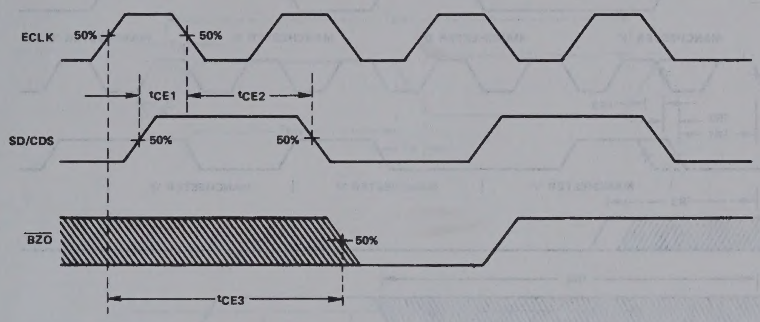

INPUT COUNT
1
2
3
4
5
6
7
DCLK
SYNC PULSE
UDI
BZO
BOO
RST
SRST

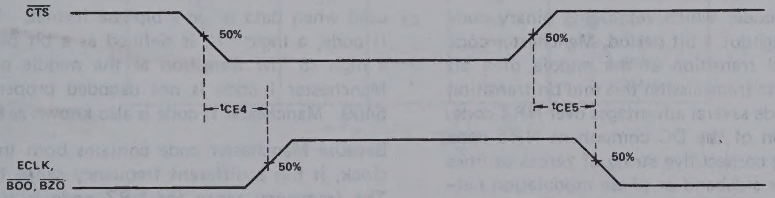
Switching Waveforms


NOTE: UDI = 0, FOR NEXT DIAGRAMS
BIT PERIOD
BIT PERIOD
BIT PERIOD
BOI
T1
T2
T3
T3
BZI
T1
T2
COMMAND SYNC
BOI
T1
T2
T3
T3
BZI
T1
T2
DATA SYNC
BOI
T1
T1
T3
T3
T3
T3
T3
BZI
T1
T4
T5
T5
T4
ONE
ZERO
ONE
NOTE: BOI = 0; BZI = 1 FOR NEXT DIAGRAMS
UDI
T2
T2
COMMAND SYNC
UDI
T2
T2
DATA SYNC
UDI
T4
T5
T5
T4
T4
ONE
ZERO
ONE
ONE

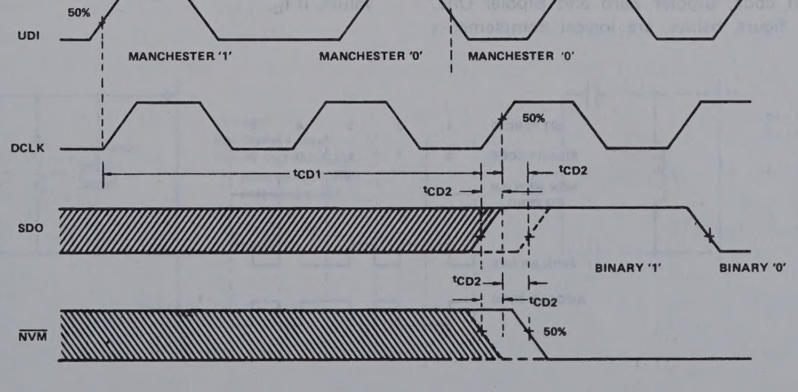

ALL OUTPUTS EXCEPT Ox
90%
10%
t_6
t_6
90%
10%
C_L = 100pF for CO
C_L = 50pF for all other outputs
Ix, BZI, BOI,UDI
90%
10%
t_7
t_7
90%
10%

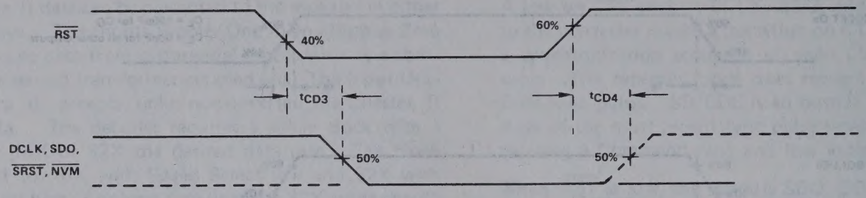
Encoder Timing


ECLK
50%
50%
t_{CE1}
t_{CE2}
SD/CDS
50%
50%
BZO
50%
t_{CE3}

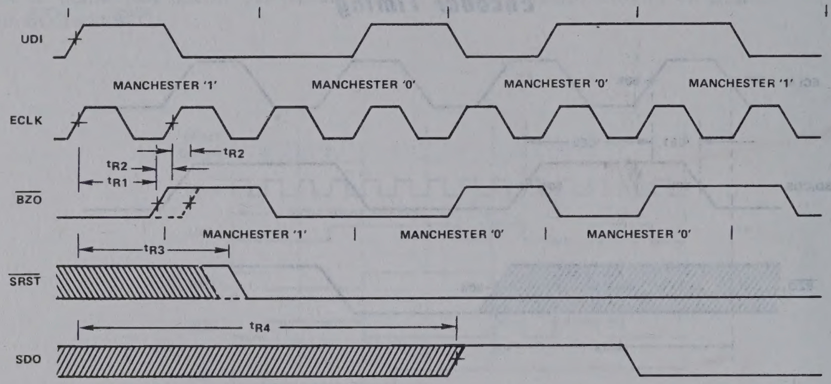

CTS
50%
50%
t_{CE4}
t_{CE5}
ECLK, BOO, BZO
50%
50%

Decoder Timing


UDI
50%
MANCHESTER '1'
MANCHESTER '0'
MANCHESTER '0'
DCLK
50%
t_{CD1}
t_{CD2}
t_{CD2}
SDO
BINARY '1'
BINARY '0'
t_{CD2}
t_{CD2}
NVM
50%


RST
40%
60%
tCD3
tCD4
DCLK, SDO,
SRST, NVM
50%
50%

Repeater Timing

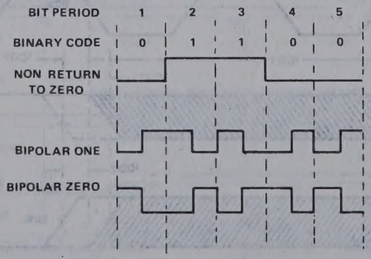

UDI
MANCHESTER '1'
MANCHESTER '0'
MANCHESTER '0'
MANCHESTER '1'
ECLK
tR2
tR2
tR1
BZO
MANCHESTER '1'
MANCHESTER '0'
MANCHESTER '0'
tR3
SRST
tR4
SDO

MANCHESTER CODE

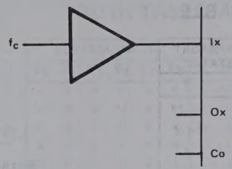
In contrast to NRZ code, which represents binary code as a static level throughout a bit period, Manchester code is based upon a level transition at the middle of a bit period. For serial data transmission this mid bit transition affords Manchester code several advantages over NRZ code. One is the elimination of the DC component NRZ code produces when a long consecutive string of zeroes or ones is transmitted. Single sideband or phase modulation networks require additional circuitry to use DC signals. Secondly, the transition can be used to recover the clock from the Manchester data, allowing the synchronization of the transmitted data with the receiver clock to occur every bit period rather than every word frame. This improves the bit error rate.

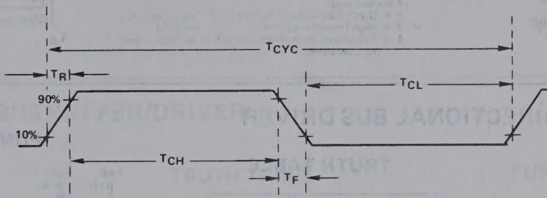
The Manchester II code, Bipolar Zero and Bipolar One, as shown in the figure below, are logical complements used when data is in a biphase format. For Manchester II code, a logic "1" is defined as a bit period containing a high to low transition at the middle of a bit period. Manchester I code is not decoded properly by the HD-6409. Manchester II code is also known as Biphase-L code.

Because Manchester code contains both the data and the clock, it has a different frequency range than NRZ code. The frequency range for NRZ code is from DC to $f_C/2$ (f_C-clock frequency), with constant unchanging logical values producing a low frequency of 0 and alternating logical values producing an upper frequency of $f_C/2$. In contrast, the low frequency for Manchester code, obtained when the logical values of data alternates, is $f_C/2$, while the high frequency represented by unchanging logical values, if f_C.


BIT PERIOD
1
2
3
4
5
BINARY CODE
0
1
1
0
0
NON RETURN
TO ZERO
BIPOLAR ONE
BIPOLAR ZERO

External Clock Mode

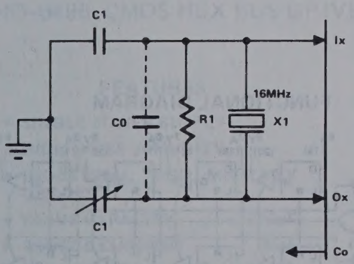



TCYC
TR
TCL
90%
10%
TCH
TF

PARAMETER	MIN	MAX	UNITS	CONDITIONS
T_{CYC}	62		ns	
T_{CH}	20		ns	
T_{CL}	20		ns	
T_R		50	ns	$f_c \leqslant 3.3MHz$
		*	ns	$f_c \geqslant 3.3MHz$
T_F		50	ns	$f_c \leqslant 3.3MHz$
		*	ns	$f_c \geqslant 3.3MHz$

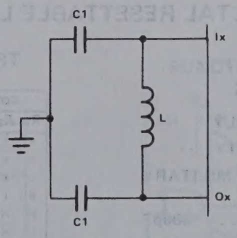
* $T_R, T_F \leqslant \frac{1}{5 f_c}$ sec

Crystal Oscillator Mode


C1
C0
R1
16MHz
X1
C1
Ix
Ox
Co

C1 = 32pF
C0 = Crystal + Stray
X1 = AT CUT PARALLEL RESONANCE FUNDAMENTAL MODE
Rs (TYP) = 30Ω
R1 = 15 MΩ

LC Oscillator Mode



C1 = 20pF
C0 = 5pF

$C_e \approx \frac{C1 - 2C0}{2}$

$f_o \approx \frac{1}{2 \pi \sqrt{LC_e}}$

CMOS Bus Driver Family

HD-6431 CMOS HEX LATCHING BUS DRIVER

FEATURES

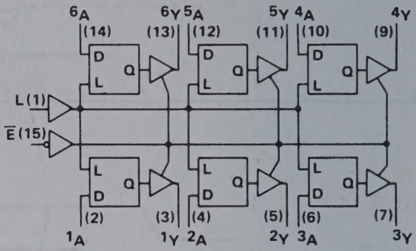
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 65nsec @ 5V

TRUTH TABLE

CONTROL INPUTS		DATA PORT STATUS	
$\overline{E}$	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	•
L	H	L	L
L	H	H	H

* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low Level

FUNCTIONAL DIAGRAM


6A
(14)
6Y
(13)
5A
(12)
5Y
(11)
4A
(10)
4Y
(9)
D
Q
L
L(1)
Ē(15)
(2)
1A
(3)
1Y
(4)
2A
(5)
2Y
(6)
3A
(7)
3Y

HD-6432 CMOS HEX BI-DIRECTIONAL BUS DRIVER

FEATURES

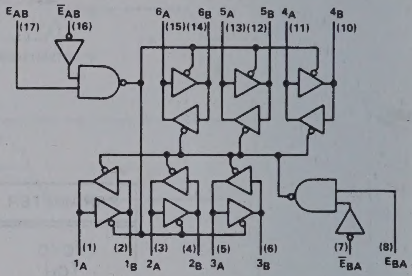
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

FUNCTIONAL DIAGRAM


EAB
(17)
ĒAB
(16)
6A
6B
(15)
(14)
5A
5B
(13)
(12)
4A
(11)
4B
(10)
(1)
1A
(2)
1B
(3)
2A
(4)
2B
(5)
3A
(6)
3B
(7)
ĒBA
(8)
EBA

HD-6433 CMOS QUAD BUS SEPARATOR/DRIVER

FEATURES

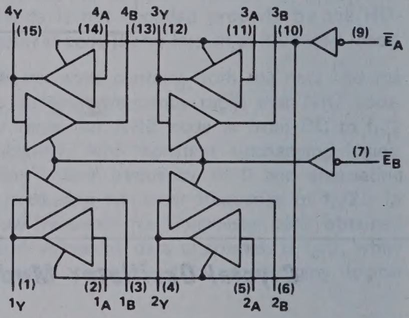
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 40nsec @ 5V

TRUTH TABLE

CONTROL INPUTS		FUNCTION		
$\overline{E}_A$	$\overline{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output, D = Disconnected

FUNCTIONAL DIAGRAM


4Y
(15)
4A
(14)
4B
(13)
3Y
(12)
3A
(11)
3B
(10)
(9)
ĒA
(7)
ĒB
(1)
1Y
(2)
1A
(3)
1B
(4)
2Y
(5)
2A
(6)
2B

HD-6434 CMOS OCTAL RESETTABLE LATCHED BUS DRIVER

FEATURES

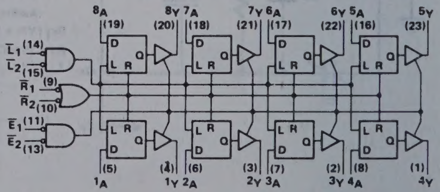
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	HI-Z
X	X	X	H	X	X	X	HI-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	•
H	H	L	L	L	↑	X	•

X = Don't Care HI-Z = High Impedance
L = Low H = High
* Data is latched to the val of the last input
↑ = Transition from a Low to High level

FUNCTIONAL DIAGRAM


8A
(19)
8Y
(20)
7A
(18)
7Y
(21)
6A
(17)
6Y
(22)
5A
(16)
5Y
(23)
L̄1 (14)
L̄2 (15)
R̄1 (9)
R̄2 (10)
Ē1 (11)
Ē2 (13)
D
Q
L R
(5)
1A
(4)
1Y
(6)
2A
(3)
2Y
(7)
3A
(2)
3Y
(8)
4A
(1)
4Y

CMOS Bus Driver Family

HD-6435 CMOS HEX RESETTABLE LATCHED BUS DRIVER

FEATURES

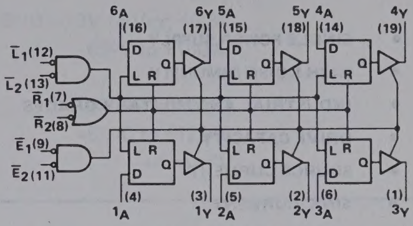
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	HI-Z
X	X	X	H	X	X	X	HI-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care HI-Z = High Impedance
L = Low H = High
* Data is latched to the value of the last input
↑ = Transition from a Low to High level

FUNCTIONAL DIAGRAM


6A (16)
6Y (17)
5A (15)
5Y (18)
4A (14)
4Y (19)
$\overline{L}_1$(12)
$\overline{L}_2$(13)
$\overline{R}_1$(7)
$\overline{R}_2$(8)
$\overline{E}_1$(9)
$\overline{E}_2$(11)
D
Q
L R
1A (4)
1Y (3)
2A (5)
2Y (2)
3A (6)
3Y (1)

HD-6436 CMOS OCTAL BUS BUFFER/DRIVER

FEATURES

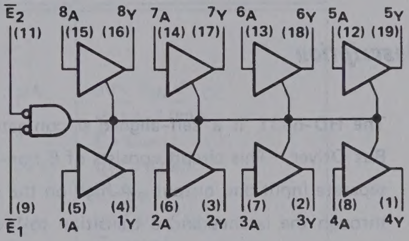
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

CONTROL		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

L = Low, H = High X = Don't Care
HI-Z = High Impedance

FUNCTIONAL DIAGRAM


$\overline{E}_2$ (11)
8A (15)
8Y (16)
7A (14)
7Y (17)
6A (13)
6Y (18)
5A (12)
5Y (19)
(9) $\overline{E}_1$
(5) 1A
(4) 1Y
(6) 2A
(3) 2Y
(7) 3A
(2) 3Y
(8) 4A
(1) 4Y

HD-6440 CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER

FEATURES

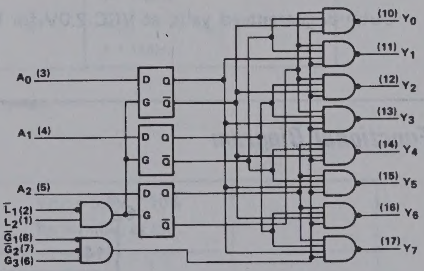
- HIGH SPEED DECODING FOR MEMORY ARRAYS
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 200pF
- SOURCE CURRENT .... 2 mA
- SINK CURRENT ...... 2.4 mA
- PROPAGATION DELAY . 65nsec @ 5V

TRUTH TABLE

INPUTS															
ENABLE					ADDRESS			OUTPUTS							
$\overline{G}_1$	$\overline{G}_2$	G_3	$\overline{L}_1$	L_2	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
X	H	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
L	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	DECODE
L	L	H	L	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	H	L	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	X	L	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H	H	X	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	

L = Low, H = High, X = Don't Care
Y_n = Data is latched to the value of the last input

FUNCTIONAL DIAGRAM


A_0 (3)
A_1 (4)
A_2 (5)
$\overline{L}_1$(2)
L_2(1)
$\overline{G}_1$(8)
$\overline{G}_2$(7)
G_3(6)
D Q
G $\overline{Q}$
(10) Y_0
(11) Y_1
(12) Y_2
(13) Y_3
(14) Y_4
(15) Y_5
(16) Y_6
(17) Y_7

HD-6495 CMOS HEX BUS DRIVER

FEATURES

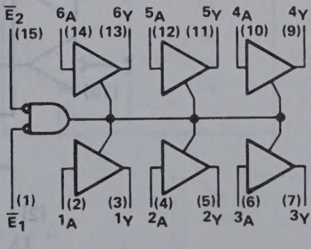
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY: 35nsec @ 5V

TRUTH TABLE

CONTROL		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = Don't Care HI-Z = High Impedance

FUNCTIONAL DIAGRAM


$\overline{E}_2$ (15)
6A (14)
6Y (13)
5A (12)
5Y (11)
4A (10)
4Y (9)
(1) $\overline{E}_1$
(2) 1A
(3) 1Y
(4) 2A
(5) 2Y
(6) 3A
(7) 3Y

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-643

CMOS HE

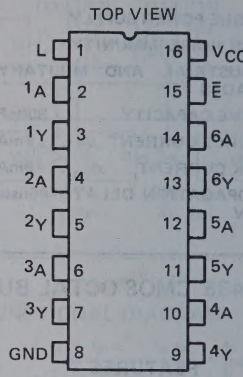
LATCHING BUS DRIVE

Features

SINGLE POWER SUPPLY	
HIGH NOISE IMMUNITY	
INDUSTRIAL AND MILITARY GRADES	
DRIVE CAPACITY	300pF
SOURCE CURRENT	4mA
SINK CURRENT	6mA
PROPAGATION DELAY	75nsec MAX.

Pinout

TOP VIEW


L 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 $\overline{E}$
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y

Description

The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control $\overline{E}$ forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

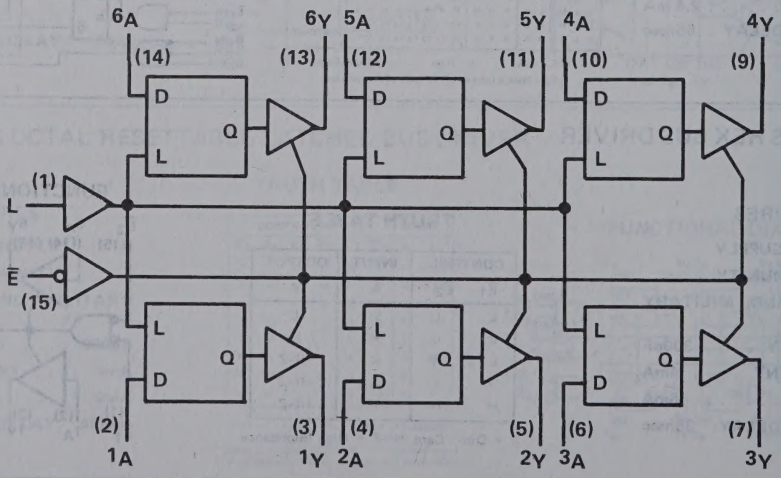
Truth Table

CONTROL INPUTS		DATA PORT STATUS	
$\overline{E}$	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low level

4

Functional Diagram


6A
(14)
6Y
(13)
5A
(12)
5Y
(11)
4A
(10)
4Y
(9)
D
L
Q
(1)
L
$\overline{E}$
(15)
(2)
1A
(3)
1Y
(4)
2A
(5)
2Y
(6)
3A
(7)
3Y

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

BSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431-9	-40°C to +85°C
Military HD-6431-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

LECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

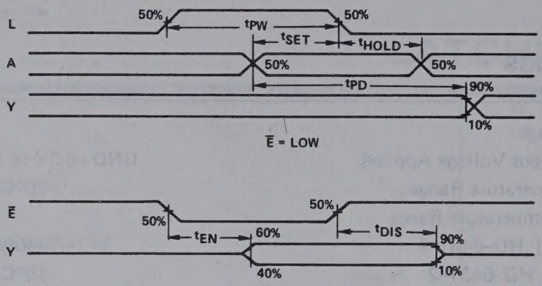
C_L = 300pF

.C.

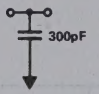
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		30		75	ns
t_{EN}	Enable Time		40		90	ns
t_{DIS}	Disable Time		40		90	ns
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PW}	Pulse Width	20		30		ns
t_R	Output Rise Time		45		90	ns
t_F	Output Fall Time		40		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

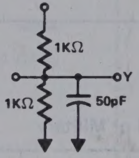
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

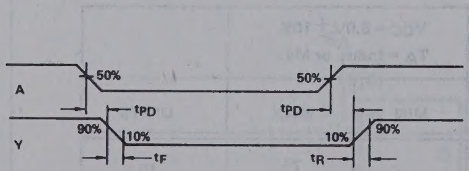


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = (\Sigma C_L)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 80\text{ns}, V_{CC} = 5.0\text{V}, \text{each } C_L = 300\text{pF}, I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{80 \times 10^{-9}} = 90\text{mA}.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



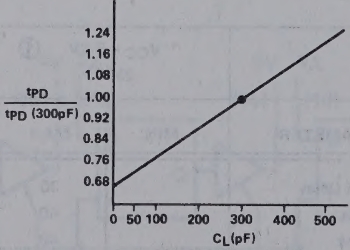


FIGURE 1

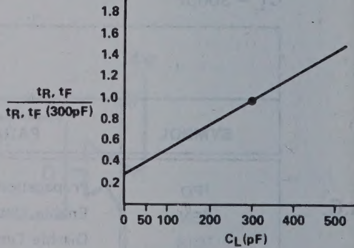


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6431-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 75nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 75 x 0.84 or 63nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 90 x 0.65 or 58nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 92nsec. The rise time was used here because it is always the worst case.

HD-6432

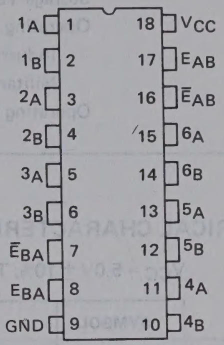
CMOS HEX BI-DIRECTIONAL BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY 55nsec MAX.

Pinout

TOP VIEW


1A 1
1B 2
2A 3
2B 4
3A 5
3B 6
$\overline{E}_{BA}$ 7
EBA 8
GND 9
18 VCC
17 EAB
16 $\overline{E}_{AB}$
15 6A
14 6B
13 5A
12 5B
11 4A
10 4B

Description

The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

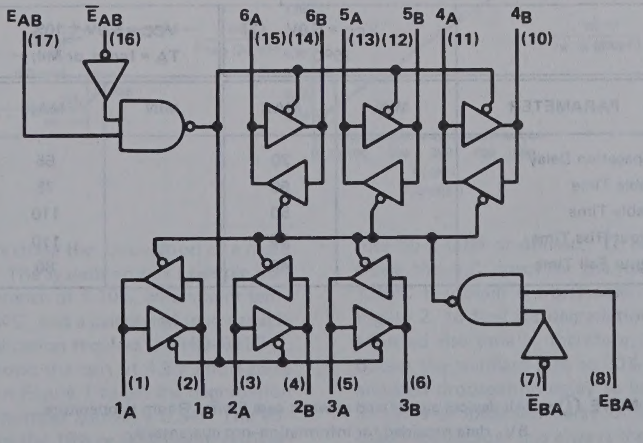
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

Functional Diagram


EAB (17)
$\overline{E}_{AB}$ (16)
6A (15)
6B (14)
5A (13)
5B (12)
4A (11)
4B (10)
(1) 1A
(2) 1B
(3) 2A
(4) 2B
(5) 3A
(6) 3B
(7) $\overline{E}_{BA}$
(8) EBA

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432-9	-40°C to +85°C
Military HD-6432-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, E_{AB} = E_{BA} = Low
I_{CC}	Supply Current		10	μA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

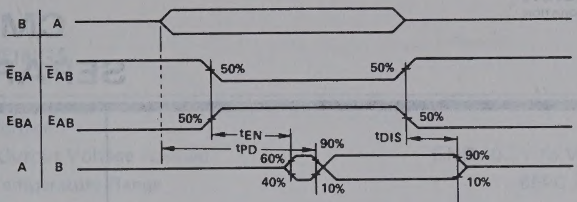
C_L = 300pF

A.C.

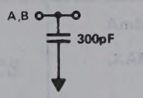
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		20		55	ns
t_{EN}	Enable Time		50		75	ns
t_{DIS}	Disable Time		50		110	ns
t_R	Output Rise Time		50		110	ns
t_F	Output Fall Time		40		80	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

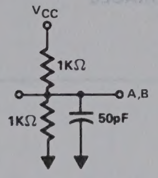
Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

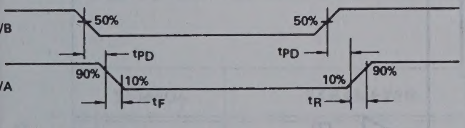


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = (\Sigma C_L)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\Big[t_R = 100\text{ns} \quad V_{CC} = 5.0\text{V} \quad \text{each } C_L = 300\text{pF} \quad I_T = (6)\,(300 \times 10^{-12})\frac{5.0 \times 0.8}{100 \times 10^{-9}} = 72\text{mA}. \Big]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 µF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

ROPAGATION DELAYS



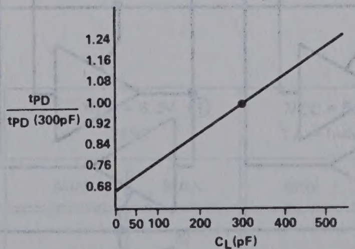


FIGURE 1

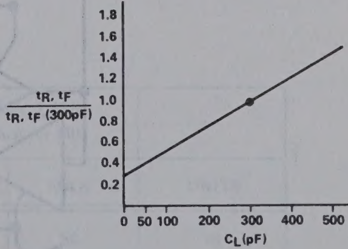


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6432-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 55nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 55 x 0.84 or 46nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 110nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 110 x 0.65 or 72nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 82nsec. The rise time was used here because it is always the worst case.

HD-6433

CMOS QUAD BUS SEPARATOR/DRIVER

Features

• SINGLE POWER SUPPLY	
• HIGH NOISE IMMUNITY	
• INDUSTRIAL AND MILITARY GRADES	
• DRIVE CAPACITY	300pF
• SOURCE CURRENT	4mA
• SINK CURRENT	6mA
• PROPAGATION DELAY	50nsec MAX.

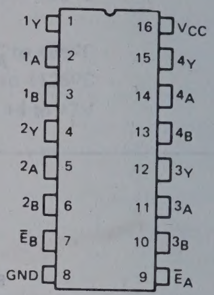
Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

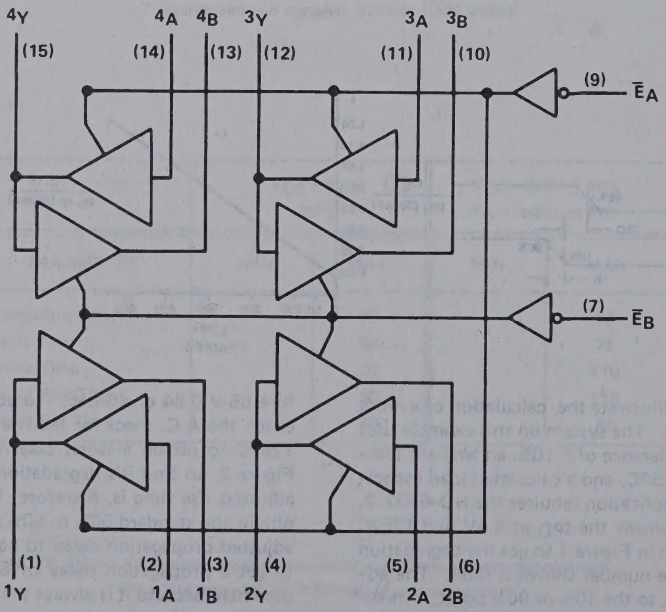

1_Y 1
1_A 2
1_B 3
2_Y 4
2_A 5
2_B 6
$\bar{E}_B$ 7
GND 8
16 V_{CC}
15 4_Y
14 4_A
13 4_B
12 3_Y
11 3_A
10 3_B
9 $\bar{E}_A$

Truth Table

CONTROL INPUTS		FUNCTION		
$\bar{E}_A$	$\bar{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output,
D = Disconnected

Functional Diagram


4_Y
(15)
4_A
(14)
4_B
(13)
3_Y
(12)
3_A
(11)
3_B
(10)
(9)
$\bar{E}_A$
(7)
$\bar{E}_B$
(1)
1_Y
(2)
1_A
(3)
1_B
(4)
2_Y
(5)
2_A
(6)
2_B

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433-9	-40°C to +85°C
Military HD-6433-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	µA	$0V \leq V_O \leq V_{CC}$ $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		10	µA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

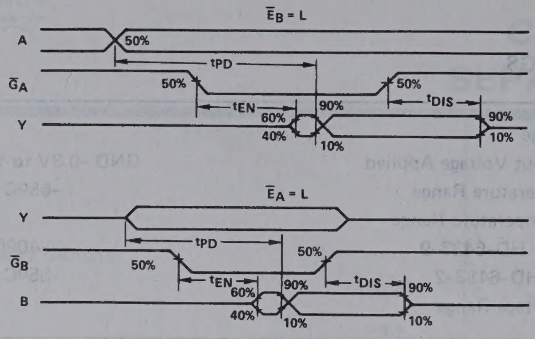
C_L = 300pF

A.C.

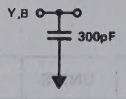
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% TA = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		20		50	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		60		100	ns
t_R	Output Rise Time		50		95	ns
t_F	Output Fall Time		45		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

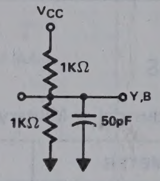
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

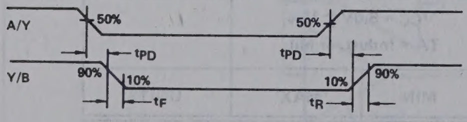


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\Big[$ t_R = 85ns, V_{CC} = 5.0V, each C_L = 300pF, $I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 56.5\text{mA}.\Big]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



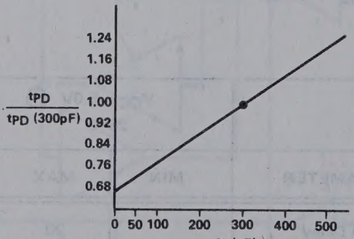


FIGURE 1

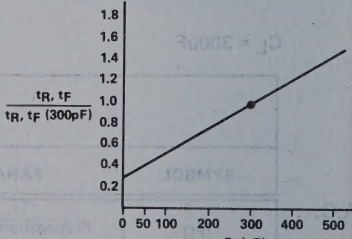


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6433-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 50nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 50 x 0.84 or 42nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 73nsec. The rise time was used here because it is always the worst case.

HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6434

CMOS OCTAL RESETTABLE LATCHED BUS DRIVER

Features

• SINGLE POWER SUPPLY	
• HIGH NOISE IMMUNITY	
• INDUSTRIAL AND MILITARY GRADES	
• DRIVE CAPACITY	300pF
• SOURCE CURRENT	6mA
• SINK CURRENT	9mA
• PROPAGATION DELAY	50nsec MAX.

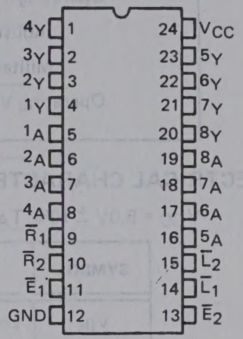
Description

The HD-6434 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 8 non-inverting latching drivers with separate input and output. A low on both strobe lines ($\overline{L}$) allows data to go through the latches and a transition to high latches the data. A high on either Three State control ($\overline{E}$) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line ($\overline{R}$) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

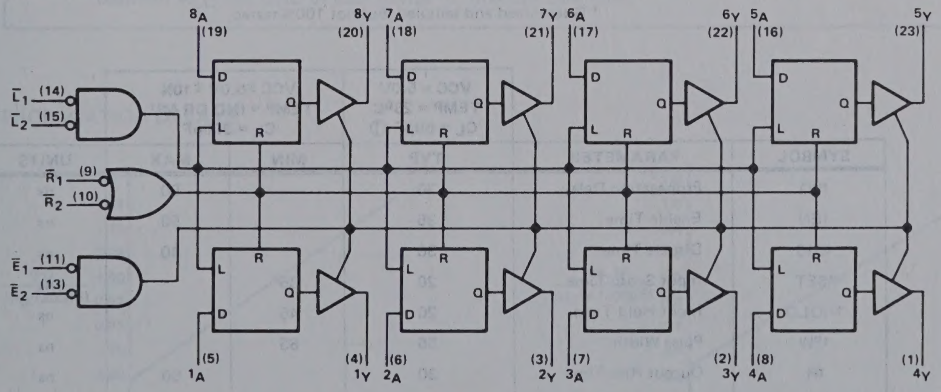

4Y 1
3Y 2
2Y 3
1Y 4
1A 5
2A 6
3A 7
4A 8
R̄1 9
R̄2 10
Ē1 11
GND 12
24 VCC
23 5Y
22 6Y
21 7Y
20 8Y
19 8A
18 7A
17 6A
16 5A
15 L̄2
14 L̄1
13 Ē2

Truth Table

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	Hi-Z
X	X	X	H	X	X	X	Hi-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care Hi-Z = High Impedance L = Low
H = High * = Data is latched to the value of the last input
↑ = Transition from a Low to High level

Functional Diagram


8A (19)
8Y (20)
7A (18)
7Y (21)
6A (17)
6Y (22)
5A (16)
5Y (23)
L̄1 (14)
L̄2 (15)
R̄1 (9)
R̄2 (10)
Ē1 (11)
Ē2 (13)
D
Q
L
R
(5) 1A
(4) 1Y
(6) 2A
(3) 2Y
(7) 3A
(2) 3Y
(8) 4A
(1) 4Y

Specifications HD-6434

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6434-9	-40°C to +85°C
Military HD-6434-2	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

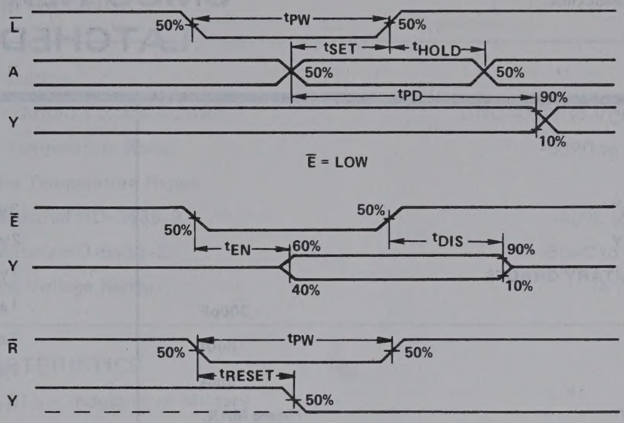
* Guaranteed and sampled, but not 100% tested.

A.C.

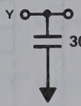
		VCC = 5.0V TEMP = 25°C C_L = 50pF ①	VCC ±5.0V ±10% TEMP = IND OR MIL C_L = 300pF		
SYMBOL	PARAMETER	TYP	MIN	MAX	UNITS
tPD	Propagation Delay	30		50	ns
tEN	Enable Time	35		50	ns
tDIS	Disable Time	30		40	ns
tSET	Input Setup Time	20	35		ns
tHOLD	Input Hold Time	20	45		ns
tPW	Pulse Width	55	65		ns
tR	Output Rise Time	30		50	ns
tF	Output Fall Time	25		50	ns
tRESET	Reset Delay Time	45		65	ns

① All devices guaranteed at worst case limits. Room temperature, 5V, C_L = 50pF data provided for information only - not guaranteed.

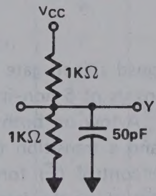
Switching Waveforms


L̄
50%
tPW
50%
tSET
tHOLD
A
50%
50%
tPD
90%
Y
10%
Ē = LOW
Ē
50%
50%
tEN
60%
tDIS
90%
Y
40%
10%
R̄
50%
tPW
50%
tRESET
Y
50%

All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS


VCC
1KΩ
Y
1KΩ
50pF

OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

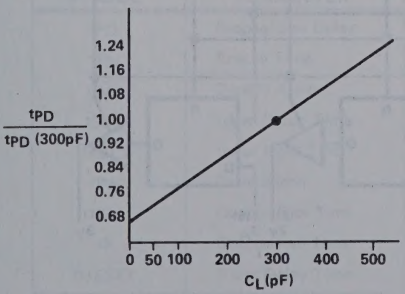


FIGURE 1

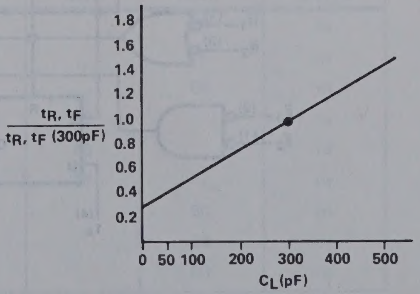


FIGURE 2

TYPICAL CURVES

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6435

CMOS HEX RESETTABLE LATCHED BUS DRIVER

Features

• SINGLE POWER SUPPLY	
• HIGH NOISE IMMUNITY	
• INDUSTRIAL AND MILITARY GRADES	
• DRIVE CAPACITY	300pF
• SOURCE CURRENT	6mA
• SINK CURRENT	9mA
• PROPAGATION DELAY	70nsec MAX.

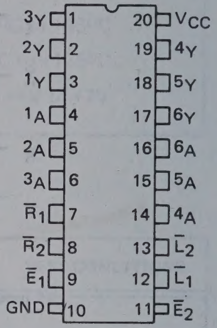
Description

The HD-6435 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A low on both strobe lines ($\overline{L}$) allows data to go through the latches and a transition to high latches the data. A high on either Three State control ($\overline{E}$) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line ($\overline{R}$) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



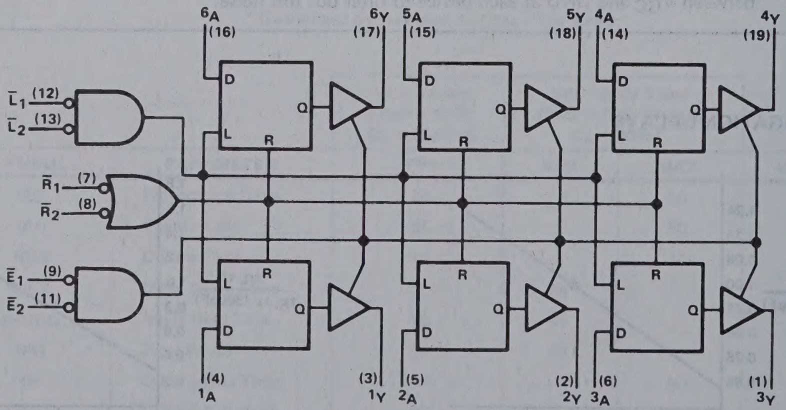
3_Y 1
2_Y 2
1_Y 3
1_A 4
2_A 5
3_A 6
$\overline{R}_1$ 7
$\overline{R}_2$ 8
$\overline{E}_1$ 9
GND 10
20 V_{CC}
19 4_Y
18 5_Y
17 6_Y
16 6_A
15 5_A
14 4_A
13 $\overline{L}_2$
12 $\overline{L}_1$
11 $\overline{E}_2$

Truth Table

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	Hi-Z
X	X	X	H	X	X	X	Hi-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care Hi-Z = High Impedance L = Low
H = High * = Data is latched to the value of the last input
↑ = Transition from a Low to High level

Functional Diagram



6_A (16)
6_Y (17)
5_A (15)
5_Y (18)
4_A (14)
4_Y (19)
$\overline{L}_1$ (12)
$\overline{L}_2$ (13)
$\overline{R}_1$ (7)
$\overline{R}_2$ (8)
$\overline{E}_1$ (9)
$\overline{E}_2$ (11)
D
Q
L
R
(4) 1_A
(3) 1_Y
(5) 2_A
(2) 2_Y
(6) 3_A
(1) 3_Y

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HD-6435

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6435-9	-40°C to +85°C
Military HD-6435-2	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

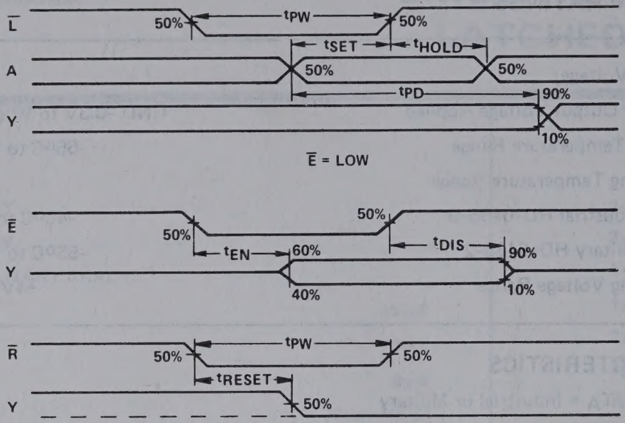
* Guaranteed and sampled, but not 100% tested.

A.C.

		VCC = 5.0V TEMP = 25°C C_L = 50pF ①	VCC ±5.0V ±10% TEMP = IND OR MIL C_L = 300pF		
SYMBOL	PARAMETER	TYP	MIN	MAX	UNITS
tPD	Propagation Delay	30		70	ns
tEN	Enable Time	35		75	ns
tDIS	Disable Time	30		55	ns
tSET	Input Setup Time	20	35		ns
tHOLD	Input Hold Time	20	45		ns
tPW	Pulse Width	50	60		ns
tR	Output Rise Time	30		50	ns
tF	Output Fall Time	25		50	ns
tRESET	Reset Delay Time	40		50	ns

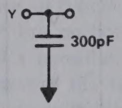
① All devices guaranteed at worst case limits. Room temperature, 5V, C_L = 50pF data provided for information only - not guaranteed.

Switching Waveforms

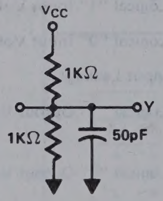


$\overline{L}$
50%
tPW
50%
tSET
tHOLD
A
50%
50%
tPD
90%
Y
10%
$\overline{E}$ = LOW
$\overline{E}$
50%
50%
tEN
60%
tDIS
90%
Y
40%
10%
$\overline{R}$
50%
tPW
50%
tRESET
Y
50%

All inputs have t_R, $t_F \leq 20ns$.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS



V_{CC}
1KΩ
Y
1KΩ
50pF

OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1µF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

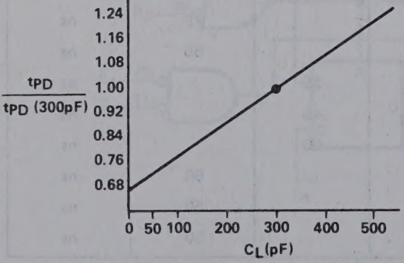


FIGURE 1

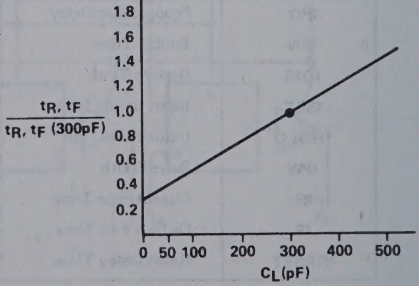


FIGURE 2

TYPICAL CURVES

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6436

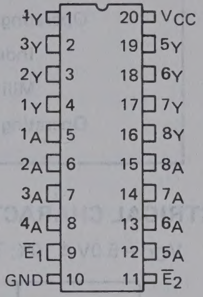
CMOS OCTAL BUS BUFFER/DRIVER

Features

SINGLE POWER SUPPLY	
HIGH NOISE IMMUNITY	
INDUSTRIAL AND MILITARY GRADES	
DRIVE CAPACITY	300pF
SOURCE CURRENT	6mA
SINK CURRENT	9mA
PROPAGATION DELAY	55nsec MAX.

Pinout

TOP VIEW


4_Y 1
3_Y 2
2_Y 3
1_Y 4
1_A 5
2_A 6
3_A 7
4_A 8
$\overline{E}_1$ 9
GND 10
20 V_{CC}
19 5_Y
18 6_Y
17 7_Y
16 8_Y
15 8_A
14 7_A
13 6_A
12 5_A
11 $\overline{E}_2$

Description

The HD-6436 is a self-aligned silicon gate CMOS Three State buffer driver. The circuit consists of 8 noninverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

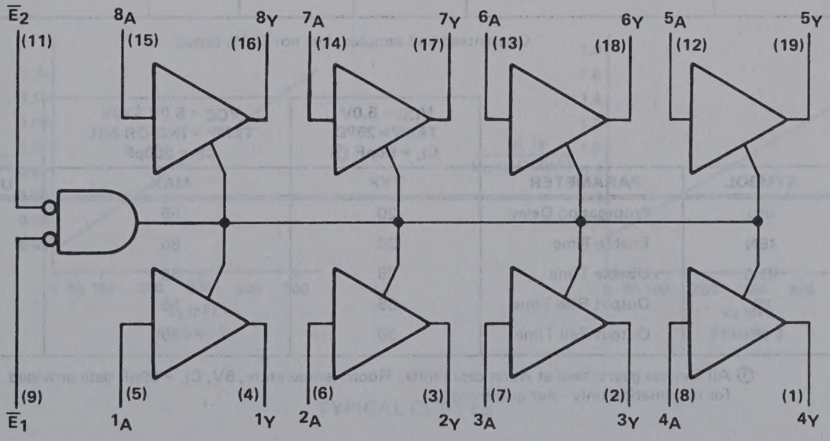
Outputs guaranteed valid at V_{CC} = 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	Hi-Z
H	L	X	Hi-Z
H	H	X	Hi-Z

L = Low, H = High
X = Don't Care
Hi-Z = High Impedance

Functional Diagram


$\overline{E}_2$
(11)
8_A
(15)
(16)
8_Y
7_A
(14)
(17)
7_Y
6_A
(13)
(18)
6_Y
5_A
(12)
(19)
5_Y
(9)
$\overline{E}_1$
(5)
1_A
(4)
1_Y
(6)
2_A
(3)
2_Y
(7)
3_A
(2)
3_Y
(8)
4_A
(1)
4_Y

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6436-9	-40°C to +85°C
Military HD-6436-2	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -6.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 9.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

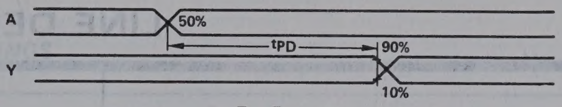
* Guaranteed and sampled, but not 100% tested.

A.C.

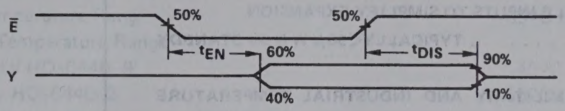
		V_{CC} = 5.0V TEMP = 25°C C_L = 50pF ①	V_{CC} = 5.0V ±10% TEMP = IND OR MIL C_L = 300pF	
SYMBOL	**PARAMETER**	**TYP**	**MAX**	**UNITS**
t_{PD}	Propagation Delay	20	55	ns
t_{EN}	Enable Time	30	65	ns
t_{DIS}	Disable Time	25	55	ns
t_R	Output Rise Time	35	55	ns
t_F	Output Fall Time	30	55	ns

① All Devices guaranteed at worst case limits. Room temperature, 5V, C_L = 50pF data provided for information only - not guaranteed.

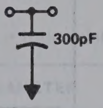
Switching Waveforms



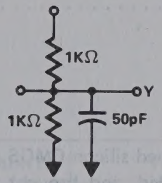
$\bar{E}_1 = \bar{E}_2 =$ LOW



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS



OUTPUT TEST CIRCUIT FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS

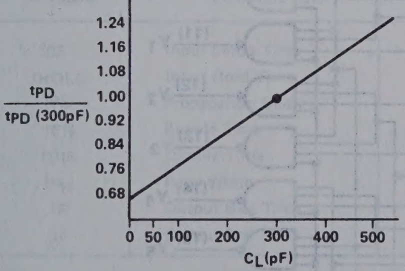


FIGURE 1

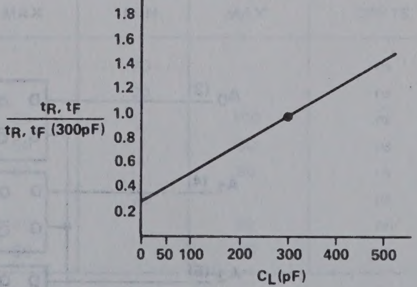


FIGURE 2

TYPICAL CURVES

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6440

CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER

Features

- HIGH SPEED DECODING FOR MEMORY ARRAYS
- INCORPORATES 3 ENABLE INPUTS TO SIMPLIFY EXPANSION
- LOW POWER . . . . TYPICALLY<50μW @ 5V STANBDY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE 200pF
- HIGH OUTPUT DRIVE . . . . I_{OH} = -2mA, I_{OL} = 2.4mA
- SINGLE POWER SUPPLY

Description

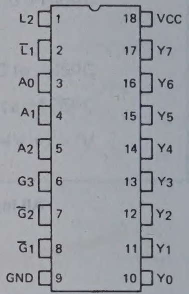
The HD-6440 is a self aligned silicon CMOS gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables (L_1, L_2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables (G_1, G_2, G_3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW


L2 1
$\overline{L}$1 2
A0 3
A1 4
A2 5
G3 6
$\overline{G}$2 7
$\overline{G}$1 8
GND 9
18 VCC
17 Y7
16 Y6
15 Y5
14 Y4
13 Y3
12 Y2
11 Y1
10 Y0

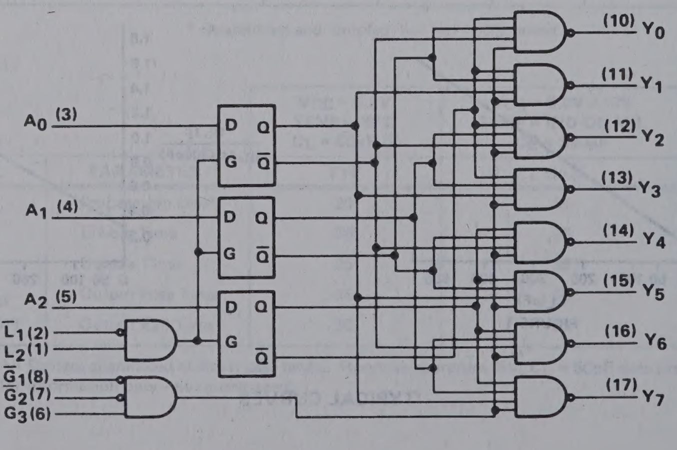
Truth Table

INPUTS								OUTPUTS								
ENABLE					ADDRESS											
$\overline{G}_1$	$\overline{G}_2$	G_3	$\overline{L}_1$	L_2	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
X	H	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
L	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	DECODE
L	L	H	L	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	H	L	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	X	L	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H	H	X	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	

L = Low, H = High, X = Don't Care

Y_n = Data is latched to the value of the last input

Functional Diagram


A0 (3)
A1 (4)
A2 (5)
$\overline{L}$1 (2)
L2 (1)
$\overline{G}$1 (8)
$\overline{G}$2 (7)
G3 (6)
D
Q
G
$\overline{Q}$
(10) Y0
(11) Y1
(12) Y2
(13) Y3
(14) Y4
(15) Y5
(16) Y6
(17) Y7

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HD-6440

BSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440-9	-40°C to +85°C
Military HD-6440-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

LECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -2.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 2.4mA
I_{CC}	Supply Current		10	μA	V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

*Guaranteed and sampled, but not 100% tested.

A.C.

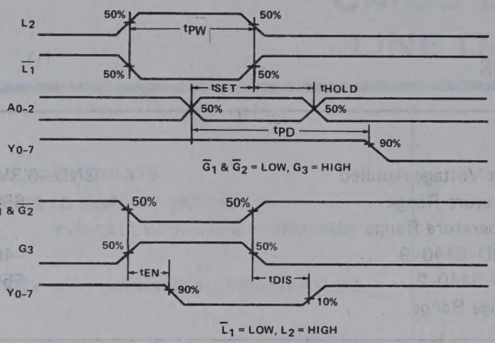
C_L = 200pF

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	20		20		ns
t_{HOLD}	Input Hold Time	20		20		ns
t_{PD}	Propagation Delay		65		100	ns
t_{EN}	Enable Time		50		90	ns
t_{DIS}	Disable Time		50		90	ns
t_{PW}	Pulse Width	30		30		ns
t_R	Output Rise Time		60		90	ns
t_F	Output Fall Time		50		80	ns

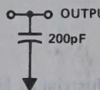
NOTE:

① All devices guaranteed at worse case limits. Room temperature, 5V data provided for information – not guaranteed.

Switching Waveforms


L2
$\overline{L_1}$
A0-2
Y0-7
50%
tPW
tSET
tHOLD
tPD
90%
$\overline{G}_1$ & $\overline{G}_2$ = LOW, G_3 = HIGH
$\overline{G_1}$ & $\overline{G_2}$
G3
Y0-7
tEN
tDIS
90%
10%
$\overline{L}_1$ = LOW, L_2 = HIGH

All Inputs have t_R, $t_F \leq$ 20ns

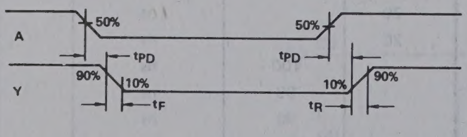


OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\Big[t_R = 60\text{ns}, V_{CC} = 5.0\text{V}$, each $C_L = 200\text{pF}, I_T = (2)\,(200 \times 10^{-12})\ \frac{5.0 \times 0.8}{60 \times 10^{-9}} = 26.7\text{mA}. \Big]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAY



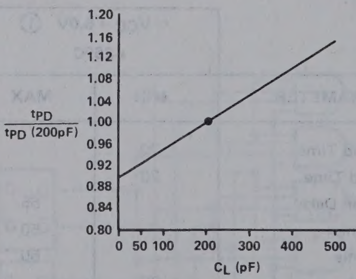


FIGURE 1

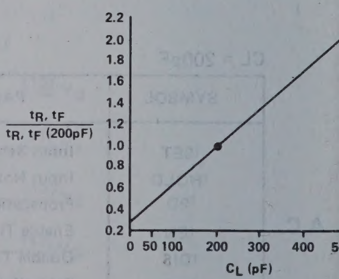


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6440-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 100nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.97. The adjusted propagation delay, to the 10% or 90% point, is therefore 100 x 0.97 or 97nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.85. The adjusted rise time is, therefore, 90 x 0.85 or 76.5nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 135nsec. The rise time was used here because it is always the worst case.

Battery Backup Applications

The **HD-6440** is especially well suited for use in battery backup systems in conjunction with low power CMOS RAM arrays. When designing a RAM array in conjunction with the **HD-6440**, the following criteria should be met:

1. As RAM VCC drops, the inputs logical one voltages should follow so as not to exceed VCC +0.3V and logical zero voltages do not go below GND -0.3V.

2. $\overline{G}_1$ or $\overline{G}_2$ must be held high at CMOS VCC, or G_3 held low. $\overline{L}_1$, L_2 and address inputs should be held at either GND or CMOS VCC.

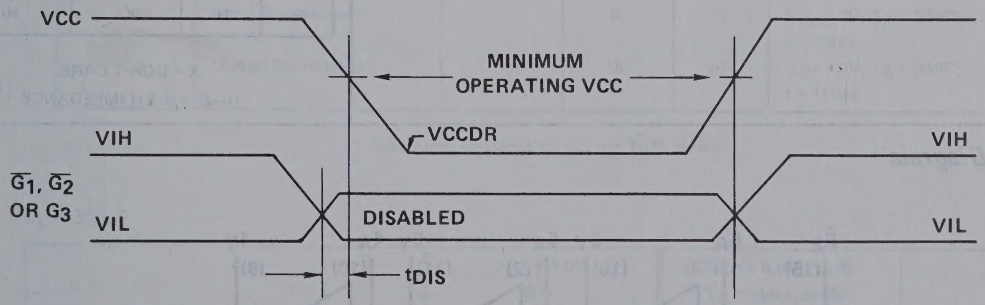
3. Y_0 - Y_7 will maintain a VOH of VCC -0.3 or greater at IOH of 100 μA provided the **HD-6440** VCC is $\geq$2.0V.

4. When exiting from the battery backup mode, VCC should ramp without ring on discontinuities.

5. The **HD-6440** can begin operation when VCC reaches the minimum operating voltage.

6. The **HD-6440** should be disabled one t_{DIS} before VCC reaches the minimum operating voltage.

TIMING DIAGRAM



HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6495
CMOS HEX BUS DRIVER

Features

• SINGLE POWER SUPPLY	
• HIGH NOISE IMMUNITY	
• INDUSTRIAL AND MILITARY GRADES	
• DRIVE CAPACITY	300pF
• SOURCE CURRENT	4mA
• SINK CURRENT	6mA
• PROPAGATION DELAY	45nsec MAX.

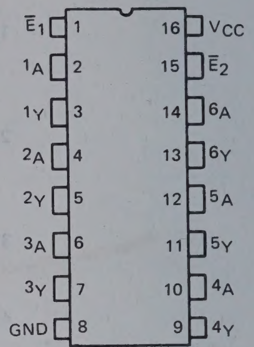
Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



Ē1 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 Ē2
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y

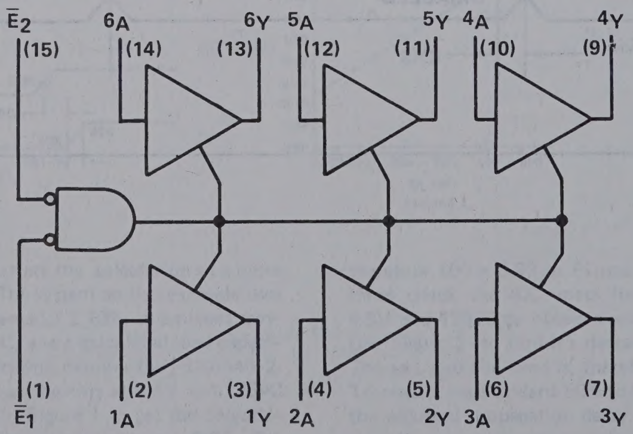
Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = DON'T CARE

HI-Z = HIGH IMPEDANCE

Functional Diagram



Ē2 (15)
6A (14)
6Y (13)
5A (12)
5Y (11)
4A (10)
4Y (9)
Ē1 (1)
1A (2)
1Y (3)
2A (4)
2Y (5)
3A (6)
3Y (7)

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495-9	-40°C to +85°C
Military HD-6495-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

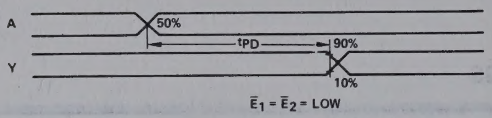
C_L = 300pF

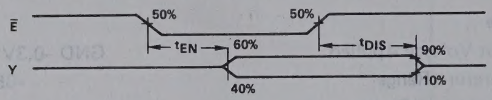
.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		20		45	ns
t_{EN}	Enable Time		50		100	ns
t_{DIS}	Disable Time		50		100	ns
t_R	Output Rise Time		50		95	ns
t_F	Output Fall Time		45		75	ns

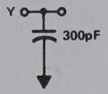
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

Switching Waveforms

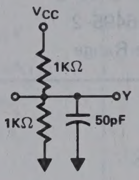




All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

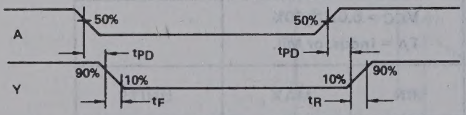


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85\text{ns}, V_{CC} = 5.0\text{V}, \text{ each } C_L = 300\text{pF}, I_T = (6)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 84.7\text{mA}.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



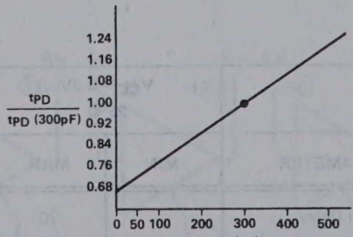


FIGURE 1

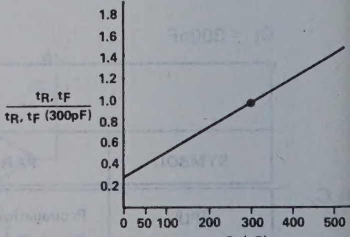


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of ± 10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6495-2. The table of A.C. specs shows the t_{PD} at 4.5V and 125°C is 45nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 45 x 0.84 or 38nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 69nsec. The rise time was used here because it is always the worst case.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

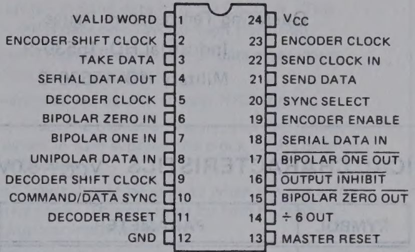
HD-15530

CMOS Manchester Encoder-Decoder

Features

- SUPPORT OF MIL-STD-1553
- 1.25 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE

Pinout


VALID WORD 1
ENCODER SHIFT CLOCK 2
TAKE DATA 3
SERIAL DATA OUT 4
DECODER CLOCK 5
BIPOLAR ZERO IN 6
BIPOLAR ONE IN 7
UNIPOLAR DATA IN 8
DECODER SHIFT CLOCK 9
COMMAND/DATA SYNC 10
DECODER RESET 11
GND 12
24 VCC
23 ENCODER CLOCK
22 SEND CLOCK IN
21 SEND DATA
20 SYNC SELECT
19 ENCODER ENABLE
18 SERIAL DATA IN
17 BIPOLAR ONE OUT
16 OUTPUT INHIBIT
15 BIPOLAR ZERO OUT
14 ÷ 6 OUT
13 MASTER RESET

Description

The Harris HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset function.

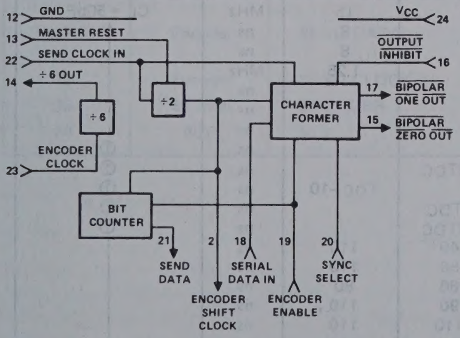
This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

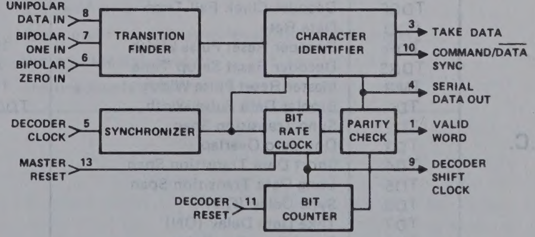
The HD-15530 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable or fiber optic cable throughout the building.

Block Diagrams

ENCODER


12 GND
13 MASTER RESET
22 SEND CLOCK IN
14 ÷ 6 OUT
÷ 6
÷ 2
ENCODER CLOCK
23
BIT COUNTER
CHARACTER FORMER
VCC 24
OUTPUT INHIBIT 16
17 BIPOLAR ONE OUT
15 BIPOLAR ZERO OUT
21 SEND DATA
2 ENCODER SHIFT CLOCK
18 SERIAL DATA IN
19 ENCODER ENABLE
20 SYNC SELECT

DECODER


UNIPOLAR DATA IN 8
BIPOLAR ONE IN 7
BIPOLAR ZERO IN 6
TRANSITION FINDER
CHARACTER IDENTIFIER
3 TAKE DATA
10 COMMAND/DATA SYNC
4 SERIAL DATA OUT
DECODER CLOCK 5
SYNCHRONIZER
BIT RATE CLOCK
PARITY CHECK
1 VALID WORD
MASTER RESET 13
9 DECODER SHIFT CLOCK
DECODER RESET 11
BIT COUNTER

CAUTION: These devices are sensitive to electrostatic discharge.
Users should follow IC Handling Procedures specified on pg. 1-6.

Specifications HD-15530

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-15530-9	-40°C to +85°C
Military HD-15530-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
I_{IL}	Input Leakage	-1.0		+1.0	µA	0V ⩽ V_{IN} ⩽ V_{CC}
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
I_{CCSB}	Supply Current Standby		0.5	2	mA	V_{IN} = V_{CC} = 5.25V Outputs Open
I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.25V, f = 1MHz
C_{IN}	Input Capacitance*		5.0	7.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed and sampled but not 100% tested.

ENCODER TIMING V_{CC} = 5.0V ±5% T_A = Industrial or Military

A.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
F_{EC}	Encoder Clock Frequency			15	MHz	C_L = 50pF
F_{ESC}	Send Clock Frequency			2.5	MHz	
T_{ECR}	Encoder Clock Rise Time			8	ns	
T_{ECF}	Encoder Clock Fall Time			8	ns	
F_{ED}	Data Rate			1.25	MHz	
T_{MR}	Master Reset Pulse Width	150			ns	
T_{E1}	Shift Clock Delay			125	ns	
T_{E2}	Serial Data Setup	75			ns	
T_{E3}	Serial Data Hold	75			ns	
T_{E4}	Enable Setup	90			ns	
T_{E5}	Enable Pulse Width	80			ns	
T_{E6}	Sync Setup	55			ns	
T_{E7}	Sync Pulse Width	150			ns	
T_{E8}	Send Data Delay			50	ns	
T_{E9}	Bipolar Output Delay			130	ns	

DECODER TIMING V_{CC} = 5.0V ±5% T_A = Industrial or Military

A.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
F_{DC}	Decoder Clock Frequency			15	MHz	C_L = 50pF
T_{DCR}	Decoder Clock Rise Time			8	ns	
T_{DCF}	Decoder Clock Fall Time			8	ns	
F_{DD}	Data Rate			1.25	MHz	
T_{DR}	Decoder Reset Pulse Width	150			ns	
T_{DRS}	Decoder Reset Setup Time	75			ns	
T_{MR}	Master Reset Pulse Width	150			ns	
T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	①
T_{D2}	Sync Transition Span		18T_{DC}		ns	①
T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
T_{D4}	Short Data Transition Span		6T_{DC}		ns	①
T_{D5}	Long Data Transition Span		12T_{DC}		ns	①
T_{D6}	Sync Delay (ON)		40	110	ns	
T_{D7}	Take Data Delay (ON)		50	110	ns	
T_{D8}	Serial Data Out Delay		80	80	ns	
T_{D9}	Sync Delay (OFF)		90	110	ns	
T_{D10}	Take Data Delay (OFF)		110	110	ns	
T_{D11}	Valid Word Delay		90	110	ns	

NOTE ①: 15T_{DC} +10 = [15 (Decoder Clock Period)] +10ns T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

Pin Assignments

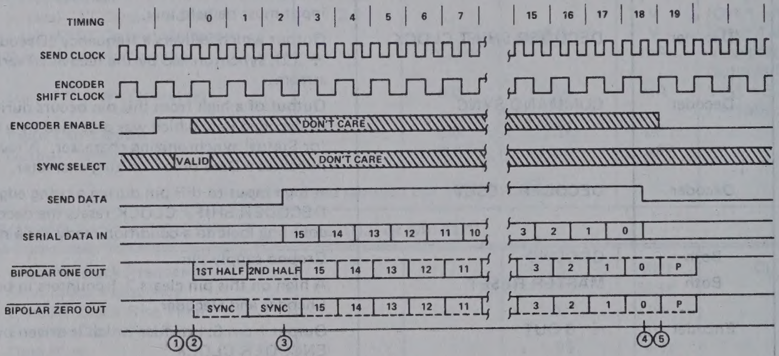
PIN	SECTION	NAME	DESCRIPTION
1	Decoder	VALID WORD	Output high indicates receipt of a valid word.
2	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	Decoder	TAKE DATA	Output is high during receipt of data after identification fo a sync pulse.
4	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
5	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	Decoder	UNIPOLAR DATA IN	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (Decoder Clock ÷ 12), synchronized by the recovered serial data stream.
10	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	Both	GROUND	Ground supply pin.
13	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the Encoder and Decoder.
14	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	Encoder	$\overline{\text{BIPOLAR}}\ \overline{\text{ZERO}}\ \overline{\text{OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	Encoder	$\overline{\text{OUTPUT}}\ \overline{\text{INHIBIT}}$	A low on this input forces pin 15 and pin 17 high, the inactive states.
17	Encoder	$\overline{\text{BIPOLAR}}\ \overline{\text{ONE}}\ \overline{\text{OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	Encoder	ENCODER ENABLE	A high on this input initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	Encoder	SYNC SELECT	Actuates command sync for an input high and data sync for an input low.
21	Encoder	SEND DATA	Is an active high output which enables the external source of serial data.
22	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
23	Encoder	ENCODER	Input to the 6:1 divider.
24	Both	V_{CC}	Positive supply pin.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxillary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word ② . When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③ . During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ – ④ . After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR}}$ $\overline{\text{ONE}}$ and $\overline{\text{BIPOLAR}}$ $\overline{\text{ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. At any time a low on $\overline{\text{OUTPUT}}$ $\overline{\text{INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



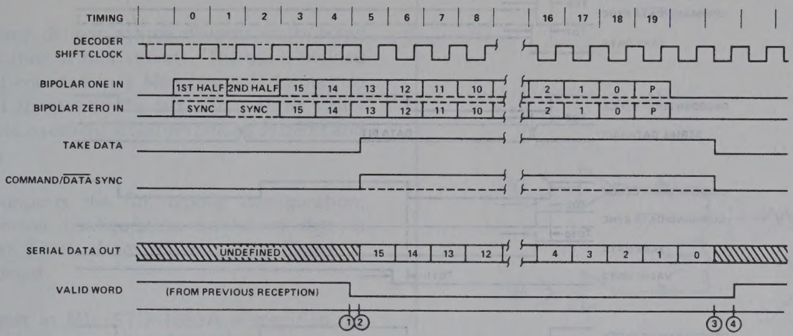
Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR}}$ $\overline{\text{ZERO}}$ $\overline{\text{OUT}}$ of an Encoder.)

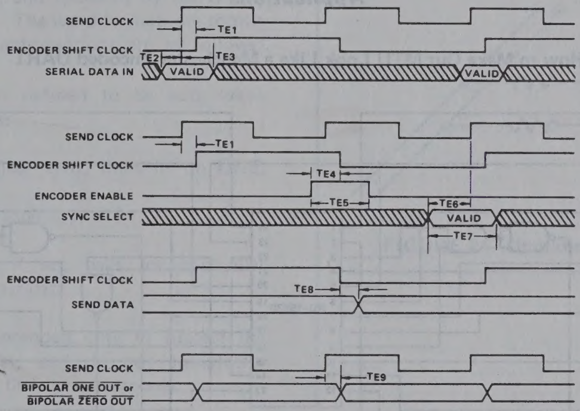
The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③ , otherwise it will remain low. The TAKE DATA output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② – ③.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

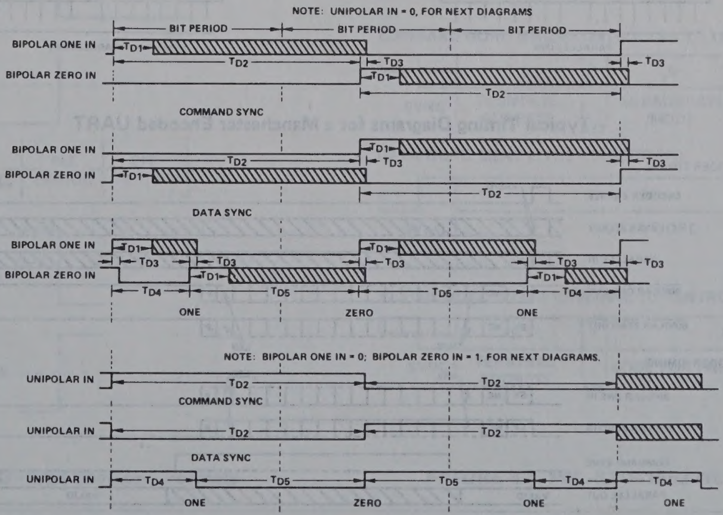
At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

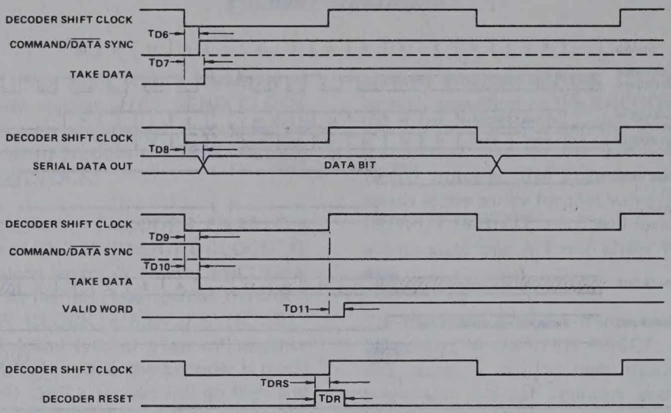

TIMING
0
1
2
3
4
5
6
7
8
16
17
18
19
DECODER SHIFT CLOCK
BIPOLAR ONE IN
1ST HALF
2ND HALF
15
14
13
12
11
10
2
1
0
P
BIPOLAR ZERO IN
SYNC
SYNC
TAKE DATA
COMMAND/$\overline{\text{DATA}}$ SYNC
SERIAL DATA OUT
UNDEFINED
4
3
VALID WORD
(FROM PREVIOUS RECEPTION)
①②
③④

Encoder Timing


SEND CLOCK
ENCODER SHIFT CLOCK
SERIAL DATA IN
TE1
TE2
TE3
VALID
VALID
SEND CLOCK
ENCODER SHIFT CLOCK
ENCODER ENABLE
SYNC SELECT
TE1
TE4
TE5
TE6
TE7
VALID
ENCODER SHIFT CLOCK
SEND DATA
TE8
SEND CLOCK
$\overline{\text{BIPOLAR ONE OUT}}$ or
$\overline{\text{BIPOLAR ZERO OUT}}$
TE9

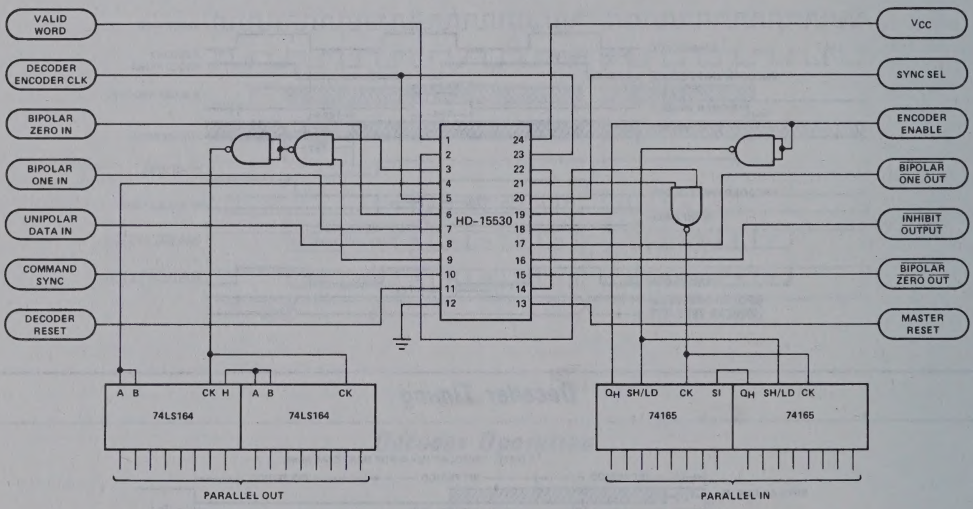
Decoder Timing


NOTE: UNIPOLAR IN = 0, FOR NEXT DIAGRAMS
BIT PERIOD
BIT PERIOD
BIT PERIOD
BIPOLAR ONE IN
BIPOLAR ZERO IN
TD1
TD2
TD3
COMMAND SYNC
BIPOLAR ONE IN
BIPOLAR ZERO IN
DATA SYNC
BIPOLAR ONE IN
BIPOLAR ZERO IN
TD4
TD5
ONE
ZERO
ONE
NOTE: BIPOLAR ONE IN = 0; BIPOLAR ZERO IN = 1, FOR NEXT DIAGRAMS.
UNIPOLAR IN
COMMAND SYNC
UNIPOLAR IN
DATA SYNC
UNIPOLAR IN
ONE
ZERO
ONE
ONE

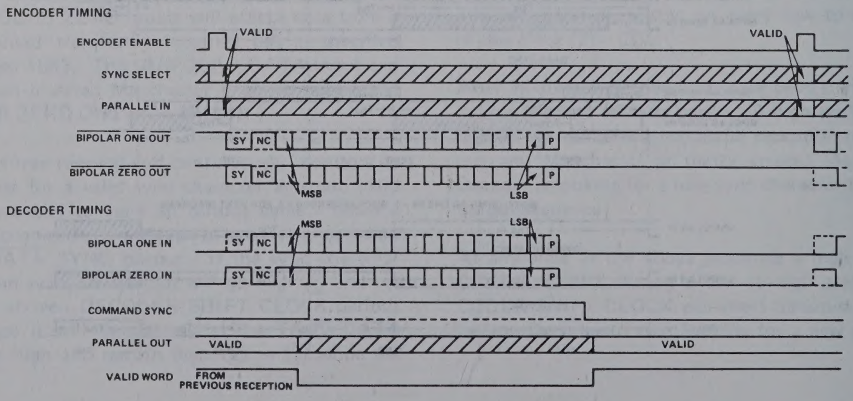

DECODER SHIFT CLOCK
COMMAND/DATA SYNC
TD6
TD7
TAKE DATA
DECODER SHIFT CLOCK
TD8
SERIAL DATA OUT
DATA BIT
DECODER SHIFT CLOCK
TD9
COMMAND/DATA SYNC
TD10
TAKE DATA
VALID WORD
TD11
DECODER SHIFT CLOCK
TDRS
DECODER RESET
TDR

Applications

How to Make Our MTU Look Like a Manchester Encoded UART


VALID WORD
DECODER ENCODER CLK
BIPOLAR ZERO IN
BIPOLAR ONE IN
UNIPOLAR DATA IN
COMMAND SYNC
DECODER RESET
VCC
SYNC SEL
ENCODER ENABLE
BIPOLAR ONE OUT
INHIBIT OUTPUT
BIPOLAR ZERO OUT
MASTER RESET
HD-15530
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
A B CK H
74LS164
A B CK
74LS164
QH SH/LD CK SI
74165
QH SH/LD CK
74165
PARALLEL OUT
PARALLEL IN

Typical Timing Diagrams for a Manchester Encoded UART


ENCODER TIMING
ENCODER ENABLE
VALID
VALID
SYNC SELECT
PARALLEL IN
BIPOLAR ONE OUT
BIPOLAR ZERO OUT
SY
NC
P
MSB
LSB
DECODER TIMING
MSB
LSB
BIPOLAR ONE IN
BIPOLAR ZERO IN
COMMAND SYNC
PARALLEL OUT
VALID
VALID
VALID WORD
FROM PREVIOUS RECEPTION

MIL-STD-1553A

The 1553A standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15530 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553A is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. These control words reference Data Words. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20μsec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P	Parity, which is defined to be odd, taken across all 17 bits.
R/T	Receive on logical zero, transmit on ONE.
ME	Message Error if logical 1.
TF	Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553A, and do not completely describe its bus requirements, timing or protocols.

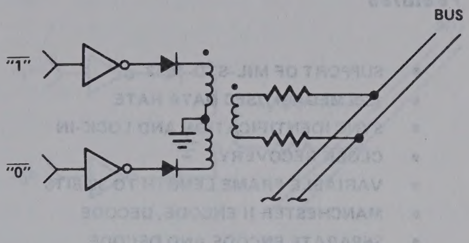


FIGURE 1 – Simplified MIL-STD-1553 Driver

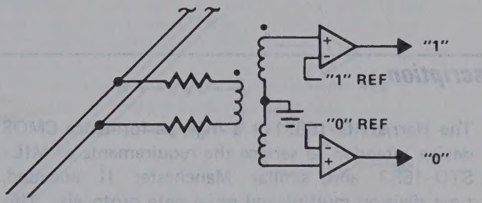

"1"
"1" REF
"0" REF
"0"

FIGURE 2 – Simplified MIL-STD-1553 Receiver

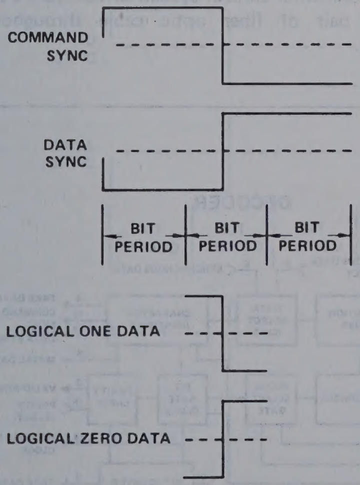

COMMAND SYNC
DATA SYNC
BIT PERIOD
BIT PERIOD
BIT PERIOD
LOGICAL ONE DATA
LOGICAL ZERO DATA

FIGURE 3 – MIL-STD-1553 Character Formats

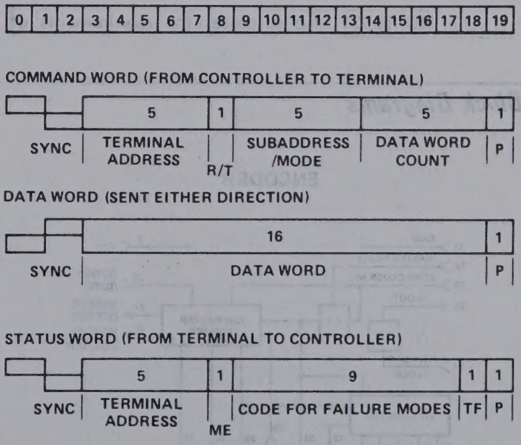

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
COMMAND WORD (FROM CONTROLLER TO TERMINAL)
5
1
5
5
1
SYNC
TERMINAL ADDRESS
R/T
SUBADDRESS /MODE
DATA WORD COUNT
P
DATA WORD (SENT EITHER DIRECTION)
16
1
SYNC
DATA WORD
P
STATUS WORD (FROM TERMINAL TO CONTROLLER)
5
1
9
1
1
SYNC
TERMINAL ADDRESS
ME
CODE FOR FAILURE MODES
TF
P

FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553A and is not intended to describe the operation of the HD-15530.

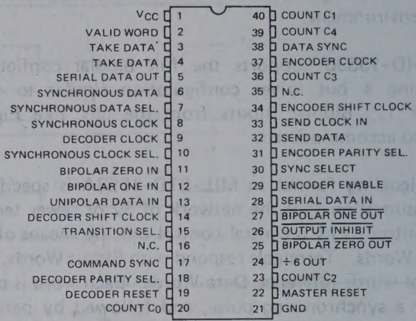
HD-15531

CMOS Manchester Encoder-Decoder

Features

- SUPPORT OF MIL-STD-1553
- 1.25 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- VARIABLE FRAME LENGTH TO 32 BITS
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW @ 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE

Pinout


VCC 1
VALID WORD 2
TAKE DATA' 3
TAKE DATA 4
SERIAL DATA OUT 5
SYNCHRONOUS DATA 6
SYNCHRONOUS DATA SEL. 7
SYNCHRONOUS CLOCK 8
DECODER CLOCK 9
SYNCHRONOUS CLOCK SEL. 10
BIPOLAR ZERO IN 11
BIPOLAR ONE IN 12
UNIPOLAR DATA IN 13
DECODER SHIFT CLOCK 14
TRANSITION SEL. 15
N.C. 16
COMMAND SYNC 17
DECODER PARITY SEL. 18
DECODER RESET 19
COUNT C0 20
21 GND
22 MASTER RESET
23 COUNT C2
24 ÷6 OUT
25 BIPOLAR ZERO OUT
26 OUTPUT INHIBIT
27 BIPOLAR ONE OUT
28 SERIAL DATA IN
29 ENCODER ENABLE
30 SYNC SELECT
31 ENCODER PARITY SEL.
32 SEND DATA
33 SEND CLOCK IN
34 ENCODER SHIFT CLOCK
35 N.C.
36 COUNT C3
37 ENCODER CLOCK
38 DATA SYNC
39 COUNT C4
40 COUNT C1

Description

The Harris HD-15531 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the Master Reset and frame length functions.

This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

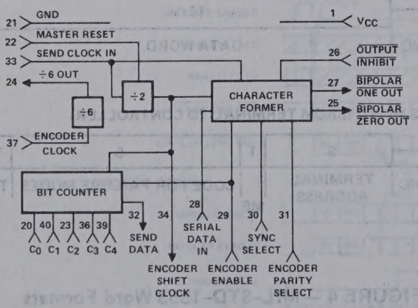
The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the frame length to be programmable. The frame length may be programmed from 2 to 28 data bits plus sync and parity. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

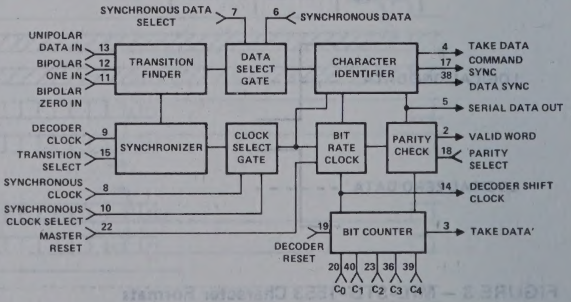
The HD-15531 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

Block Diagrams

ENCODER


21 GND
22 MASTER RESET
33 SEND CLOCK IN
24 ÷6 OUT
÷6
÷2
37 ENCODER CLOCK
1 VCC
26 OUTPUT INHIBIT
CHARACTER FORMER
27 BIPOLAR ONE OUT
25 BIPOLAR ZERO OUT
BIT COUNTER
20 40 23 36 39
C0 C1 C2 C3 C4
32 SEND DATA
34 ENCODER SHIFT CLOCK
28 SERIAL DATA IN
29 ENCODER ENABLE
30 SYNC SELECT
31 ENCODER PARITY SELECT

DECODER


SYNCHRONOUS DATA SELECT 7
6 SYNCHRONOUS DATA
UNIPOLAR DATA IN 13
BIPOLAR ONE IN 12
BIPOLAR ZERO IN 11
TRANSITION FINDER
DATA SELECT GATE
CHARACTER IDENTIFIER
4 TAKE DATA
17 COMMAND SYNC
38 DATA SYNC
5 SERIAL DATA OUT
DECODER CLOCK 9
TRANSITION SELECT 15
SYNCHRONIZER
CLOCK SELECT GATE
BIT RATE CLOCK
PARITY CHECK
2 VALID WORD
18 PARITY SELECT
SYNCHRONOUS CLOCK 8
SYNCHRONOUS CLOCK SELECT 10
MASTER RESET 22
14 DECODER SHIFT CLOCK
19 DECODER RESET
BIT COUNTER
3 TAKE DATA'
20 40 23 36 39
C0 C1 C2 C3 C4

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-6.

MIL-STD-1553A

The 1553A standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553A is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20 μ sec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P	Parity, which is defined to be odd, taken across all 17 bits.
R/T	Receive on logical zero, transmit on ONE.
ME	Message Error if logical 1.
TF	Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553A, and do not completely describe its bus requirements, timing or protocols.

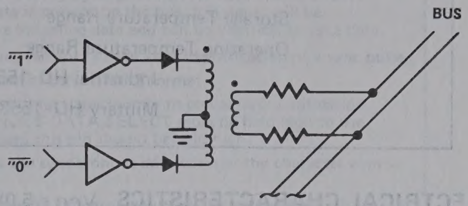


FIGURE 1 – Simplified MIL-STD-1553 Driver

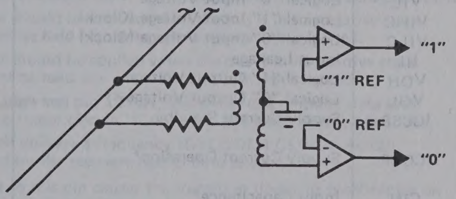

"1"
"1" REF
"0" REF
"0"

FIGURE 2 – Simplified MIL-STD-1553 Receiver

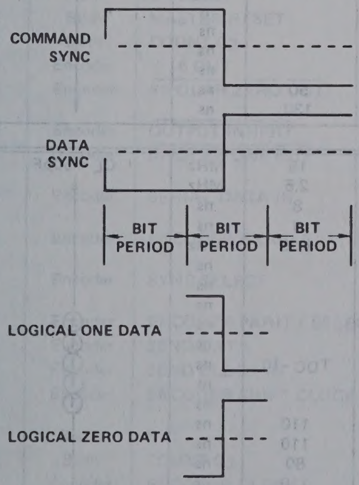

COMMAND SYNC
DATA SYNC
BIT PERIOD
BIT PERIOD
BIT PERIOD
LOGICAL ONE DATA
LOGICAL ZERO DATA

FIGURE 3 – MIL-STD-1553 Character Formats

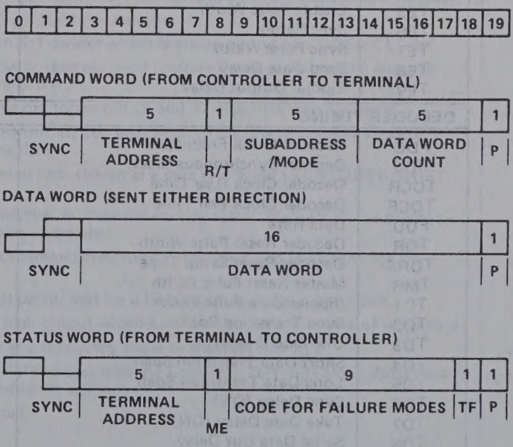

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
COMMAND WORD (FROM CONTROLLER TO TERMINAL)
5
1
5
5
1
SYNC
TERMINAL ADDRESS
R/T
SUBADDRESS /MODE
DATA WORD COUNT
P
DATA WORD (SENT EITHER DIRECTION)
16
1
SYNC
DATA WORD
P
STATUS WORD (FROM TERMINAL TO CONTROLLER)
5
1
9
1
1
SYNC
TERMINAL ADDRESS
ME
CODE FOR FAILURE MODES
TF
P

FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553A and is not intended to describe the operation of the HD-15531.

ABSOLUTE MAXUMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-15531-9	-40°C to +85°C
Military HD-15531-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_{IL}	Input Leakage	-1.0		+1.0	μA	0V ⩽ V_{IN} ⩽ V_{CC}
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2.0	mA	V_{IN} = V_{CC} = 5.25V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.25V, f = 15MHz
	C_{IN}	Input Capacitance*		5.0	7.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	
		*Guaranteed and sampled but not 100% tested.					
	ENCODER TIMING						
A.C.	FEC	Encoder Clock Frequency			15	MHz	C_L = 50pF
	FESC	Send Clock Frequency			2.5	MHz	
	TECR	Encoder Clock Rise Time			8	ns	
	TECF	Encoder Clock Fall Time			8	ns	
	FED	Data Rate			1.25	MHz	
	TMR	Master Reset Pulse Width	150			ns	
	TE1	Shift Clock Delay			125	ns	
	TE2	Serial Data Setup	75			ns	
	TE3	Serial Data Hold	75			ns	
	TE4	Enable Setup	90			ns	
	TE5	Enable Pulse Width	80			ns	
	TE6	Sync Setup	55			ns	
	TE7	Sync Pulse Width	150			ns	
	TE8	Send Data Delay			50	ns	
	TE9	Bipolar Output Delay			130	ns	
	DECODER TIMING						
A.C.	FDC	Decoder Clock Frequency			15	MHz	C_L = 50pF
	FDS	Decoder Synchronous Clock			2.5	MHz	
	TDCR	Decoder Clock Rise Time			8	ns	
	TDCF	Decoder Clock Fall Time			8	ns	
	FDD	Data Rate			1.25	MHz	
	TDR	Decoder Reset Pulse Width	150			ns	
	TDRS	Decoder Reset Setup Time	75			ns	
	TMR	Master Reset Pulse Width	150			ns	
	TD1	Bipolar Data Pulse Width	T_{DC} +10			ns	①
	TD2	Sync Transition Span		18T_{DC}		ns	①
	TD3	One Zero Overlap			T_{DC} -10	ns	①
	TD4	Short Data Transition Span		6T_{DC}		ns	①
	TD5	Long Data Transition Span		12T_{DC}		ns	①
	TD6	Sync Delay (ON)			110	ns	
	TD7	Take Data Delay (ON)			110	ns	
	TD8	Serial Data Out Delay			80	ns	
	TD9	Sync Delay (OFF)			110	ns	
	TD10	Take Data Delay (OFF)			110	ns	
	TD11	Valid Word Delay			110	ns	
	TD12	Synchronous Clock To Shift Clock Delay			75	ns	
	TD13	Synchronous Data Setup	30			ns	

NOTE ①: 15T_{DC} +10 = [15 (Decoder Clock Period)] +10ns T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

Pin Assignments

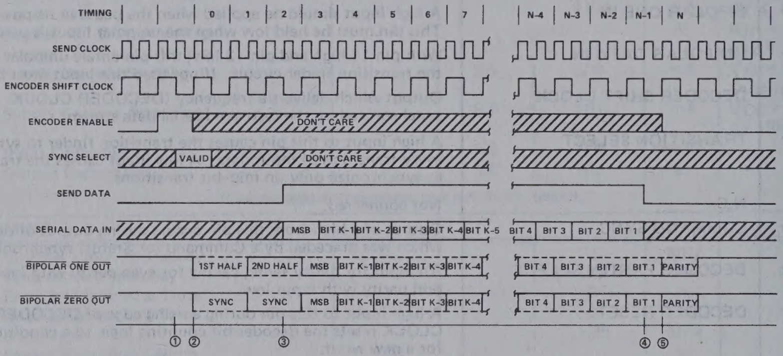
PIN	SECTION	NAME	DESCRIPTION
1	Both	VCC	Positive supply pin.
2	Decoder	VALID WORD	Output high indicates receipt of a valid word.
3	Decoder	TAKE DATA'	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	Decoder	TAKE DATA	Output is high during receipt of data after identification of a sync pulse
5	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
6	Decoder	SYNCHRONOUS DATA	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin should be held high.
7	Decoder	SYNCHRONOUS DATA SELECT	In high state allows the synchronous data to enter the character identification logic.
8	Decoder	SYNCHRONOUS CLOCK	Input provides externally synchronized clock to the decoder. This input should be tied high when not in use.
9	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder.
10	Decoder	SYNCHRONOUS CLOCK SELECT	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK
11	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	Decoder	UNIPOLAR DATA IN	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
14	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
15	Decoder	TRANSITION SELECT	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16	Blank	N.C.	Not connected.
17	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character
18	Decoder	DECODER PARITY SELECT	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	Both	COUNT C_0	One of five binary inputs which establish the total bit count to be encoded or decoded.
21	Both	GROUND	Supply pin.
22	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the encoder and decoder.
23	Both	COUNT C_2	See pin 20.
24	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	Encoder	BIPOLAR $\overline{\text{ZERO OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	Encoder	$\overline{\text{OUTPUT INHIBIT}}$	A low on this pin forces pin 25 and 27 high, the inactive states.
27	Encoder	BIPOLAR $\overline{\text{ONE OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	Encoder	ENCODER ENABLE	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
30	Encoder	SYNC SELECT	Actuates a Command sync for an input high and Data sync for an input low.
31	Encoder	ENCODER PARITY SELECT	Sets transmit parity odd for a high input, even for a low input.
32	Encoder	SEND DATA	Is an active high output which enables the external source of serial data
33	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
34	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This shift clock shifts data on a low-to-high transition.
35	Blank	N.C.	Not connected.
36	Both	COUNT C_3	See pin 20.
37	Encoder	ENCODER CLOCK	Input to the 6:1 divider.
38	Decoder	DATA SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Data synchronizing character.
39	Both	COUNT C_4	See pin 20.
40	Both	COUNT C_1	See pin 20.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a Command sync or a low will produce a Data sync for that word ②. When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④. During these K periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ - ④. After the sync and Manchester II encoded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit with is the parity for that word ⑤. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



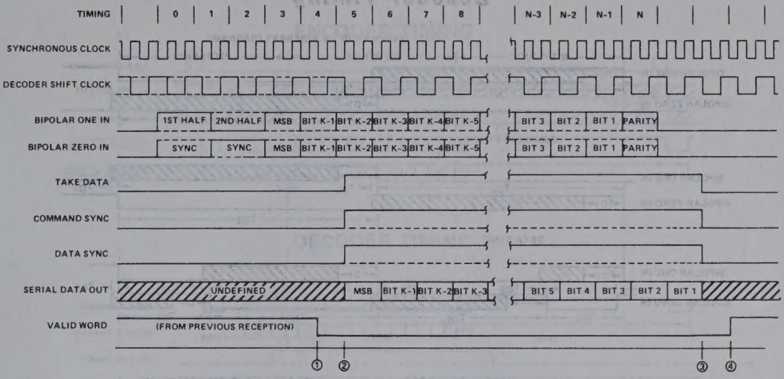
Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS DATA input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g. from BIPOLAR ZERO OUT on an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ③, where K is the number of bits to be received. If the sync character was a data sync the DATA SYNC output will go high. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③.

After all K decoded bits have been transmitted ③ the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

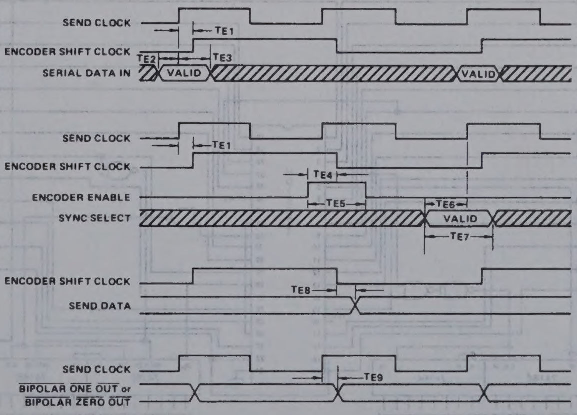

TIMING
0
1
2
3
4
5
6
7
8
N-3
N-2
N-1
N
SYNCHRONOUS CLOCK
DECODER SHIFT CLOCK
BIPOLAR ONE IN
1ST HALF
2ND HALF
MSB
BIT K-1
BIT K-2
BIT K-3
BIT K-4
BIT K-5
BIT 3
BIT 2
BIT 1
PARITY
BIPOLAR ZERO IN
SYNC
SYNC
TAKE DATA
COMMAND SYNC
DATA SYNC
SERIAL DATA OUT
UNDEFINED
BIT 5
BIT 4
VALID WORD
(FROM PREVIOUS RECEPTION)
①
②
③
④

Frame Count

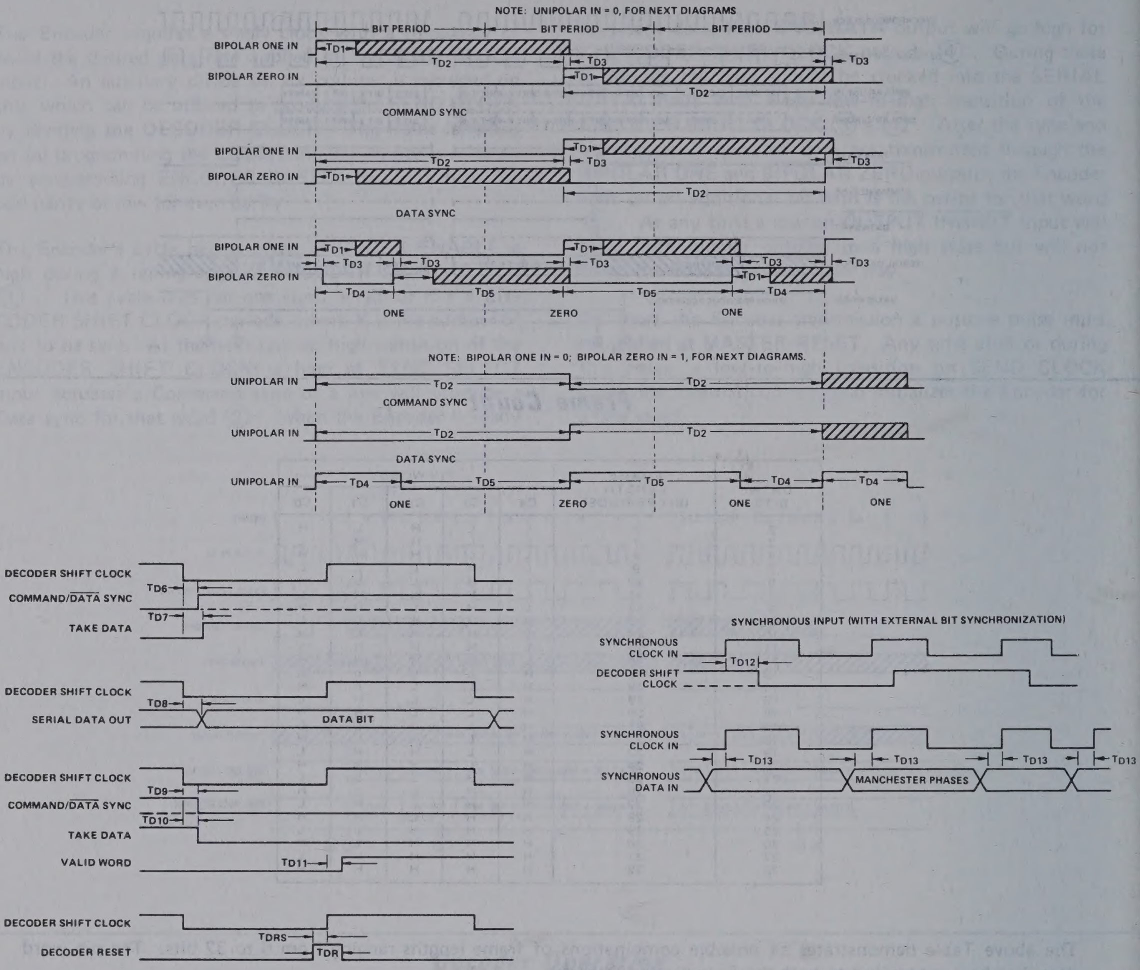
DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD				
		C4	C3	C2	C1	C0
2	6	L	L	H	L	H
3	7	L	L	H	H	L
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
11	15	L	H	H	H	L
12	16	L	H	H	H	H
13	17	H	L	L	L	L
14	18	H	L	L	L	H
15	19	H	L	L	H	L
16	20	H	L	L	H	H
17	21	H	L	H	L	L
18	22	H	L	H	L	H
19	23	H	L	H	H	L
20	24	H	L	H	H	H
21	25	H	H	L	L	L
22	26	H	H	L	L	H
23	27	H	H	L	H	L
24	28	H	H	L	H	H
25	29	H	H	H	L	L
26	30	H	H	H	L	H
27	31	H	H	H	H	L
28	32	H	H	H	H	H

The above Table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

Encoder Timing

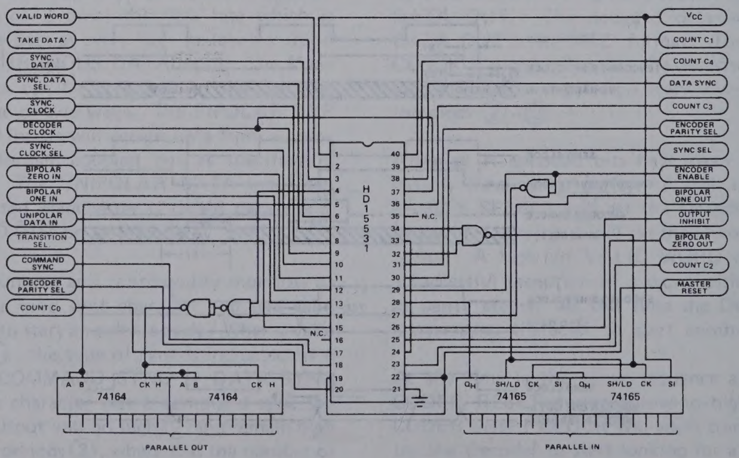

SEND CLOCK
TE1
ENCODER SHIFT CLOCK
TE2
TE3
SERIAL DATA IN
VALID
VALID
SEND CLOCK
TE1
ENCODER SHIFT CLOCK
TE4
ENCODER ENABLE
TE5
TE6
SYNC SELECT
VALID
TE7
ENCODER SHIFT CLOCK
TE8
SEND DATA
SEND CLOCK
TE9
BIPOLAR ONE OUT or
BIPOLAR ZERO OUT

Decoder Timing


NOTE: UNIPOLAR IN = 0, FOR NEXT DIAGRAMS
BIT PERIOD
BIT PERIOD
BIT PERIOD
BIPOLAR ONE IN
BIPOLAR ZERO IN
COMMAND SYNC
BIPOLAR ONE IN
BIPOLAR ZERO IN
DATA SYNC
BIPOLAR ONE IN
BIPOLAR ZERO IN
TD1
TD2
TD3
TD4
TD5
ONE
ZERO
ONE
NOTE: BIPOLAR ONE IN = 0; BIPOLAR ZERO IN = 1, FOR NEXT DIAGRAMS.
UNIPOLAR IN
COMMAND SYNC
UNIPOLAR IN
DATA SYNC
UNIPOLAR IN
ONE
ZERO
ONE
ONE
DECODER SHIFT CLOCK
COMMAND/DATA SYNC
TAKE DATA
TD6
TD7
DECODER SHIFT CLOCK
SERIAL DATA OUT
TD8
DATA BIT
DECODER SHIFT CLOCK
COMMAND/DATA SYNC
TAKE DATA
VALID WORD
TD9
TD10
TD11
DECODER SHIFT CLOCK
DECODER RESET
TDRS
TDR
SYNCHRONOUS INPUT (WITH EXTERNAL BIT SYNCHRONIZATION)
SYNCHRONOUS CLOCK IN
DECODER SHIFT CLOCK
TD12
SYNCHRONOUS CLOCK IN
SYNCHRONOUS DATA IN
TD13
MANCHESTER PHASES

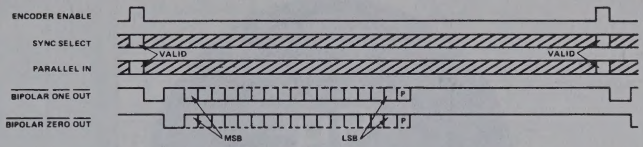
Applications

How to Make Our MTU Look Like a Manchester Encoded UART

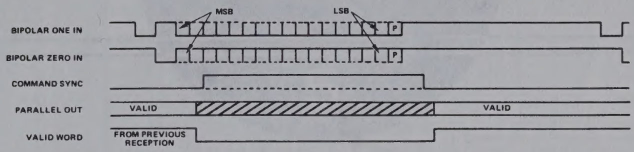

VALID WORD
TAKE DATA
SYNC. DATA
SYNC. DATA SEL.
SYNC. CLOCK
DECODER CLOCK
SYNC. CLOCK SEL
BIPOLAR ZERO IN
BIPOLAR ONE IN
UNIPOLAR DATA IN
TRANSITION SEL.
COMMAND SYNC
DECODER PARITY SEL
COUNT C0
VCC
COUNT C1
COUNT C4
DATA SYNC
COUNT C3
ENCODER PARITY SEL
SYNC SEL
ENCODER ENABLE
BIPOLAR ONE OUT
OUTPUT INHIBIT
BIPOLAR ZERO OUT
COUNT C2
MASTER RESET
HD15531
N.C.
N.C.
74164
74164
A B
CK H
74165
74165
QH
SH/LD
CK
SI
PARALLEL OUT
PARALLEL IN

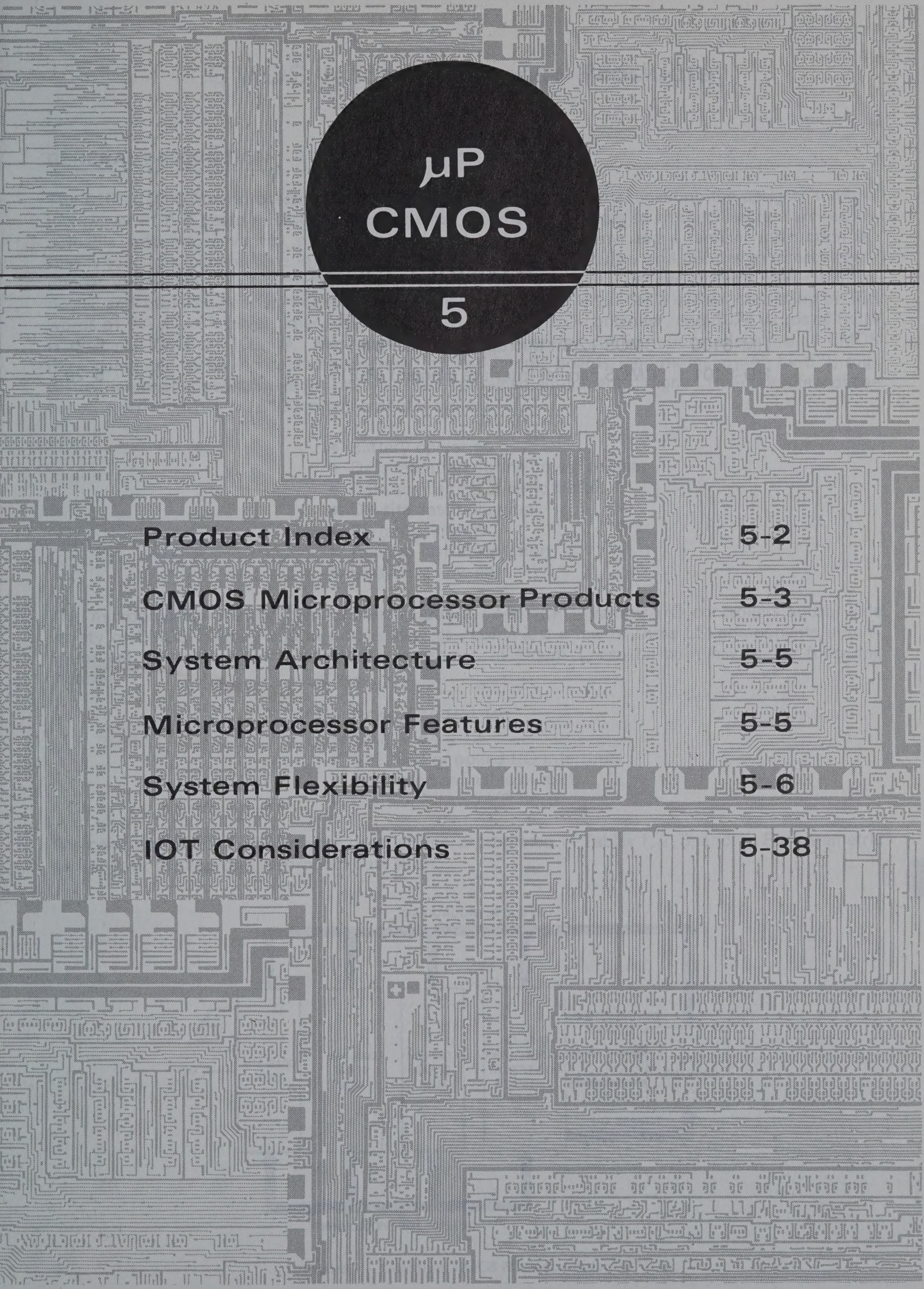
Typical Timing Diagrams for a Manchester Encoded UART

ENCODER TIMING


ENCODER ENABLE
SYNC SELECT
PARALLEL IN
BIPOLAR ONE OUT
BIPOLAR ZERO OUT
VALID
VALID
P
P
MSB
LSB

DECODER TIMING


MSB
LSB
BIPOLAR ONE IN
BIPOLAR ZERO IN
COMMAND SYNC
PARALLEL OUT
VALID WORD
P
P
VALID
VALID
FROM PREVIOUS RECEPTION



µP CMOS

5

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System Flexibility 5-6

IOT Considerations 5-38

Product Index

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HD-6101 CMOS Parallel Interface Element (PIE) 5-29

CMOS Microprocessor Products

GENERAL DESCRIPTION

The 6100 CMOS Microprocessor Family offers all CMOS components, enabling the designer to build low power PDP-8 based microcomputer systems. Obvious advantages of this architecture are readily available software, a variety of development and operating systems and a familiar instruction set that is easy to program. The low power, single voltage CMOS circuitry and LSI design of each component within the 6100 microcomputer system will result in cost effective systems that minimize power and packaging costs. For example, the operating power drain for a system consisting of 256 words of RAM, an interval timer, two latched I/O ports, an I/O controller, and 1024 words of ROM is typically less than 100mW. Minimum package, high density configurations allow this all CMOS microcomputer to be incorporated on small printed circuit boards (approximately 4″ by 5″), suggesting interesting possibilities for portable, self-contained equipment designs. Here are a few of the benefits derived from the 6100 microcomputer system.

- Battery operation
- Data retention during power outages
- Data acquisition at remote sites
- On-site data reduction
- Portable systems
- Remote instrumentation
- Small size, low cost

The microprocessor family components include a 12-bit CPU, various I/O controllers and a wide variety of CMOS memory and bus driver devices. Using just a few of these LSI components, a minimum yet very powerful microcomputer, as shown in Figure 1, can be built having the following features.

- ROM – 1024 x 12
- RAM – 64 x 12
- Vectored or polled I/O interrupts
- Four programmable outputs
- Control for two I/O ports

The complete 6100 microprocessor product line is tabulated in Tables 1, 2, 3, and 4. For parametric data consult the appropriate product data sheet.

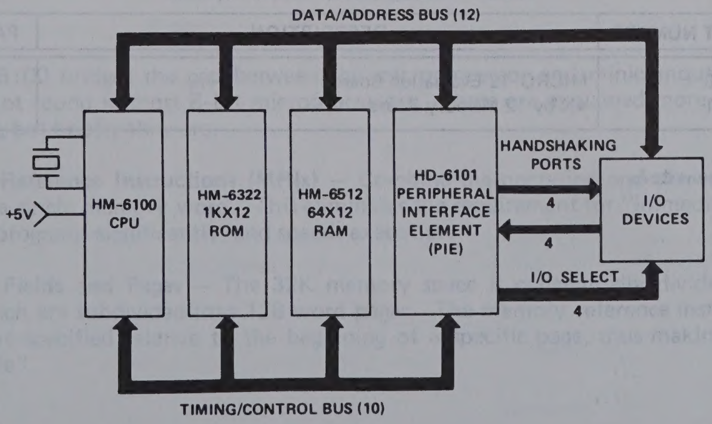


Figure 1 – Minimum CMOS Microcomputer

Table 1 – CMOS Microprocessor Products

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
CPU/Controller Group		
HM-6100	12- Bit PDP -8/E* Microprocessor (CPU)	5-7
HD-6101	Peripheral Interface Element (PIE)	5-29

Table 2 – 6100 Compatible CMOS Memory Products

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
Read Only Memory		
HM-6322	1024 x 12 ROM	3-4
HM-6661	256 x 4 PROM	3-112
Random Access Memory	RAM	
HM-6512	64 x 12	3-42
HM-6561	256 x 4	3-78
HM-6518	1024 x 1	3-66

Table 3 – CMOS Interface Products

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
Communication Group		
HD-6402	Universal Asynchronous Receiver/Transmitter (UART)	4-7
HD-4702	Programmable Bit Rate Generator (BRG)	4-3
HD-6408	Asynchronous Serial Manchester Adapter	4-12
Bus Driver Group		
HD-6431	Hex Latched Bus Driver	4-28
HD-6432	Hex Bi-Directional Bus Driver	4-31
HD-6433	Quad Bus Separator/Driver	4-34
HD-6434	Octal Resettable Latched Bus Driver	4-37
HD-6435	Hex Resettable Latched Bus Driver	4-40
HD-6436	Octal Bus Buffer/Driver	4-43
HD-6440	One-of-Eight Latched Decoder/Driver	4-46
HD-6495	Hex Bus Buffer/Driver	4-50

Table 4 – Microprocessor Support Systems

HARRIS PART NUMBER	DESCRIPTION	PAGE NUMBER
HB-61000	MICRO-12 Evaluation Board	6-4
HB-61001	4K by 12 Memory Board	6-8

*Digital Equipment Corp

System Architecture

Figure 2 shows the architecture of an HM-6100 system. Note that the Register Page and Auto Increment Registers which are an integral part of the processor architecture are located in memory rather than "on-chip". This permits a larger number of registers to be made available (128 per field) and they can be operated on by all Memory Reference Instructions rather than a separate group of "register operation" instructions.

The registers on the register page are true general purpose registers in that they can be accessed with a single word instruction from anywhere in the instruction field, and can be used as stack pointers, program vectors, or as memory locations.

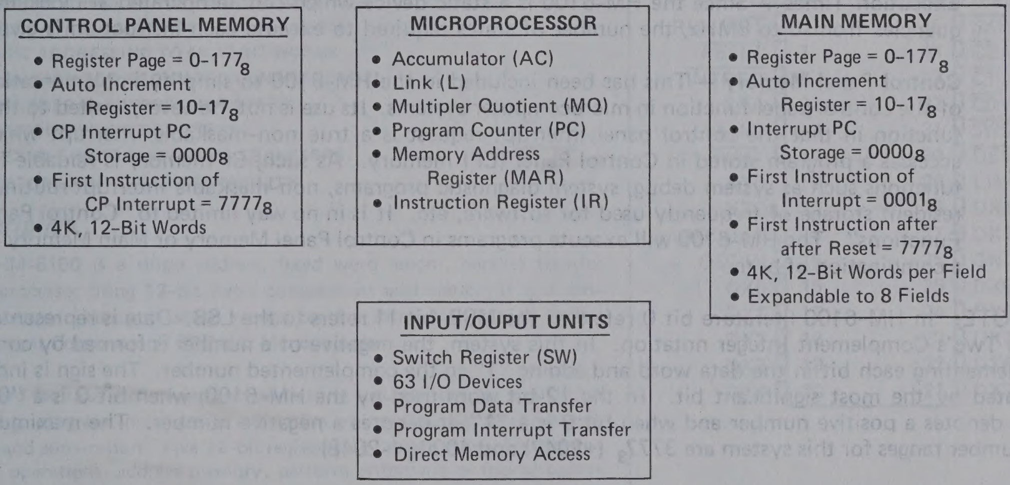

CONTROL PANEL MEMORY
• Register Page = 0-177$_8$
• Auto Increment Register = 10-17$_8$
• CP Interrupt PC Storage = 0000$_8$
• First Instruction of CP Interrupt = 7777$_8$
• 4K, 12-Bit Words
MICROPROCESSOR
• Accumulator (AC)
• Link (L)
• Multipler Quotient (MQ)
• Program Counter (PC)
• Memory Address Register (MAR)
• Instruction Register (IR)
MAIN MEMORY
• Register Page = 0-177$_8$
• Auto Increment Register = 10-17$_8$
• Interrupt PC Storage = 0000$_8$
• First Instruction of Interrupt = 0001$_8$
• First Instruction after after Reset = 7777$_8$
• 4K, 12-Bit Words per Field
• Expandable to 8 Fields
INPUT/OUPUT UNITS
• Switch Register (SW)
• 63 I/O Devices
• Program Data Transfer
• Program Interrupt Transfer
• Direct Memory Access

Figure 2 – HM-6100 System Architecture

Microprocessor Features

Since the HM-6100 bridges the gap between the microprocessor and minicomputer worlds, it has some features not found in most 8-bit microprocessors. These are explained more fully in the HM-6100 data sheet, but briefly they are:

Memory Reference Instructions (MRIs) – Combine the operation and the address of the operand in a single memory word. This eliminates the requirement for "immediate" instructions, shortens programs significantly, and speeds execution.

Memory Fields and Pages – The 32K memory space is conceptually divided into 4K word fields which are subdivided into 128 word pages. The memory reference instruction addresses are always specified relative to the beginning of a specific page, thus making software "page relocatable".

General Purpose Registers Located in Memory – The first 128 words of each memory field (page 0, or the Register Page) can be used as general purpose registers. Since they are located in memory, the MRIs are used to manipulate them rather than a separate set of "register instructions".

Auto Increment Registers – When locations $10\text{-}17_8$ of the register page are used as operand addresses they are automatically incremented prior to each use.

IOTs – There is an entire class of Input/Output transfer instructions. Hardware interfacing of the CPU to the various peripherals is simple and straight forward.

Microcode – Accumulator operations can be microcoded to tailor the instruction set to a particular application.

Execution Times – Since the HM-6100 is a static device which can be operated at clock frequencies from 0 to 8MHz, the number of states required to execute each instruction is given.

Control Panel Memory – This has been included in the HM-6100 to simplify implementation of the control panel function in microcomputer systems. Its use is not, however, limited to that function in that the control panel interrupt request is a true non-maskable interrupt which accesses a program stored in Control Panel (CP) memory. As such, CP memory is valuable for functions such as system debug, system diagnostic programs, non-maskable interrupt routines, resident storage of frequently used for software, etc. It is in no way limited to "Control Panel Functions". The HM-6100 will execute programs in Control Panel Memory or Main Memory or a combination of both.

NOTE: In HM-6100 literature bit 0 refers to the MSB, bit 11 refers to the LSB. Data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the HM-6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum number ranges for this system are 3777_8 (+2047) and 4000_8 (-2048).

System Flexibility

Using the HM-6100 family, the designer has access to a comprehensive product line dedicated to satisfy his particular system requirements. He also has a very low cost reproduction of the PDP-8/E minicomputer whose existence is justified by a large product market base and a wealth of existing software. The wide range of CMOS memory products enable partitioning of the memory system in blocks from 64 to 4096 words of RAM and from 256 to 1024 words of ROM or PROM.

DEVELOPMENT SUPPORT

The 6100 CPU family is supported by the Harris, single-board, CMOS MICRO-12 microcomputer and by existing PDP-8 minicomputers and their low cost operating systems.

HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6100
CMOS 12 BIT MICROPROCESSOR (CPU)

Features

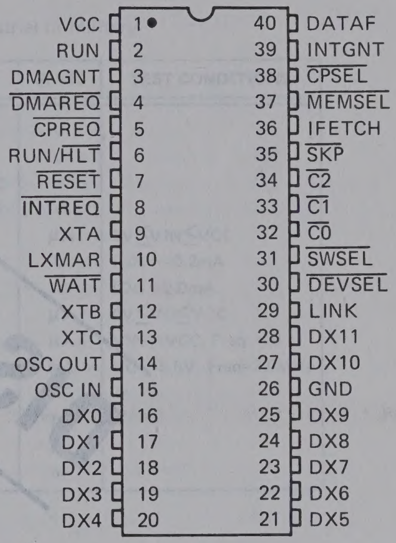
- LOW POWER - TYP. $< 5.0\mu W$
- SINGLE SUPPLY 4-11 VOLT
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- SINGLE PHASE CLOCK, ON CHIP CRYSTAL OSC.
- SOFTWARE COMPATIBLE WITH PDP-8/E
- 12-BIT DATA WORD
- OVER 90 SINGLE WORD INSTRUCTIONS
- RELOCATABLE MEMORY ORGANIZATION
- BASIC ADDRESSING TO 4K 12 BIT WORDS
- PROVISION FOR DEDICATED CONTROL PANEL
- 128 GENERAL PURPOSE REGISTERS
- 8 AUTOINDEXING REGISTERS
- FLEXIBLE PROGRAMMED I/O TRANSFERS
- VECTORED INTERRUPT CAPABILITY

Description

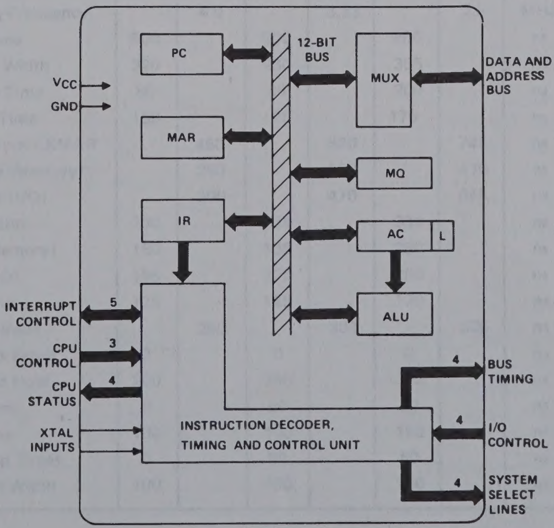
The HM-6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit two's complement arithmetic. It is a general purpose processor which recognizes the instruction set of Digital Equipment Corporation's PDP-8/E Minicomputer.

Standard features include indirect addressing and facilities for instruction skipping, program interrupts as a function of input/output device conditions, and auto-restart. Five 12-bit registers are used to control microprocessor operations, address memory, perform arithmetic or logical operations, and store data. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

Pinout


VCC 1
RUN 2
DMAGNT 3
DMAREQ 4
CPREQ 5
RUN/HLT 6
RESET 7
INTREQ 8
XTA 9
LXMAR 10
WAIT 11
XTB 12
XTC 13
OSC OUT 14
OSC IN 15
DX0 16
DX1 17
DX2 18
DX3 19
DX4 20
40 DATAF
39 INTGNT
38 CPSEL
37 MEMSEL
36 IFETCH
35 SKP
34 C2
33 C1
32 C0
31 SWSEL
30 DEVSEL
29 LINK
28 DX11
27 DX10
26 GND
25 DX9
24 DX8
23 DX7
22 DX6
21 DX5

Functional Diagram


PC
MAR
IR
12-BIT BUS
MUX
MQ
AC
L
ALU
DATA AND ADDRESS BUS
VCC
GND
INTERRUPT CONTROL
5
CPU CONTROL
3
CPU STATUS
4
XTAL INPUTS
INSTRUCTION DECODER, TIMING AND CONTROL UNIT
4
BUS TIMING
4
I/O CONTROL
4
SYSTEM SELECT LINES

DISCONTINUED

Specifications HM-6100

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HM-6100-9	-40°C to +85°C
Military HM-6100-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 10% Volts, T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-1.0		+1.0	μA	0V≤VIN≤VCC
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 2.0mA
IO	Output Leakage	-1.0		+1.0	μA	0V≤VO≤VCC
ICC1	Supply Current (Static)			400	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			2.5	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25°C VCC = 5.0V (1)		TA = Indust. VCC = 5.0 ± 10%V		TA = Military VCC = 5.0 ± 10%V			
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
fMAX	Max Operating Frequency		4.0		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	500		600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	220		230		355		ns	
TAS	Address Setup Time	80		85		200		ns	
TAH	Address Hold Time	150		125		175		ns	
TAL	Access Time from LXMAR		450		520		745	ns	
TEN	Output Enable (Memory)		250		300		470	ns	
TEND	Output Enable (I/O)		300		470		655	ns	
TWP	Write Pulse Width	200		235		330		ns	
TDS	Data Setup (Memory)	160		135		250		ns	
TDSD	Data Setup (I/O)	185		225		350		ns	
TDH	Data Hold Time	125		125		170		ns	
TST	Status Signals Valid		250		300		325	ns	
TRS	Request Inputs Setup	0		0		0		ns	
TRH	Request Inputs Hold	200		250		300		ns	
TWS	Wait Setup Time	0		50		50		ns	
TWH	Wait Hold Time	100		100		150		ns	
TRHS	Run Halt Setup Time	0		50		50		ns	
TRHP	Run Halt Pulse Width	100		100		150		ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.

Specifications HM-6100C-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	Gnd -0.3V to VCC +0.3V
Storage Temperature Range	-65oC to 150oC
Operating Temperature Range	
Industrial HM-6100C-9	-40oC to +85oC

ELECTRICAL CHARACTERISTICS VCC = 5.0 ± 5% Volts, T_A = Industrial

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIHC	Logical "1" Osc. Input Voltage	VCC-.5			V	
VIL	Logical "0" Input Voltage			.8	V	
VILC	Logical "0" Osc. Input Voltage			GND +.5	V	
IIL	Input Leakage (1)	-10		+10	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Volt. (2)	2.4			V	IOH = -0.2mA
VOL	Logical "0" Output Volt. (2)			0.45	V	IOL = 1.6mA
IO	Output Leakage	-10		+10	μA	$0V \leq VO \leq VCC$
ICC1	Supply Current (Static)			600	μA	VIN = VCC, Freq. = 0
ICC2	Supply Current (Operating)			5.0	mA	VCC=5.5V, Freq=2.0MHz
CI	Input Capacitance (3)		5	7	pF	
CO	Output Capacitance (3)		8	10	pF	
CIO	Input/Output Capacitance (3)		8	10	pF	
COSC	Oscillator IN/OUT CAP. (3)		30		pF	

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

A.C.

		TA = 25oC VCC=5.0V(1)		TA = Indust. VCC = 5.0 ± 5%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT	TEST CONDITION
fMAX	Max operating Freq.		3.33		2.5	MHz	CL = 50pF
TS	Major State Time	600		800		ns	See Timing Diagram
TLX	LXMAR Pulse Width	270		335		ns	
TAS	Address Setup Time	100		120		ns	
TAH	Address Hold Time	150		175		ns	
TAL	Access Time from LXMAR	500	500	650	650	ns	
TEN	Output Enable (Memory)	300	300	400	400	ns	
TEND	Output Enable (I/O)	350	350	575	575	ns	
TWP	Write Pulse Width	250		320		ns	
TDS	Data Setup (Memory)	180		240		ns	
TDSD	Data Setup (I/O)	200		275		ns	
TDH	Data Hold Time	130		175		ns	
TST	Status Signals Valid		300		350	ns	
TRS	Request Inputs Setup	0		0		ns	
TRH	Request Inputs Hold	100		130		ns	
TWS	Wait Setup Time	0		0		ns	
TWH	Wait Hold Time	100		130		ns	
TRHS	Run Halt Setup Time	0		70		ns	
TRHP	Run Halt Pulse Width	100		130		ns	

Note 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information – not guaranteed.

Timing and State Control

The HM-6100 generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500ns duration. The major timing states are described in Figure 1.

T1 For memory reference instructions, a 12-bit address is sent on the DataX, DX, lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T2 Memory/Peripheral data is read for an input transfer (READ). $\overline{\text{WAIT}}$ controls the transfer duration. If $\overline{\text{WAIT}}$ is active during input transfers, the CPU waits in the T2 state. The wait duration is an integral multiple of the crystal frequency - 250ns for 4MHz.

For Memory reference instructions, the Memory Select, $\overline{\text{MEMSEL}}$, lines are active. For I/O instruction the $\overline{\text{DEVSEL}}$, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$, and SKP are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, $\overline{\text{CPSEL}}$, and Switch Register Select, $\overline{\text{SWSEL}}$, become active low for data transfers between the HM-6100 and Control Panel Memory and the Switch Register, respectively.

T3, T4, T5
ALU operation and internal register transfers.

T6 This state is entered for an output transfer (WRITE). The address is defined during T1. $\overline{\text{WAIT}}$ controls the time for which the WRITE data must be maintained.

The following illustrates the timing of the CPU when its operating frequency is low enough that propagation delays can be ignored. It effectively shows the timing of the CPU when it is single clocked.

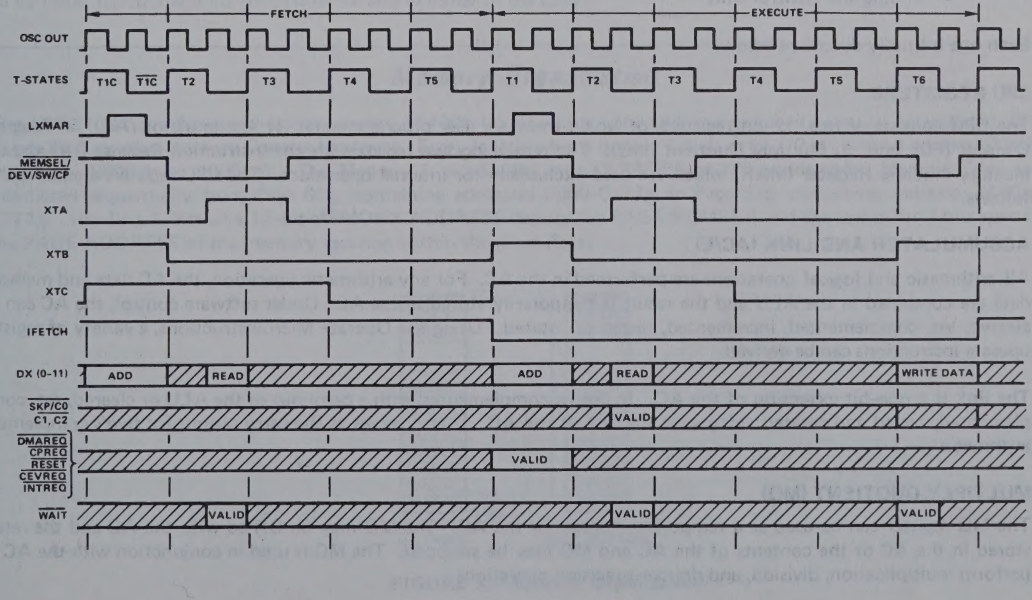


FIGURE 1 – Static Timing

The dynamic or high frequency timing illustrates the propagation delays at specified operating frequencies. (Refer to specifications) It defines the interface requirements for memory and I/O devices on the bus.

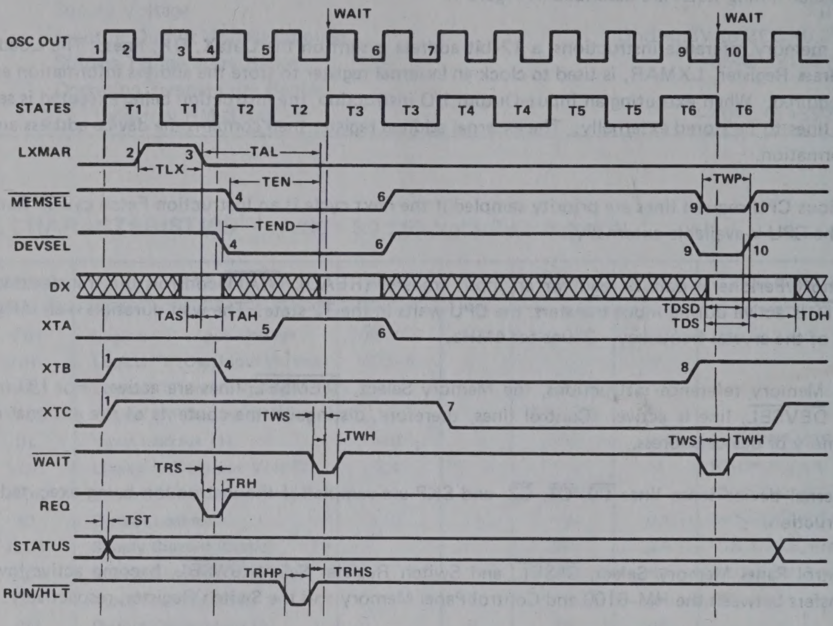


FIGURE 2 — Dynamic Timing

Microprocessor Architecture

The block diagram of the CPU architecture, shown on the front page, consists of the following major functional segments:

- CPU Registers
- Arithmetic and Logic Unit
- Dx-Bus Multiplexer
- Timing and Control Unit

Each one is briefly described below.

CPU REGISTERS

The CPU consists of five, 12-bit registers, of which three are user programmable; 1) Accumulator (AC), 2) Program Counter (PC), and 3) Multiply Quotient (MQ). The remaining two registers are the Instruction Register (IR) and the Memory Address Register (MAR) which are used exclusively for internal operations. The CPU registers are defined as follows.

ACCUMULATOR AND LINK (AC/L)

All arithmetic and logical operations are performed in the AC. For any arithmetic operation, the AC data and memory data are combined in the ALU and the result is temporarily stored in the AC. Under software control, the AC can be cleared, set, complemented, incremented, tested or rotated. Using the Operate Microinstructions, a variety of register operate instructions can be derived.

The link is a one-bit extension of the AC. It can be complemented with a carry out of the ALU or cleared, set, complemented, tested and rotated along with the rest of the AC. It also serves as the carry output for two's complement arithmetic.

MULTIPLY QUOTIENT (MQ)

The MQ register can be used as a temporary storage for the AC. The MQ may be OR'ed with the AC and the result stored in the AC or the contents of the AC and MQ may be swapped. The MQ is used in conjunction with the AC to perform multiplication, division, and double-precision operations.

PROGRAM COUNTER (PC)

The PC supports both memory and input-output device operations. For memory operations, the PC is controlled exclusively by internal logic and instructions fetched from memory. During an instruction fetch cycle the contents of the PC are transferred to the memory address register (MAR) while the current instruction is being decoded. The PC is then loaded with a new address or simply incremented for the next instruction depending upon the type of instruction. The next instruction obtained from memory is then loaded into the Instruction Register. For example, if the instruction is a JMP X, then the branch address X is loaded into the PC for program controlled branching.

Branching can also be controlled by an external device during input-output operations. This feature allows I/O controlled vectored interrupts.

MEMORY ADDRESS REGISTER (MAR)

The MAR contains the address of the memory location that is currently selected for memory or I/O read-write operations. It is also used for microprogram control during data transfers to and from memory and peripherals.

INSTRUCTION REGISTER (IR)

The instruction fetched from memory is held in the IR while being interpreted by the Instruction Decoder. The IR specifies the initial step of the microprogram sequence for each instruction and is also used to store temporary data for microprogram control.

ARITHMETIC AND LOGIC UNIT (ALU)

The ALU performs 12-bit arithmetic, logical and rotate operations. Its input is derived from the AC and any one of the other CPU registers. The type of operations performed by the ALU include:

ADD
Logical AND
Logical OR
Test AC
Left-right shifts and rotates
Increment
Complement
Set/Clear

DX-BUS MULTIPLEXER

To keep the CPU pin count to a reasonable 40 and still maintain a 12-bit word structure, the address and data paths are multiplexed by the DX-Bus Multiplexer. It handles data, address and instruction transfers between the CPU and memory or peripheral devices on a time-multiplexed basis.

TIMING AND CONTROL UNIT

The Timing and Control Unit generates the state and cycle timing signals from a single-phase clock and maintains the proper sequences of events required for any processing task. It also decodes the instruction obtained from the IR and combines the result with various timing signals and external control inputs to provide control and gating signals required by other functional units (both internal and external to the CPU).

Memory Organization

The HM-6100 has a basic addressing capacity of 4096 12-bit words. The addressing capacity may be extended to 32K words by Extended Memory Control hardware. Every location has a unique 4 digit octal (12 bit binary) address, 0000_8 to 7777_8 (0000_{10} to 4095_{10}). The Memory is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00_8, containing addresses 0000-0177_8, to Page 37_8, containing addresses 7600_8-7777_8. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

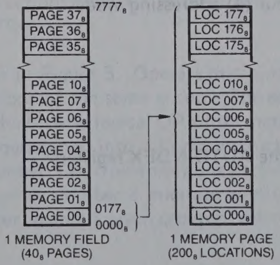


FIGURE 3 — Memory Organization

Memory and Processor Instructions

The HM-6100 instructions are 12-bit words stored in memory. The HM-6100 makes no distinction between instruction and data; it can manipulate instructions as stored variables or execute data as instructions. There are three general classes of HM-6100 instructions. They are Memory Reference Instructions (MRI), Operate Instructions (OPR), and Input/Output Transfer Instructions (IOT).

During an instruction fetch cycle, the HM-6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the "current" instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), 0000$_8$-0177$_8$, by definition, denotes the first 128 words of memory and is called the Register Page.)

Since the HM-6100 is a static design it can operate at any crystal frequency from 0 to 8MHz. State times required for execution are given for each instruction. Execution time can be calculated from the equation:

$$T = N*(2*(1/F))$$

where N is the number of state times and F is the crystal or input clock frequency.

MEMORY REFERENCE INSTRUCTIONS (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 4.

0 1 2	3	4	5 6 7 8 9 10 11
OP CODE 0 - 5	IA	MP	PAGE RELATIVE ADDRESS

IA: Indirect Addressing 0 = Direct; 1 = Indirect
MP: Memory Page 0 = Register Page; 1 = Current Page

FIGURE 4 – Memory Reference Instruction Format

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR REGISTER PAGE BIT. If bit 4 is a 0, the page address is interpreted as a location on the Register Page. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

By this Method, 256 locations may be directly addressed, 128 on the REGISTER PAGE and 128 on the CURRENT PAGE. Other locations are addressed by using bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in the REGISTER PAGE or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location. Note that locations 0010$_8$-0017$_8$ in the Register Page are AUTOINDEXED. When these locations are used for index registers their contents are incremented by 1 and restored before they are used as the operand address. These locations are therefore convenient for indexing applications.

Combinations of mode and page bits yield four (4) addressing modes:

- Current Page, Direct
- Current Page, Indirect
- Register Page, Direct
- Register Page, Indirect

A fifth addressing mode results from use of the AUTOINDEX registers:

- Register Page, Autoindexed

TABLE 1

MNE-MONIC	OP CODE	NUMBER OF STATES			OPERATION
		DIRECT	INDIRECT	AUTO-INDEXED	
AND	0XXX	10	15	16	LOGICAL AND: Causes a bit-by-bit boolean AND between the contents of the Accumulator and the contents of the effective address (XXX) specified by the instruction. The result is left in the AC and the data word in the referenced location is not altered.
TAD	1XXX	10	15	16	TWO'S COMPLEMENT ADD: Performs a binary two's complement addition between the specified data word and the contents of the AC; the result is left in the AC. If a carry out occurs, the state of the Link is complemented. If the AC is initially cleared, this instruction acts as a LOAD from memory.
ISZ	2XXX	16	21	22	INCREMENT AND SKIP IF ZERO: The contents of the effective address are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
DCA	3XXX	11	16	17	DEPOSIT AND CLEAR THE ACCUMULATOR: The contents of the AC are stored in the effective address and the AC is cleared.
JMS	4XXX	11	16	17	JUMP TO SUBROUTINE: The contents of the PC are stored in the effective address and the effective address + 1 is stored in the PC. The link, AC, and MQ are unchanged.
JMP	5XXX	10	15	16	JUMP: The effective address is loaded into the PC thus causing program execution to branch to a new location.
IOT	6XXX	17			INPUT/OUTPUT TRANSFER: Used to initiate the operation of peripheral devices and to transfer data between the peripherals and the CPU.
OPI	7XXX				OPERATE Instructions: Used to perform logical operations on the contents of the major registers.
		10			2 - Cycle OPERATE
		15			3 - Cycle OPERATE

Operate Instructions

The Operate Instructions, which have an OPCODE of 7_8(111), consist of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 micro instructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 5. Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third, and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	A								B

MICROINSTRUCTION	A	B
Group 1	0	0/1
Group 2	1	0
Group 3	1	1

FIGURE 5 – Basic OPR Instruction Format

GROUP 1 MICROINSTRUCTIONS

Figure 6 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 6.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	RAR	RAL	0/1	IAC

Logical Sequences:
1 - CLA CLL
2 - CMA CML
3 - IAC
4 - RAR RAL RTR RTL BSW

BIT 8	BIT 9	BIT 10	FUNCTION
0	0	1	BSW
0	1	0	RAL
0	1	1	RTL
1	0	0	RAR
1	0	1	RTR

FIGURE 6 – Group 1 Microinstruction Format

Table 2-1 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, and the number of states. The same format is followed in Table 3 and 4 which corresponds to group 2 and 3 microinstructions, respectively.

There are several commonly used microprogrammed combinations of group 1 microinstructions. These are listed in Table 2-2. When writing programs it is necessary to load various constants into the AC for such purposes as initiallizing counters and to provide comparisons. Table 2-3 lists those constants which can be loaded directly via microprogrammed combinations of group 1 instructions.

TABLE 2 - 1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7000	1	10	NO OPERATION - This instruction causes a 10 state delay in program execution, without affecting the state of the HM-6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.
CLA	7200	1	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary 0's.

FIGURE 2 - 1 Continued

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLL	7100	1	10	CLEAR LINK - The link is loaded with a binary 0.
CMA	7040	2	10	COMPLEMENT ACCUMULATOR - The content of each bit of the AC is complemented. This has the effect of replacing the contents of the AC with its one's complement.
CML	7020	2	10	COMPLEMENT LINK - The content of the link is complemented.
IAC	7001	3	10	INCREMENT ACCUMULATOR - The content of the AC is incremented by one (1) and the carry out componments the Link (L).
BSW	7002	4	15	BYTE SWAP - The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC(0) is swapped with AC(6), AC(1) with AC(7), etc. The link is not affected.
RAL	7004	4	15	ROTATE ACCUMULATOR LEFT - The content of the AC and L are rotated one binary position to the left. AC(0) is shifted to L and L is shifted to AC(11). The ROTATE instructions use what is commonly called a circular shift, meaning that any bit rotated off one end of the accumulator will reappear at the other end.
RTL	7006	4	15	ROTATE TWO LEFT - The contents of the AC and L are rotated two binary positions to the left. AC(1) is shifted to L and L is shifted to AC(10).
RAR	7010	4	15	ROTATE ACCUMULATOR RIGHT - The contents of the AC and L are rotated one binary position to the right. AC(11) is shifted to L and L is shifted to AC(0).
RTR	7012	4	15	ROTATE TWO RIGHT - The contents of the AC and L are rotated two binary positions to the right. AC(10) is shifted to L and L is shifted to AC(1).

TABLE 2 - 2

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
CLA CLL	7300	1	10	CLEAR ACCUMULATOR - CLEAR LINK
CIA	7041	2, 3	10	COMPLEMENT AND INCREMENT ACCUMULATOR - The content of the AC is replaced with its two's complement. The carry out complements the link. This is a microprogrammed combination of CMA and IAC.
STL	7120	1, 2	10	SET THE LINK - The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.
STA	7240	1, 2	10	SET THE ACCUMULATOR - Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.
CLA IAC	7201	1, 3	10	Sets the accumulator to a 1.

TABLE 2 - 2 Continued

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
GLK	7204	1, 4	15	GET LINK - The AC is cleared and the content of the link is shifted into AC(11) while a 0 is shifted into the link. This is a microprogrammed combination of CLA and RAL.
CLL RAL	7104	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR LEFT
CLL RTL	7106	1, 4	15	CLEAR LINK - ROTATE TWO LEFT
CLL RAR	7110	1, 4	15	CLEAR LINK - ROTATE ACCUMULATOR RIGHT
CLL RTR	7112	1, 4	15	CLEAR LINK - ROTATE TWO RIGHT

TABLE 2 - 3

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	DECIMAL CONSTANT	INSTRUCTIONS COMBINED
NL0000	7300	1	10	0	CLA CLL
NL0001	7301	1, 3	10	1	CLA CLL IAC
NL0002	7305	1, 3, 4	15	2	CLA CLL IAC RAL
NL0003	7325	1, 2, 3, 4	15	3	CLA CLL CML IAC RAL
NL0004	7307	1, 3, 4	15	4	CLA CLL IAC RTL
NL0006	7327	1, 2, 3, 4	15	6	CLA CLL CML IAC RTL
NL0100	7303	1, 3, 4	15	64	CLA IAC BSW
NL2000	7332	1, 2, 4	15	1024	CLA CLL CML RTR
NL3777	7350	1, 2, 4	15	2047	CLA CLL CMA RAR
NL4000	7330	1, 2, 4	15	-0	CLA CLL CML RAR
NL5777	7352	1, 2, 4	15	-1025	CLA CLL CMA RTL
NL6000	7333	1, 2, 3, 4	15	-1024	CLA CLL CML IAC RTR
NL7775	7346	1, 2, 4	15	-3	CLA CLL CMA RTL
NL7776	7344	1, 2, 4	15	-2	CLA CLL CMA RAL
NL7777	7340	1, 2	10	-1	CLA CLL CMA

GROUP 2 MICROINSTRUCTIONS

Figure 7 shows the instruction format of group 2 microinstructions, Bits 4 - 10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4 - 7 or 9 - 10 is set, the instruction is a microprogrammed combination group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 7.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA	SZA	SNL	*	OSR	HLT	0

Logical Sequences:
1 (BIT 8 = 0) -SMA or SZA or SNL
(BIT 8 = 1) -SPA or SNA or SZL
2 -CLA
3 -OSR, HLT

* Reverse sensing BIT:
Unconditional SKIP when
BITS 5, 6, & 7 are 0's

FIGURE 7 — Group 2 Microinstruction Format

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or when bit 8 is 1, the decision will be based on the logical AND.

TABLE 3 -1

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7400	1	10	NO OPERATION - See Group 1 microinstructions.
CLA	7600	2	10	CLEAR ACCUMULATOR - The accumulator is loaded with binary 0's.
HLT	7402	3	10	HALT - Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.
SKP	7410	1	10	SKIP - The content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	10	SKIP ON NON-ZERO LINK - The content of L is sampled; the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.
SZL	7430	1	10	SKIP ON ZERO LINK - The instruction is skipped if the link contains a 0.
SZA	7440	1	10	SKIP ON ZERO ACCUMULATOR - The content of the AC is sampled; the next sequential instruction is skipped if all AC bits are 0. If any bit in the AC is a 1, the next instruction is executed.
SNA	7450	1	10	SKIP ON NON-ZERO ACCUMULATOR - The next instruction is skipped if any one bit of the AC contains a 1. If every bit in the AC is 0, the next instruction is executed.
SMA	7500	1	10	SKIP ON MINUS ACCUMULATOR - If the content of AC(0) contains a negative two's complement number, the next sequential instruction is skipped. If AC(0) contains a 0, the next instruction is executed.
SPA	7510	1	10	SKIP ON POSITIVE ACCUMULATOR - If the content of AC(0) contains a 0, indicating a positive two's complement number, the next sequential instruction is skipped.
OSR	7404	3	15	OR WITH SWITCH REGISTER - The content of the Switch Register is inclusively OR'ed with the content of the AC and the result stored in the AC. The HM-6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B. This instruction provides the simplest way to input data to the HM-6100 from peripherals.
LAS	7604	1, 3	15	LOAD ACCUMULATOR WITH SWITCH REGISTER - The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.

Table 3 - 2 lists every legal combination of skip microinstructions, along with the resulting condition upon which the decision to skip or execute the next sequential instruction is based. When these combinations include a CLA, the accumulator is cleared after the decision is made. This is a useful trick to save code when a new value will be TAD'ed into the AC.

TABLE 3 - 2

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
SZA SNL	7460	1	10	Skip if AC = 0 or L = 1 or both.
SNA SZL	7470	1	10	Skip if AC ≠ 0 and L = 0.
SMA SNL	7520	1	10	Skip if AC < 0 or L = 1 or both.
SPA SZL	7530	1	10	Skip if AC ≥ 0 and L = 0.
SMA SZA	7540	1	10	Skip if AC ≤ 0.
SPA SNA	7550	1	10	Skip if AC > 0.
SMA SZA SNL	7560	1	10	Skip if AC ≤ 0 or L = 1 or both.
SPA SNA SZL	7570	1	10	Skip if AC > 0 and L = 0.

When writing an actual program, it is useful to think in terms of the FORTRAN relational operators - .LT., .EQ., etc.- when trying to compare numbers. The following method along with Table 3 - 3 will provide this.

```
CLA CLL         / Initialize AC and Link
TAD B           /Fetch 2nd number
CML CMA IAC     /Create "-B" (AC & L act like a 13 bit accumulator)
TAD A           /Fetch 1st number
Test    CLA     /Use instructions from Table 3 - 3 to provide test
                /The CLA is optional to provide a clear AC after test
JMP FAIL        /Branch to FAIL routine if test failed
. . .           /Test passed, continue with program
. .
```

TABLE 3 - 3

SKIP IF	UNSIGNED COMPARE	SIGNED COMPARE
A. NE. B	SNA	SNA
A. LT. B	SNL	SMA
A. LE. B	SNL SZA	SMA SZA
A. EQ. B	SZA	SZA
A. GE. B	SZL	SPA
A. GT. B	SZL SNA	SPA SAN

GROUP 3 MICROINSTRUCTIONS

Figure 8 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 8.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

Logical Sequences:

1 - CLA
2 - MQA, MQL
3 - NOP

*Don't care

FIGURE 8 - Group 3 Microinstruction Format

TABLE 4

MNE-MONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7401	3	10	NO OPERATION - See group 1 microinstructions.
CLA	7600	1	10	CLEAR ACCUMULATOR
MQA	7501	2	10	MQ REGISTER INTO ACCUMULATOR - The content of the MQ is logical OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.
MQL	7421	2	10	MQ REGISTER LOAD - The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost. This is similar to a DCA instruction.
ACL	7701	1, 2	10	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR - This is equivalent to a microprogrammed combination of CLA and MQA. It is similar to the two instruction combination of CLA and TAD.
CAM	7621	1, 2	10	CLEAR ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogram combination of CLA and MQL.
SWP	7521	2	10	SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are interchanged by accomplishing a microprogrammed combination of MQA and MQL.
CLA SWP	7721	1, 2	10	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.

Input Output Transfer Instructions (IOT)

The input/output transfer instructions, which have an OPCODE of 6_8 are used to initiate the operation of peripheral devices and to transfer data between peripherals and the HM-6100. Three types of data transfer may be used to receive or transmit information between the HM-6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12 bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, Transfers variable-size blocks of data between high-speed peripherals and the memory with minimum of program control required by the HM-6100.

IOT INSTRUCTION FORMAT

The Input/Output Transfer instruction format is represented in Figure 9.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	USER DEFINABLE BITS								

Basic IOT Instruction: $6XXX_8$

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	DEVICE SELECTION						CONTROL		

PDP-8/E Format: $6NNX_8$

FIGURE 9 — IOT Instruction Format

The first three bits, 0 - 2, are always set to 6_8 (110) to specify an IOT instruction. The next 9 bits, 3 - 11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3 - 8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9 - 11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the HM-6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT ②. This is referred to an IFETCH and consists of five (5) internal states. The HM-6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOTA and IOTB. Bits 0 - 11 of the IOT instruction are available on DX0 - 11 at IOTA ∧ LXMAR ③. These bits must be latched in an external address register. $\overline{\text{DEVSEL}}$ is active low to enalbe data transfers between the HM-6100 and the peripheral device ④ & ⑤. Input-Output Instruction Timing is shown in Figure 10. The selected peripheral device communicates with the HM-6100 through 4 control lines - $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$. In the HM-6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Tables 5-1 and 5-2.

The control line $\overline{\text{SKP}}$, when low during an IOT, causes the HM-6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C0, C1, and C2 lines are treated independently of the $\overline{\text{SKP}}$ line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the HM-6100, DX0 - 11, $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$ and $\overline{\text{SKP}}$, are sampled during IOTA on the rising edge of time state 3 ④. The data from the HM-6100 is available to the device during $\overline{\text{DEVSEL}}$ ∧ $\overline{\text{XTC}}$ ⑤. The IOTB cycle is internal to the HM-6100 to perform the operations requested during IOTA. Both IOTA and IOTB consists of six (6) internal states.

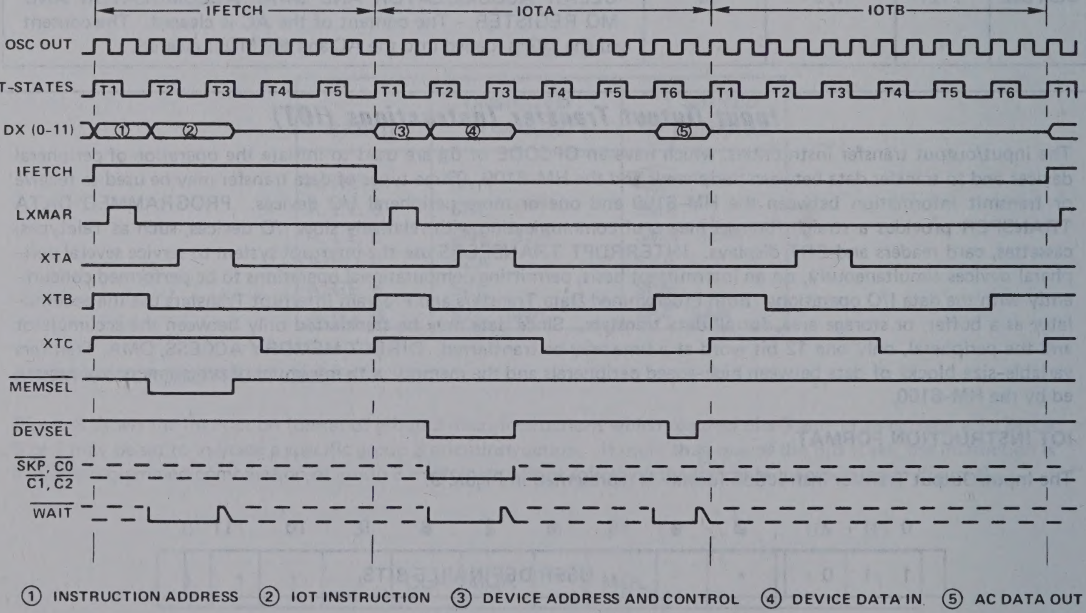


FIGURE 10 — Input-output instruction timing

TABLE 5 - 1
AC DATA TRANSFERS

CONTROL LINES					
$\overline{\text{SKP}}$	$\overline{\text{C0}}$	$\overline{\text{C1}}$	$\overline{\text{C2}}$	OPERATION	DESCRIPTION
H	H	H	H	DEV ← AC	The content of the AC is sent to the device.
H	L	H	H	DEV ← AC; CLA	The content of the AC is sent to a device and then the AC is cleared.
H	H	L	H	AC ← AC V DEV; DEV ← AC	Data is received from a device OR'ed with the data in the AC and the result is stored in the AC. The new AC content is sent to the device.
H	L	L	H	AC ← DEV; DEV ← AC	Data is received from a device and loaded into the AC. The new AC content is sent to the device.
L	H	H	H	DEV ← AC; PC ← PC + 1	The content of the AC is sent to the device and the microprocessor skips the next sequential instruction.
L	L	H	H	DEV ← AC; CLA; PC ← PC + 1	The content of the AC is sent to a device, the AC is cleared, and the microprocessor skips the next sequential instruction.
L	H	L	H	AC ← AC V DEV; DEV ← AC; PC ← PC + 1	Data is OR'ed into the AC, the new AC sent to the device, and the microprocessor skips the next sequential instruction.
L	L	L	H	AC ← DEV; DEV ← AC PC ← PC + 1	Data is loaded into the AC, the new AC contents sent to the device, and the next sequential instruction skipped.

TABLE 5 - 2
PC VECTOR TRANSFERS

CONTROL LINES					
$\overline{\text{SKP}}$	$\overline{\text{C0}}$	$\overline{\text{C1}}$	$\overline{\text{C2}}$	OPERATION	DESCRIPTION
H	*	H	L	PC ← PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
H	*	L	L	PC ← DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.
L	*	H	L	PC ← PC + DEV; PC ← PC + 1	The RELATIVE JUMP is performed and then the microprocessor skips the next sequential instruction.
L	*	L	L	PC ← DEV; PC ← PC + 1	The ABSOLUTE JUMP is executed and then the next sequential instruction is skipped.

* Don't Care

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the HM-6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that is requires some sort of intervention from the running program.

TABLE 6
PROCESSOR IOT INSTRUCTIONS

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON - If Interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON - The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction.
IOF	6002	INTERRUPT TURN OFF - The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST - The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS - The following machines states are read into the indicated bits of AC. bit 0 - Link bit 1 - Greater than flag* bit 2 - INT request bus bit 3 - Interrupt Inhibit FF* bit 4 - Interrupt Enable FF* bit 5 - User flag* bit 6 - 11 - Save Field Register* * These bits are modified by external devices driving the DX bus and the $\overline{\text{C}}$-lines ($\overline{\text{C0}}$ = L, $\overline{\text{C1}}$ = L). For example, bits 1 and 6 - 11 are part of the Extended Memory Control.
RTF	6005	RETURN FLAGS - Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control). ($\overline{\text{C0}}$ = H, $\overline{\text{C1}}$ = H)
SGT	6006	SKIP ON GREATER THAN FLAG - Operation is determined by external devices, if any. This flag is external and must control the skip line.
CAF	6007	CLEAR ALL FLAGS - AC and link are cleared. Interrupt system is disabled.

The interrupt system allows certain external conditions to interrupt the computer program by driving the $\overline{\text{INTREQ}}$ input to the HM-6100 low. If no higher priority requests are outstanding and the interrupt system is enabled, the HM-6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the HM-6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The current content of the Program Counter, PC, is deposited in location 0000_8 of the memory and the program fetches the instruction from location 0001_8. The return address is available in location 0000_8. This address must be saved, possibly in a software stack, if nested interrupts are permitted. The INTGNT signal is activated by the HM-6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

The user program controls the interrupt mechanism of the HM-6100 by executing the processor IOT instructions listed in Table 6. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words.

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the perferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The HM-6100 is involved only is setting up the transfer; the transfers take place with no processor intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The HM-6100 grants the $\overline{\text{DMAREQ}}$ by activating the $\overline{\text{DMAGNT}}$ signal at the end of the current instruction. The HM-6100 suspends any further instruction fetches until the $\overline{\text{DMAREQ}}$ line is released. The DX lines are tri-stated, all $\overline{\text{SEL}}$ lines are high, and the external timing signals XTA, XTB, and XTC are active. The device which generated the $\overline{\text{DMAREQ}}$ must provide the address and necessary control signals to the memory for data transfers. The $\overline{\text{DMAREQ}}$ line can also be used as a level sensitive "pause" line.

Control Panel Interrupt Transfer

The HM-6100 CPU provides a unique Control Panel (CP) feature through its CPREQ input and CPSEL output lines. After acknowledging the control panel request, the CPU generates the necessary timing to execute program code in CP memory while also providing the capability to transfer data between CP memory and the user memory using the AC as a buffer. This allows the user memory to be examined and/or modified by the CP software. The CPU will output the MEMSEL signal for all user memory references while the CPSEL signal is generated for CP memory references as shown in Figure 11.

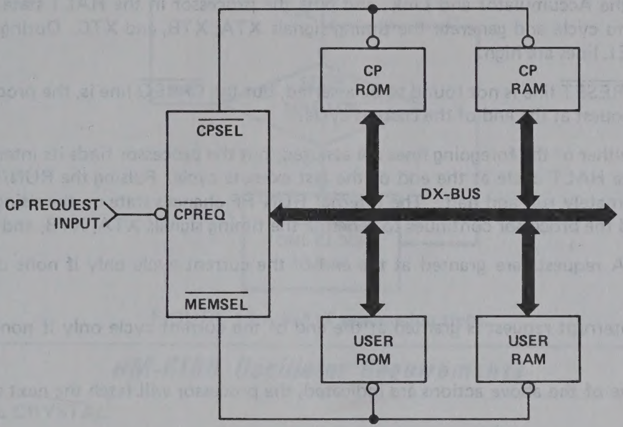


FIGURE 11 – Control Panel Block Diagram

The designer can make use of the control panel features to implement various functions that will be "transparent" to the user's (main) memory. Some of the more common functions include:

- Binary Loader and Punch
- Register Examination and Modification
- Single Cycle
- Octal Debug with Breakpoints
- Octal listing
- Auto Bootstrap

When a CPREQ is granted the PC is stored in location 0000 of Panel Memory and the HM-6100 resumes operation at location 7777 of the Panel Memory. The CPREQ bypasses the interrupt enable system and the processor IOT instruction, ION and IOF, are ignored while the HM-6100 is in the Control Panel Mode. Once a CPREQ is granted, the HM-6100 will not recognize any DMAREQ or INTREQ until the CPREQ has been fully serviced.

During Control Panel program execution access to the user memory is gained through use of indirect TAD, AND, DCA and ISZ instructions. The CPU will transfer control from CPSEL to MEMSEL during the execute phase of these instructions. The instructions are always fetched from control panel memory.

Exiting from the control panel routine is achieved by executing the following sequence:

- ION
- JMP I 0000 /Exit via location 0000 in Panel Memory

Location 0000 contains either the original return address deposited by the HM-6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine.

Internal Priority Structure

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in in Figure 12. The state of the priority network decides the next sequence of the HM-6100.

The CPU samples the RESET line, the request lines CPREQ, DMAREQ, and INTREQ, and the state of its internal RUN flip-flop during the last execute cycle of each instruction. The worst case response time of the HM-6100 to an external request is, therefore the time required to execute the longest instruction preceded by any 6-state execution cycle. For the HM-6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14 μs at 4MHz clock frequency.

When the HM-6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the HM-6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two HM-6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition of RUN/HLT should occur at least 10 clock pulses after RESET to be recognized.

The priority hierarchy is:

- RESET - If the RESET line is asserted at the sample time, the processor immediately sets its program counter to 7777, clears the Accumulator and Link, and puts the processor in the HALT state. While halted, the processor continues to cycle and generate the timing signals XTA, XTB, and XTC. During reset the DX line is tri-stated and the SEL lines are high.
- CPREQ - If the RESET line is not found to be asserted, but the CPREQ line is, the processor grants the control panel interrupt request at the end of the current cycle.
- RUN/HLT - If neither of the foregoing lines are asserted, but the processor finds its internal RUN FF in the halt state, it enters the HALT cycle at the end of the last execute cycle. Pulsing the RUN/HLT line low causes the HM-6100 to alternately run and halt. The internal RUN FF changes state on the rising edge of the RUN/HLT line. While halted the processor continues to generate the timing signals XTA, XTB, and XTC.
- DMAREQ - DMA requests are granted at the end of the current cycle only if none of the above actions are pending.
- INTREQ - An interrupt request is granted at the end of the current cycle only if none of the higher priority lines preempts it.
- IFETCH - If none of the above actions are indicated, the processor will fetch the next sequential instruction in the next cycle.

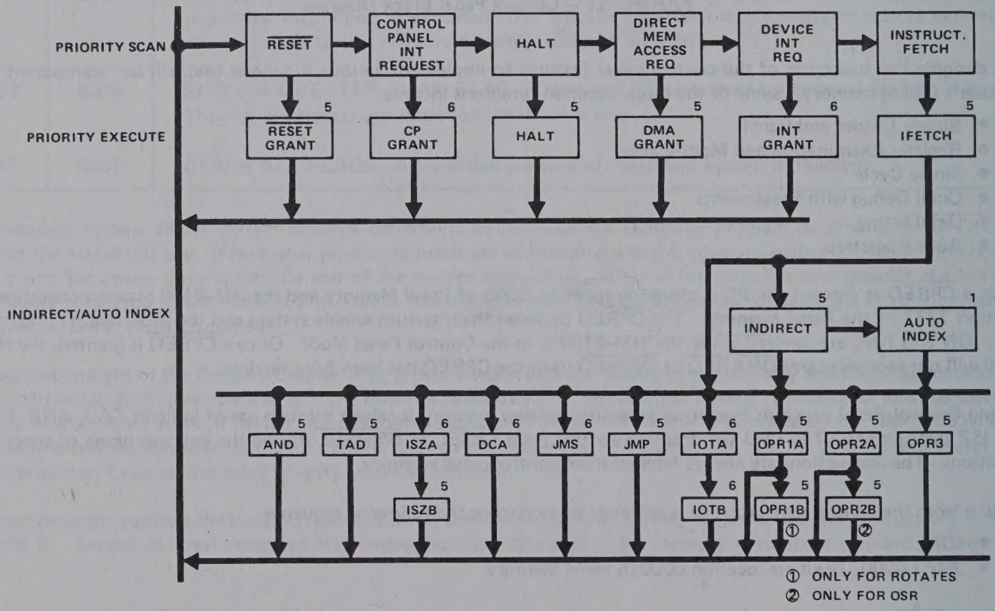

PRIORITY SCAN
RESET
CONTROL PANEL INT REQUEST
HALT
DIRECT MEM ACCESS REQ
DEVICE INT REQ
INSTRUCT. FETCH
5
6
5
5
6
5
PRIORITY EXECUTE
RESET GRANT
CP GRANT
HALT
DMA GRANT
INT GRANT
IFETCH
INDIRECT/AUTO INDEX
5
1
INDIRECT
AUTO INDEX
5
5
6
6
6
5
6
5
5
5
AND
TAD
ISZA
DCA
JMS
JMP
IOTA
OPR1A
OPR2A
OPR3
5
6
5
5
ISZB
IOTB
OPR1B
OPR2B
①
②
① ONLY FOR ROTATES
② ONLY FOR OSR

FIGURE 12 – Major processor states and number of clock cycles in each state.

Use of Wait Input

The HM-6100 samples the WAIT line during input-output data transfers. The WAIT line, if active low, controls the transfer duration. If WAIT is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), WAIT controls the time for which the write data is maintained on the DX lines by extending the T6 state. When operating at the max frequency, the internal delay of the HM-6100 causes the falling edge select lines to be past the WAIT setup time for WRITE. The rising edge of the select line for READ can be used to activate WAIT for a WRITE. The wait duration is an integral multiple of the oscillator time period (Figure 13).

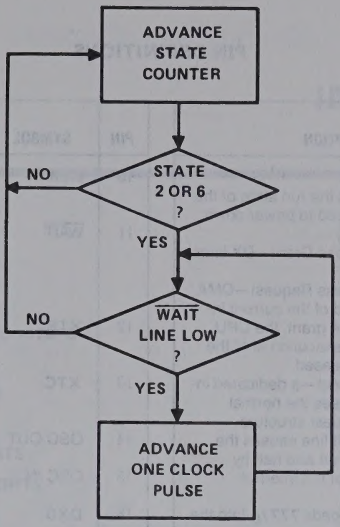


FIGURE 13 – $\overline{\text{WAIT}}$ sequencing steps.

HM-6100 Oscillator Requirements

USING AN EXTERNAL CRYSTAL

An inexpensive crystal can be used thereby eliminating the need for a clock generator. The crystal operates at parallel resonance, and thus is looks inductive in the circuit. An "AT" cut crystal should be used because it has a low temperature coefficient and can be used over a wide temperature range. The Feedback resistor and shunt capacitance are included internally. The crystal parameters needed are:

- Frequency
- Mod of Resonance - Parallel (anti-resonant)
- Maximum Power level - 1 milliwatt
- Load Capacitance - 32pF
- Series Resistance (max) - 250Ω

For precise frequency determination the effect of the stray circuit capacitance and internal 30pF capacitance must be taken into account.

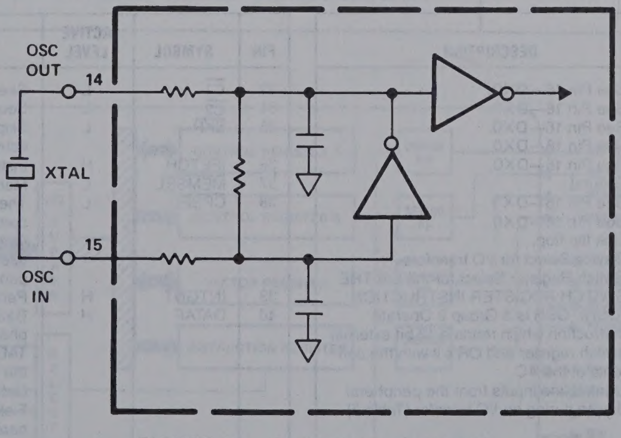


FIGURE 14 – Oscillator input schematic

USING AN EXTERNAL CLOCK GENERATOR

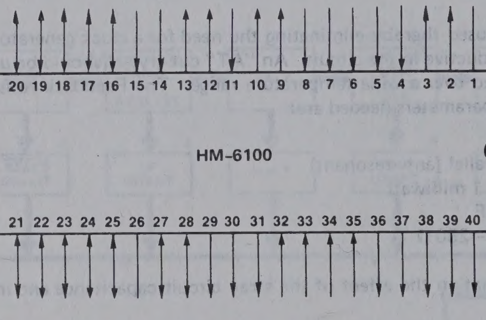
When a system clock is needed, eg. for a baud rate generator for UARTs, the HM-6100 can be externally clocked, thus eliminating the need for separate crystals. The external clock can be connected to the oscillator output pin while grounding oscillator input. This has the effect of over driving the small internal oscillator inverter causing an increase in supply current.

Duty cycle - 50/50
T_{rise}, T_{fall} - 20ns

PIN DEFINITIONS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	VCC		Supply voltage.
2	RUN	H	The signal indicates the run state of the CPU and may be used to power down the external circuitry
3	DMAGNT	H	Direct Memory Access Grant—DX lines are three-state.
4	$\overline{\text{DMAREQ}}$	L	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the $\overline{\text{DMAREQ}}$ line is released.
5	$\overline{\text{CPREQ}}$	L	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	RUN/$\overline{\text{HLT}}$	L	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/$\overline{\text{HLT}}$ flip flop.
7	$\overline{\text{RESET}}$	L	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	$\overline{\text{INTREQ}}$	L	Peripheral device interrupt request.
9	XTA	H	External coded minor cycle timing—signifies input transfers to the HM-6100.

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
10	LXMAR	H	The Load External Address Register is used to store memory and peripheral address externally.
11	$\overline{\text{WAIT}}$	L	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as $\overline{\text{WAIT}}$ is active. The CPU is in the lowest power state with clocks running.
12	XTB	H	External coded minor cycle timing—signifies output transfers from the HM-6100 .
13	XTC	H	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT		Crystal input to generate the internal timing (also external clock input).
15	OSC IN		See Pin 14—OSC OUT (also external clock ground)
16	DX0		DataX—multiplexed data in, data out and address lines.
17	DX1		See Pin 16—DX0.
18	DX2		See Pin 16—DX0.
19	DX3		See Pin 16—DX0.
20	DX4		See Pin 16—DX0.



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX5		See Pin 16—DX0.
22	DX6		See Pin 16—DX0.
23	DX7		See Pin 16—DX0.
24	DX8		See Pin 16—DX0.
25	DX9		See Pin 16—DX0.
26	GND		Ground
27	DX10		See Pin 16—DX0.
28	DX11		See Pin 16—DX0.
29	LINK	H	Link flip flop.
30	$\overline{\text{DEVSEL}}$	L	Device Select for I/O transfers.
31	$\overline{\text{SWSEL}}$	L	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	$\overline{\text{C0}}$	L	Control line inputs from the peripheral device during an I/O transfer (Table 5).

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
33	$\overline{\text{C1}}$	L	See Pin 32—C0.
34	$\overline{\text{C2}}$	L	See Pin 32—C0.
35	$\overline{\text{SKP}}$	L	Skips the next sequential instruction if active during an I/O instruction. (Table 5)
36	IFETCH	H	Instruction Fetch Cycle
37	$\overline{\text{MEMSEL}}$	L	Memory Select for memory transfers.
38	$\overline{\text{CPSEL}}$	L	The Control Panel Memory Select becomes active, instead of the $\overline{\text{MEMSEL}}$, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device Interrupt Grant
40	DATAF	H	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

HARRIS
SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6101
CMOS PARALLEL INTERFACE ELEMENT (PIE)

Features

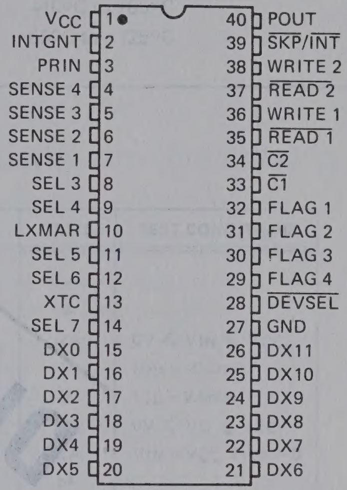
- HM-6100 COMPATIBLE
- LOW POWER STANDBY -500µW MAX
- SINGLE SUPPLY 4-11 VOLTS
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- 4 PROGRAMMABLE OUTPUTS (FLAGS)
- 4 PROGRAMMABLE SENSE INPUTS
- CONTROL FOR TWO 12 BIT INPUT PORTS
- CONTROL FOR TWO 12 BIT OUTPUT PORTS
- PRIORITY VECTORED INTERRUPTS
- UP TO 31 PIE'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIE CONTROL

Description

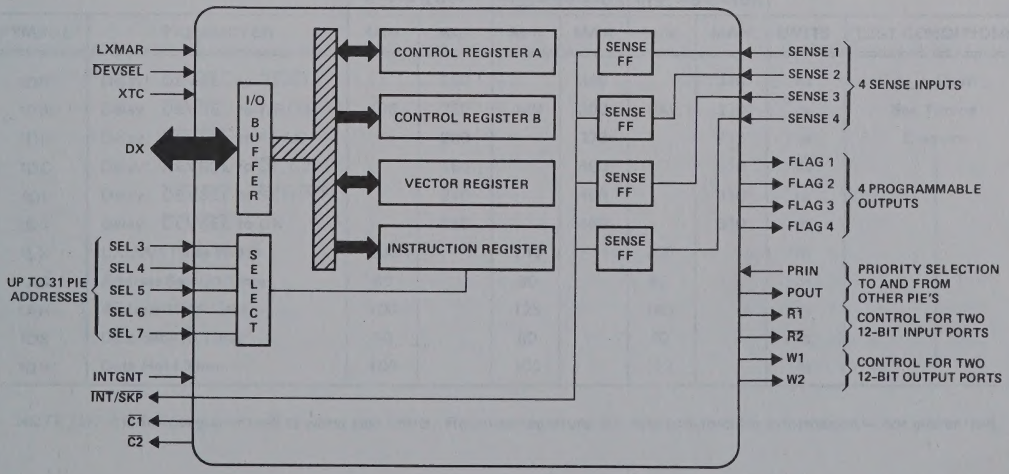
The HD-6101 Parallel Interface Elements (PIE) are high speed, low power, silicon gate CMOS general purpose devices which provide addressing interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via Input-Output Transfer (IOT) instructions, control lines and DX bus.

Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. Internal PIE registers are programmed under software control for write polarities, sense levels or edges, flag values and interrupt enables. Another software controlled register stores the address for vectored interrupt operation.

Pinout


VCC 1
INTGNT 2
PRIN 3
SENSE 4 4
SENSE 3 5
SENSE 2 6
SENSE 1 7
SEL 3 8
SEL 4 9
LXMAR 10
SEL 5 11
SEL 6 12
XTC 13
SEL 7 14
DX0 15
DX1 16
DX2 17
DX3 18
DX4 19
DX5 20
40 POUT
39 $\overline{\text{SKP/INT}}$
38 WRITE 2
37 $\overline{\text{READ 2}}$
36 WRITE 1
35 $\overline{\text{READ 1}}$
34 $\overline{\text{C2}}$
33 $\overline{\text{C1}}$
32 FLAG 1
31 FLAG 2
30 FLAG 3
29 FLAG 4
28 $\overline{\text{DEVSEL}}$
27 GND
26 DX11
25 DX10
24 DX9
23 DX8
22 DX7
21 DX6

Functional Diagram


LXMAR
$\overline{\text{DEVSEL}}$
XTC
DX
I/O BUFFER
CONTROL REGISTER A
CONTROL REGISTER B
VECTOR REGISTER
INSTRUCTION REGISTER
SENSE FF
SENSE FF
SENSE FF
SENSE FF
SENSE 1
SENSE 2
SENSE 3
SENSE 4
4 SENSE INPUTS
FLAG 1
FLAG 2
FLAG 3
FLAG 4
4 PROGRAMMABLE OUTPUTS
UP TO 31 PIE ADDRESSES
SEL 3
SEL 4
SEL 5
SEL 6
SEL 7
SELECT
PRIN
POUT
PRIORITY SELECTION TO AND FROM OTHER PIE'S
$\overline{\text{R1}}$
$\overline{\text{R2}}$
CONTROL FOR TWO 12-BIT INPUT PORTS
W1
W2
CONTROL FOR TWO 12-BIT OUTPUT PORTS
INTGNT
$\overline{\text{INT/SKP}}$
$\overline{\text{C1}}$
$\overline{\text{C2}}$

DISCONTINUED

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC + 0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101-9	-40°C to +85°C
Military HD-6101-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		+1.0	µA	0V ⩽ V_{IN} ⩽ VCC
V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage	-1.0		+1.0	µA	0V ⩽ V_O ⩽ VCC
I_{CC}	Supply Current (Static)		1.0	100	µA	V_{IN} = VCC, Freq. = 0
C_I	Input Capacitance(2)		5	7	pF	
C_O	Output Capacitance(2)		8	10	pF	
C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTE: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

		T_A = 25°C V_{CC} = 5.0V(1)		T_A = INDUSTRIAL V_{CC} = 5V ±10%		T_A = MILITARY V_{CC} = 5V ±10%			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
t_{DR}	Delay: $\overline{\text{DEVSEL}}$ to $\overline{\text{READ}}$		200		300		330	ns	C_L = 50pF
t_{DW}	Delay: $\overline{\text{DEVSEL}}$ to WRITE	100	220	140	300	150	330	ns	See Timing
t_{DF}	Delay: $\overline{\text{DEVSEL}}$ to FLAG		200		375		415	ns	Diagram
t_{DC}	Delay: $\overline{\text{DEVSEL}}$ to $\overline{\text{C1}}$, $\overline{\text{C2}}$		160		460		510	ns	
t_{DI}	Delay: $\overline{\text{DEVSEL}}$ to $\overline{\text{SKP/INT}}$		210		460		510	ns	
t_{DA}	Delay: $\overline{\text{DEVSEL}}$ to DX		350		460		510	ns	
t_{LX}	LXMAR Pulse Width	200		240		265		ns	
t_{AS}	Address Set-Up Time	60		80		90		ns	
t_{AH}	Address Hold Time	100		125		140		ns	
t_{DS}	Data Set-Up Time	50		80		80		ns	
t_{DH}	Data Hold Time	100		100		110		ns	

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

Specifications HD-6101C-9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND - 0.3V) to (VCC +0.3V)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6101C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%; T_A = Industrial

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			.8	V	
I_{IL}	Input Leakage	-10		+10	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{OH}	Logical "1" Output Voltage(1)	2.4			V	I_{OH} = -0.2mA
V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 1.6mA
I_O	Output Leakage	-10		+10	μA	$0V \leqslant V_O \leqslant V_{CC}$
I_{CC}	Supply Current (Static)		1.0	800	μA	V_{IN} = V_{CC}, Freq. = 0
C_I	Input Capacitance(2)		5	7	pF	
C_O	Output Capacitance(2)		8	10	pF	
C_{IO}	Input/Output Capacitance(2)		8	10	pF	

NOTES: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

A.C.

SYMBOL	PARAMETER	T_A = 25°C V_{CC} = 5.0V(1) MIN	MAX	T_A = INDUSTRIAL V_{CC} = 5V ±5% MIN	MAX	UNITS	TEST CONDITIONS
t_{DR}	Delay: $\overline{DEVSEL}$ to $\overline{READ}$		230		375	ns	C_L = 50pF See Timing Diagram
t_{DW}	Delay: $\overline{DEVSEL}$ to WRITE	100	240	125	375	ns	
t_{DF}	Delay: $\overline{DEVSEL}$ to FLAG		230		475	ns	
t_{DC}	Delay: $\overline{DEVSEL}$ to $\overline{C1}$, $\overline{C2}$		190		560	ns	
t_{DI}	Delay: $\overline{DEVSEL}$ to $\overline{SKP/INT}$		250		560	ns	
t_{DA}	Delay: $\overline{DEVSEL}$ to DX		400		560	ns	
t_{LX}	LXMAR Pulse Width	230		300		ns	
t_{AS}	Address Set-Up Time	80		100		ns	
t_{AH}	Address Hold Time	120		150		ns	
t_{DS}	Data Set-Up Time	60		90		ns	
t_{DH}	Data Hold Time	120		150		ns	

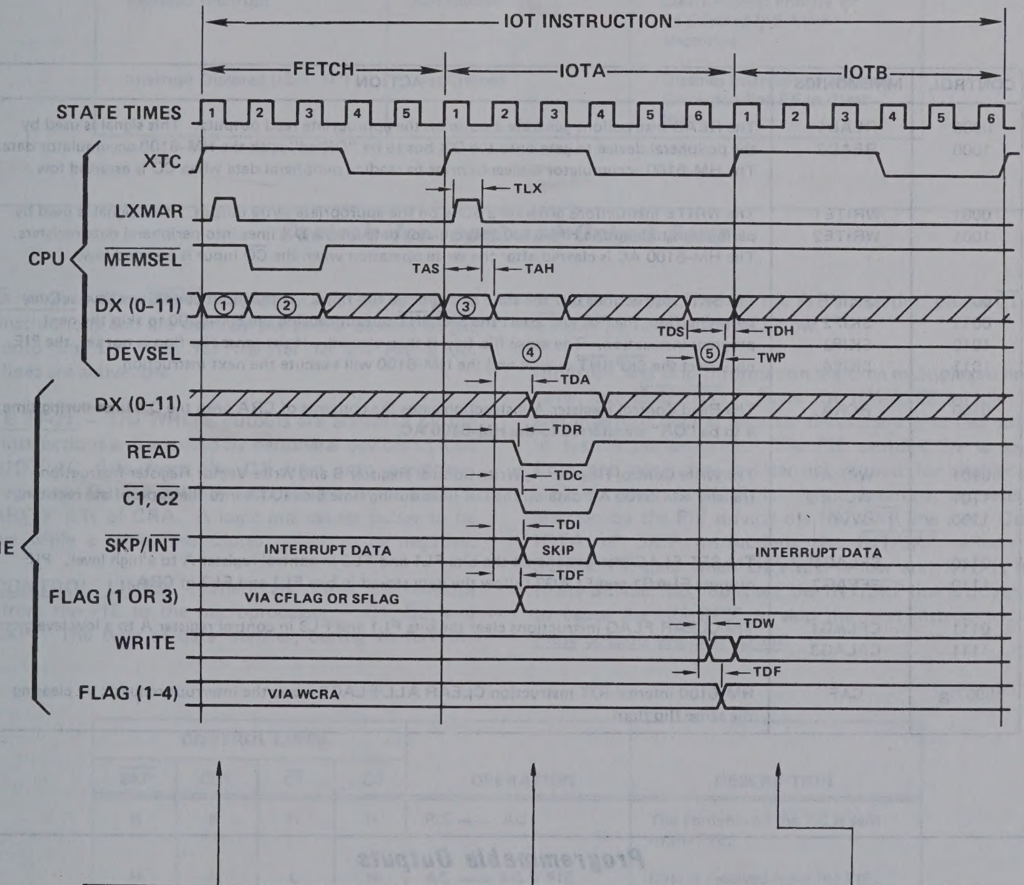
NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.

Timing Diagram

Timing for a typical transfer is shown below. During an instruction fetch the processor places the contents of the PC on the bus ① and obtains from memory an IOT instruction of the form 6XXX ② . During IOTA of the execute phase the processor places that instruction back on the DX lines ③ and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is high ④ is used by the addressed PIE along with the decoded control information to generate CPU control signals $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{SKP}}$. Also at this time either the Control Register A or the Interrupt Vector Register are outputed on the DX lines, or control outputs $\overline{\text{READ1}}$ and $\overline{\text{READ2}}$ are generated to gate peripheral data to the DX lines. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is low ⑤ is used to generate WRITE 1 and WRITE 2 controls. These signals are used to latch accumulator data into peripheral devices.

All PIE timing is generated from HM-6100 signals LXMAR, $\overline{\text{DEVSEL}}$, and XTC. No additional timing signals, clocks, or one shots are required.

Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the HM-6100.


IOT INSTRUCTION
FETCH
IOTA
IOTB
STATE TIMES
1
2
3
4
5
1
2
3
4
5
6
1
2
3
4
5
6
CPU
XTC
LXMAR
MEMSEL
DX (0-11)
DEVSEL
PIE
DX (0-11)
READ
C1, C2
SKP/INT
FLAG (1 OR 3)
WRITE
FLAG (1-4)
①
②
③
④
⑤
TLX
TAS
TAH
TDS
TDH
TWP
TDA
TDR
TDC
TDI
TDF
TDW
TDF
INTERRUPT DATA
SKIP
INTERRUPT DATA
VIA CFLAG OR SFLAG
VIA WCRA

Sense FF are sampled when LXMAR is high by the PIE.

DX data, $\overline{\text{C0}}$, $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{SKP}}$ are read by the HM-6100 on the rising edge of T3.

Interrupts are sampled by the HM-6100 on the rising edge of T2.

Pie Address and Instructions

The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the pin programmable select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIEs. Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded by the PIE to select one of 16 instructions which are described below.

PIE INSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0	ADDRESS					CONTROL			

CONTROL	MNEMONICS	ACTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be "OR'ed" with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when $\overline{\text{CO}}$ is asserted low.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the $\overline{\text{CO}}$ input is asserted low.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the $\overline{\text{SKP}}/\overline{\text{INT}}$ output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE not assert the $\overline{\text{SKP}}/\overline{\text{INT}}$ output and the HM-6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time 4 to be "OR" transferred to the HM-6100 AC.
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time 5 of IOTA into the appropriate register.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

Programmable Outputs

FLAGs (1-4) - The FLAGs are general purpose outputs that can be set and cleared under program control. GLAG1 follows bit FL1 in Control Register A and etc. FLAGs can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

Programmable Sense Inputs

The sense inputs are used to set sense flip flops (SENSE FF) inside the PIE. For each sense input there are two FF's, one for skip and one for interrupt. Conditions for setting each SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB.

The SENSE FF's are sampled when LXMAR is high. Interrupt requests are generated only when the sense flip flops are set by an edge and interrupts are enabled by writing to control reg A. Sense flip flops are reset on the following conditions.

	SENSE FLIP FLOPS	
CONDITION	**SKIP FF**	**INTERRUPT FF**
CAF Instruction (6007_8)	Clears All	Clears All
SKIP Instruction	Clears Corresponding FF	Clears Corresponding FF
Vectored Interrupt	Not Cleared	Clears Highest Priority FF on Selected PIE After Vectoring
Interrupt Disabled (IE = "0")	Not Cleared	Disables Interrupt by Holding Corresponding FF in Reset State

Controls for Input and Output Ports

$\overline{\text{READ}}$ (1-2) – The $\overline{\text{READ}}$ outputs are activated by the read instructions and are used by peripheral devices to get data onto the DX lines for transfer to the HM-6100. Read lines are active low.

WRITE (1-2) – The WRITE outputs are activated by the write instructions and are used by peripheral devices to load HM-6100 AC data from the DX lines into peripheral data registers. Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

I/O CONTROL LINES – There are three I/O control lines from the PIE to the microprocessor – $\overline{\text{C1}}$, $\overline{\text{C2}}$, and $\overline{\text{INT/SKP}}$. The type of data transfer, during an IOT instruction, is specified by the PIE's assertion of the $\overline{\text{C1}}$ and $\overline{\text{C2}}$ control lines as shown below.

Interrupt and skip information are time multiplexed on the same line ($\overline{\text{SKP/INT}}$). Since the HM-6100 samples skip and interrupt data at separate times there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits (IE1-4) when LXMAR is high. Interrupt requests are asserted by the PIE driving the $\overline{\text{INT/SKP}}$ line low. During IOTA of SKIP instructions the $\overline{\text{INT/SKP}}$ reflects the SENSE FF data when $\overline{\text{DEVSEL}}$ is low and XTC is high. If the SENSE flip flop is set, the $\overline{\text{INT/SKP}}$ line is driven low to cause the HM-6100 to skip the next instruction. All these outputs are open drain.

CONTROL LINES					
$\overline{\text{SKP}}$	**$\overline{\text{C0}}$***	**$\overline{\text{C1}}$**	**$\overline{\text{C2}}$**	**OPERATION**	**DESCRIPTION**
H	H	H	H	PIE ← AC	The contents of the AC is sent to the PIE.
H	H	L	H	AC ← AC V PIE	Data is received from the PIE, OR'ed with the data in the AC and the result stored in the AC.
H	H	L	L	PC ← Vector Address	Vector address received from PIE and loaded into PC. This is referred to as an absolute jump.
L	H	H	H	PC ← PC + 1	Forces Microprocessor to skip next sequential instruction.

NOTE: *The $\overline{\text{C0}}$ line must be connected to V_{CC} using a pull-up resistor.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands.

The format and meaning of control bits are shown below.

FL (1-4) – Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits under software control changes the corresponding FLAG outputs.

IE (1-4) – A high level on INTERRUPT ENABLE enables interrupts for the SENSE inputs.

Otherwise these inputs provide conditional skip testing as defined by the SKIP1-4 instructions.

WP (1-2) – A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2	*	WP1	*	IE4	IE3	IE2	IE1

* = Don't Care

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

SL (1-4) – A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is generated only if a sense line is set up to be edge sensitive and interrupts are enabled via the IE bits of CRA.

SP (1-4) – A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.

0	1	2	3	4	5	6	7	8	9	10	11
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1	*	*	*	*

* = Don't Care

VECTOR REGISTER

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the INTGNT line to a low level. The INTGNT signal is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. Within the PIE, SENSE1 has the highest priority and SENSE 4 has the lowest. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt. If PIN is tied to GND, then the PIE will respond as a non-vectored interrupt device.

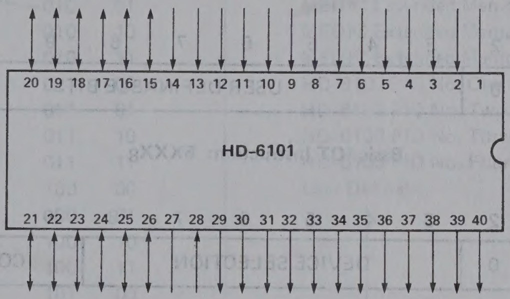
<table>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th><th>8</th><th>9</th><th>10</th><th>11</th></tr>
<tr><td colspan="10">VECTOR REGISTER</td><td colspan="2">VPRI</td></tr>
</table>

VPRI	CONDITIONS
00	SENSE 1
01	SENSE 2
10	SENSE 3
11	SENSE 4

Pin Definitions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V_{CC}		Positive voltage
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes then sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set by an edge.
5	SENSE 3	PROG	See pin 4 – SENSE 4
6	SENSE 2	PROG	See pin 4 – SENSE 4
7	SENSE 1	PROG	See pin 4 – SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	TRUE	See Pin 8 – SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 – SEL 3
12	SEL 6	TRUE	See Pin 8 – SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on $\overline{\text{DEVSEL}}$ initiates a "read" operation. When XTC is low, a low going pulse on $\overline{\text{DEVSEL}}$ initiates a write operation.
14	SEL 7	TRUE	See Pin 8 – SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 – DX 0
17	DX 2	TRUE	See Pin 15 – DX 0
18	DX 3	TRUE	See Pin 15 – DX 0
19	DX 4	TRUE	See Pin 15 – DX 0
20	DX 5	TRUE	See Pin 15 – DX 0



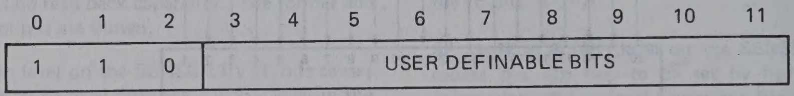
PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 – DX 0
22	DX 7	TRUE	See Pin 15 – DX 0
23	DX 8	TRUE	See Pin 15 – DX 0
24	DX 9	TRUE	See Pin 15 – DX 0
25	DX 10	TRUE	See Pin 15 – DX 0
26	DX 11	TRUE	See Pin 15 – DX 0
27	GND		
28	$\overline{\text{DEVSEL}}$	L	The $\overline{\text{DEVSEL}}$ input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 – FLAG 4
31	FLAG 2	PROG	See Pin 29 – FLAG 4
32	FLAG 1	PROG	See Pin 29 – FLAG 4
33	$\overline{\text{C1}}$	L	The PIE decodes address, control and priority information and asserts outputs $\overline{\text{C1}}$ and $\overline{\text{C2}}$ during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to V_{CC}. $\overline{\text{C1}}$(L), $\overline{\text{C2}}$(L) - vectored interrupt $\overline{\text{C1}}$(L), $\overline{\text{C2}}$(H) - $\overline{\text{READ1}}$, $\overline{\text{READ2}}$ or RRA commands $\overline{\text{C1}}$(H), $\overline{\text{C2}}$(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	$\overline{\text{C2}}$	L	See Pin 33 – $\overline{\text{C1}}$
35	$\overline{\text{READ1}}$	PROG	Outputs $\overline{\text{READ1}}$ and $\overline{\text{READ2}}$ are used to gate data from peripheral devices onto the DX bus for input to the **HM-6100**. Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the **HM-6100** DX bus into peripheral devices. Data does not pass through the PIE.
37	$\overline{\text{READ2}}$	PROG	See Pin 35 – $\overline{\text{READ1}}$
38	WRITE2	PROG	See Pin 36 – WRITE1
39	$\overline{\text{SKP/INT}}$	L	The PIE asserts this line low to generate interrupt requests and to signal the **HM-6100** when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.

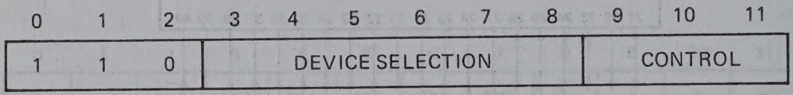
IOT Considerations

The HM-6100 communicates with peripherals via input/output transfers (IOT) instructions. The first three bits, 0-2 are always set to 6_8 (110) to specify an IOT instruction. The next 9 bits, 3-11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permits interfaces with up to 63 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The HD-6102 MEDIC utilizes the PDP-8/E format. When using the HD-6101 PIE and the HD-6103 PIO, bits 3-7 perform the device selection function and bits 8-11 provide the operation specification code.

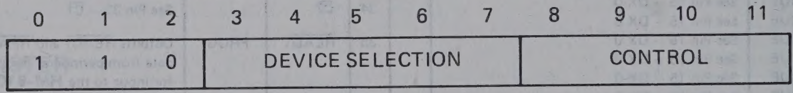
IOT INSTRUCTION FORMAT



Basic IOT Instruction: $6XXX_8$



PDP-8/E Format: $6NNX_8$



PIE and PIO Format

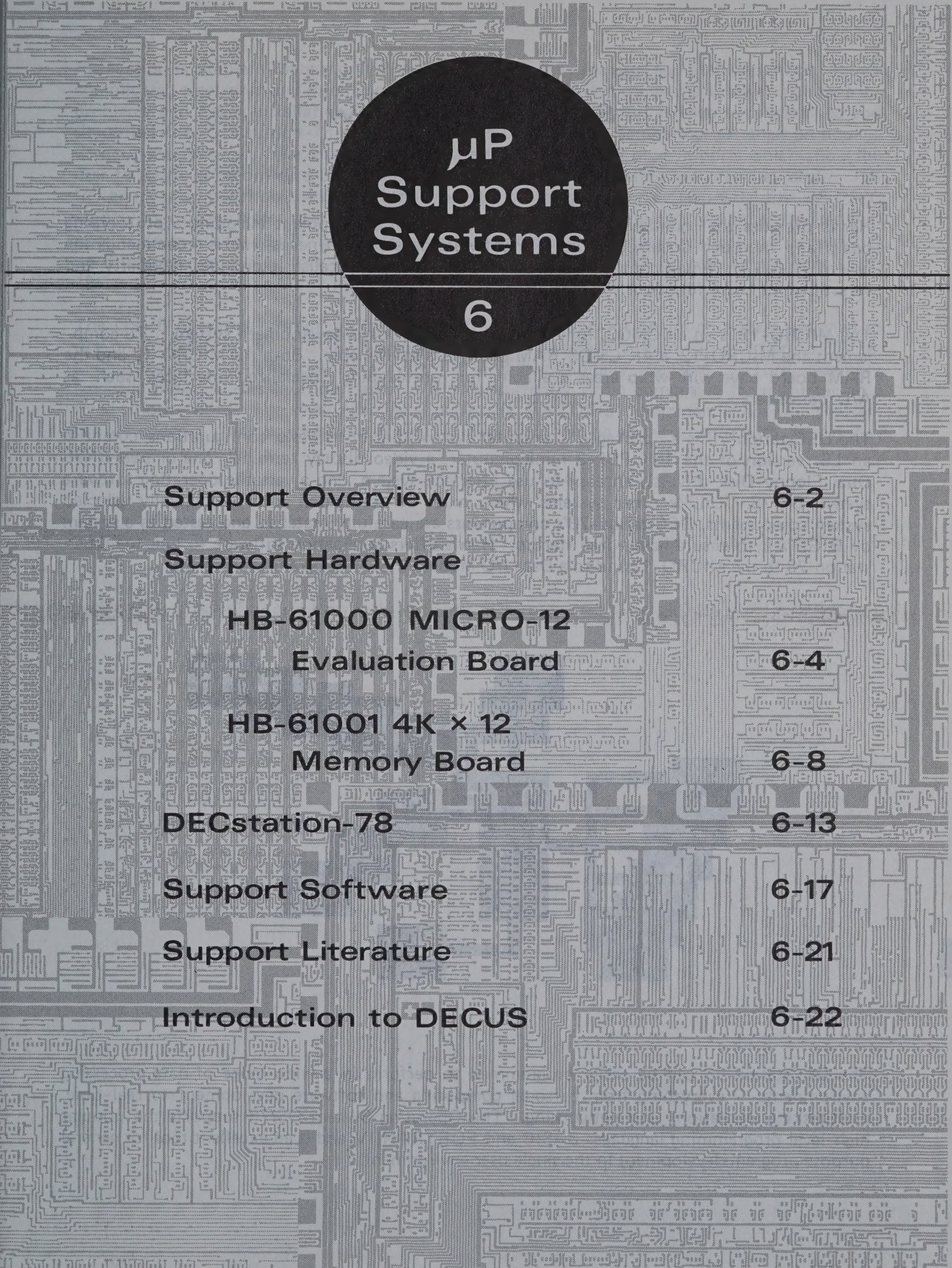
Care must be taken when building a system which uses all three peripheral interface devices from Harris to avoid conflicts with the device selection codes. Care also must be used when utilizing DEC compatible teletype and high speed reader interfaces in a system which includes PIE's and PIO's. The following table will assist in the assignment of device selection codes.

DEVICE SELECTION		
PDP-8/E ①	PIE & PIO ②	DEVICE TYPE
00	000 00	Internal IOT's
01	000 00	DEC High Speed Reader
02	000 01	DEC High Speed Punch
03	000 01	DEC Teletype Keyboard/Reader
04	000 10	DEC Teletype Printer/Punch
05	000 10	User Definable (DEC PDP-8/E Format Only)
06, 07	000 11	User Definable
10, 11	001 00	User Definable
12	001 01	User Definable (DEC PDP-8/E Format Only)
13	001 01	MEDIC Real Time Clock
14, 15	001 10	User Definable
16, 17	001 11	User Definable
20, 21	010 00	MEDIC Extended Memory Control and DMA
22, 23	010 01	MEDIC Extended Memory Control and DMA
24, 25	010 10	MEDIC Extended Memory Control and DMA
26, 27	010 11	MEDIC Extended Memory Control and DMA
30, 31	011 00	HD-6103 PIO No. One
32, 33	011 01	HD-6103 PIO No. Two
34, 35	011 10	HD-6103 PIO No. Three
36, 37	011 11	HD-6103 PIO No. Four
40, 41	100 00	User Definable
42, 43	100 01	
44, 45	100 10	
46, 47	100 11	
50, 51	101 00	
52, 53	101 01	
54, 55	101 10	
56, 57	101 11	
60, 61	110 00	
62, 63	110 01	
64, 65	110 10	
66, 67	110 11	(DEC Line Printer = 66)
70, 71	111 00	
72, 73	111 01	
74, 75	111 10	(DEC Floppy Disk Drive = 75)
76, 77	111 11	User Definable

NOTES:

① PDP-8/E device selection in octal.

② PIE & PIO device selection in binary.



µP Support Systems

6

Support Overview 6-2

Support Hardware

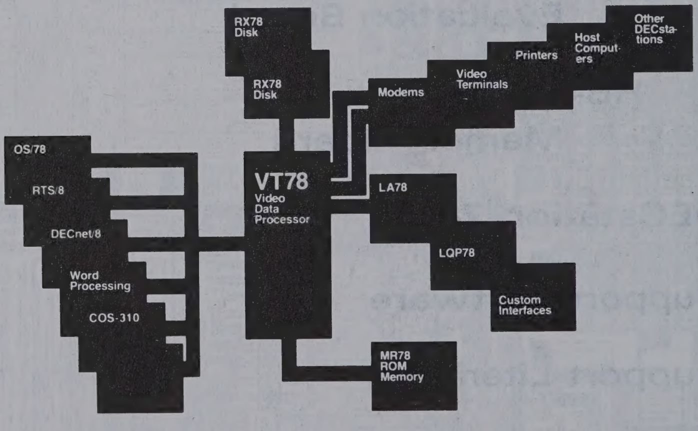
HB-61000 MICRO-12 Evaluation Board 6-4
HB-61001 4K × 12 Memory Board 6-8
DECstation-78 6-13
Support Software 6-17
Support Literature 6-21
Introduction to DECUS 6-22

Support Overview

Harris provides the foundation tools needed for system development including a prototyping board and thorough documentation. For software development needs, Harris recommends the use of DIGITAL Equipment Corporation's DECstation-78 because it provides flexibility and versatility for many functions.

The MICRO-12 is an all CMOS, fully assembled, single board development system. To complement the MICRO-12, a 4K CMOS RAM board is also available. Both the MICRO-12 and the RAM board have wire-wrap areas available for prototyping specialized interfaces such as A/D converters.

The DECstation-78 is a "packaged" computer system that in its basic configurations comprise an LSI version of the 16K PDP-8 minicomputer, a video display terminal, one or two RX78 Dual Floppy Disk drive(s), an easy-to-use interface system, and a versatile operating software system OS/78. Unlike other systems which must be configured from individually selected system components, DECstation-78's components are carefully matched and tested as a system by DIGITAL to ensure hassle-free startup. Harris offers application software to link the DECstation-78 to the MICRO-12 and to a Data I/O Model 9 PROM Programmer.


RX78 Disk
RX78 Disk
Modems
Video Terminals
Printers
Host Computers
Other DECstations
OS/78
RTS/8
DECnet/8
Word Processing
COS-310
VT78 Video Data Processor
LA78
LQP78
Custom Interfaces
MR78 ROM Memory

The DECstation-78 can be easily programmed to perform in a wide range of data processing enviromnents — everything from personal computing and software development to real-time, multitasking operations and networking. The Operating System OS/78 supports the popular high-level programming languages BASIC and FORTRAN IV and is an excellent tool for general purpose program development in the single user environment.

Installation is simple. There is only one cable between the processor and each peripheral. Fewer complicated electronic and mechanical parts and interconnection cables mean fewer maintenance problems and easier installation. In fact, system interconnection has been so streamlined and simplified that DECstation-78 can be installed by the user in something less than an hour — without special tools. The interconnections are through external plug-in ports which allow the user to adapt or reconfigure DECstation-78 to handle new processing needs as they occur. The I/O connection panel on the back of the processor contains five ports. Two serial EIA RS-232C asynchronous interface ports are suitable for interfacing with terminals and other devices that operate from 50 to 19,200 baud. One port is equipped for modem control. A parallel I/O port for printers and custom interfacing provides bi-directional 12-bit transfers at rates up to 15K words per second. A disk interface port allows connection to RX78 Floppy Disks.

The OS/78 operating system is a complete software development operating system designed to run on DECstation 78. OS/78 is supplied as part of the basic system. In addition to OS/78, a multitasking real-time operating system RTS/8 is optionally available. RTS/8, assembly language based, allows multiple tasks to run concurrently while competing for resources on a fixed priority basis. For small business applications, the COS-310 commercial operating system can be added. Word processing software, WPS-8, can also be added to help with your documentation requirements.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HB-61000
MICRO-12

Features

- **COMPLETE SINGLE BOARD CMOS MICROCOMPUTER SYSTEM**
- **INCLUDES CPU, MEMORY, UART AND I/O**
- **HIGH PERFORMANCE CMOS 12 BIT CPU**
- **WIDELY USED PDP-8* INSTRUCTION SET**
- **INTERFACES DIRECTLY WITH TTY/CRT TERMINAL/ TAPE CASSETTE**
- **INTERACTIVE KEYBOARD & DISPLAY**
- **USER WIREWRAP AREA**
- **EXTENSIVE CONTROL PANEL MONITOR IN ROM**
- **LARGE USER SOFTWARE LIBRARY AVAILABLE**
- **SMALL 5V POWER SUPPLY INCLUDED.**

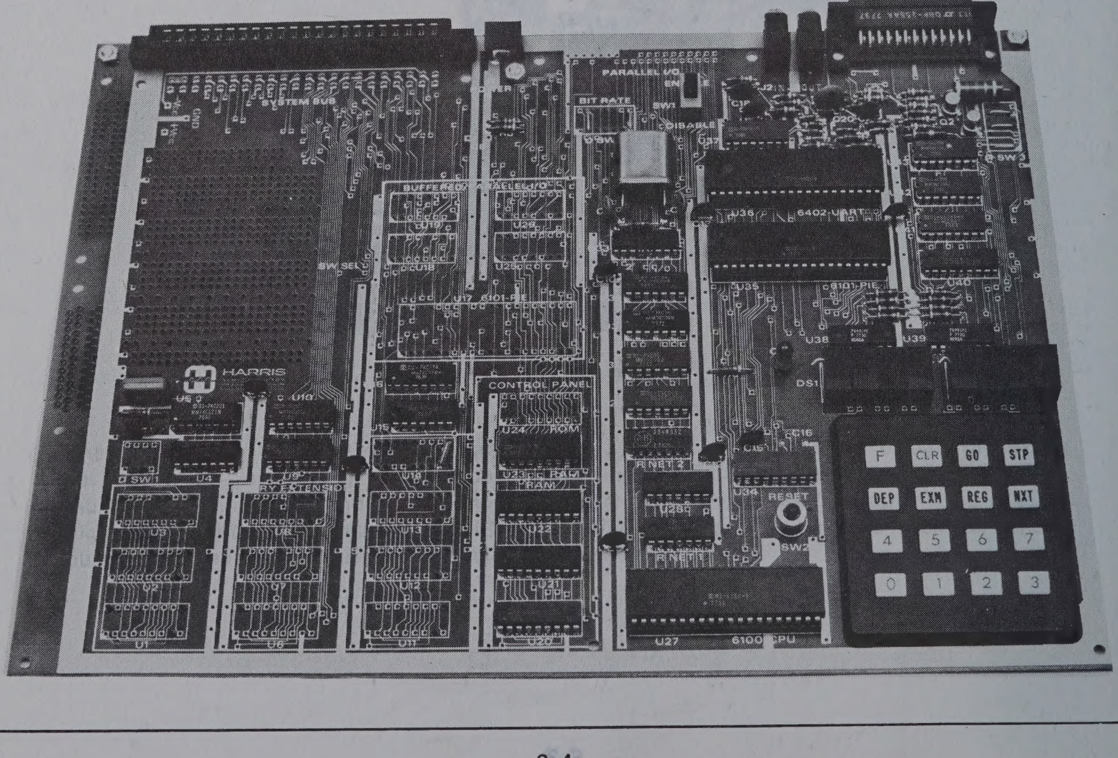
* Trademark of Digital Equipment Corp., Maynard, Ma.

Description

The Harris MICRO-12 is a fully assembled and tested single board CMOS 12 bit microprocessor system. A preprogrammed ROM provides a system monitor, keyboard and display utilities and system diagnostic capabilities.

The MICRO-12 includes an 8 digit LED display and 16 key-keyboard which allows direct program insertion, execution and examination.

The ROM system monitor also provides a Binary Loader and List capability from a TTY. A Kansas City Standard Tape Cassette interface (300 Baud) provides the user with a simple means of loading and storing programs.


SYSTEM BUS
PARALLEL I/O
BIT RATE
6402 UART
6101-PIE
CONTROL PANEL
ROM
RAM
RESET
6100 CPU
HARRIS
F
CLR
GO
STP
DEP
EXM
REG
NXT
4
5
6
7
0
1
2
3

System Description

The MICRO-12 is a fully assembled and tested 12 bit CMOS microprocessor system. It is compact (8.4" x 11.6") and provides a full compliment of CMOS system components. A system monitor ROM (1K x 12) allows the user to enter his program manually with a 16 key keyboard or through a TTY or tape cassette by using the Binary Loader feature. A standard program memory of 256 words x 12 bit RAM is provided with optional socket space for a full 1K x 12 program memory. The monitor does not use any of the user program memory.

The system monitor provides the user with four (4) independent breakpoints for program debug. An 8 digit display allows inspection of the address, memory and register data.

A special function key allows the user program to be listed on either an external TTY or CRT. Another special function key allows the user to punch a program tape on the TTY. The Binary Punch feature may also be used to load an external tape cassette from program memory. A 300 baud Kansas City Standard interface is provided for this purpose. Communications rate of 50 to 9600 baud are jumper selectable on the Bit Rate Generator through the Universal Asynchronous Receiver Transmitter (UART).

KEYBOARD MONITOR COMMANDS:

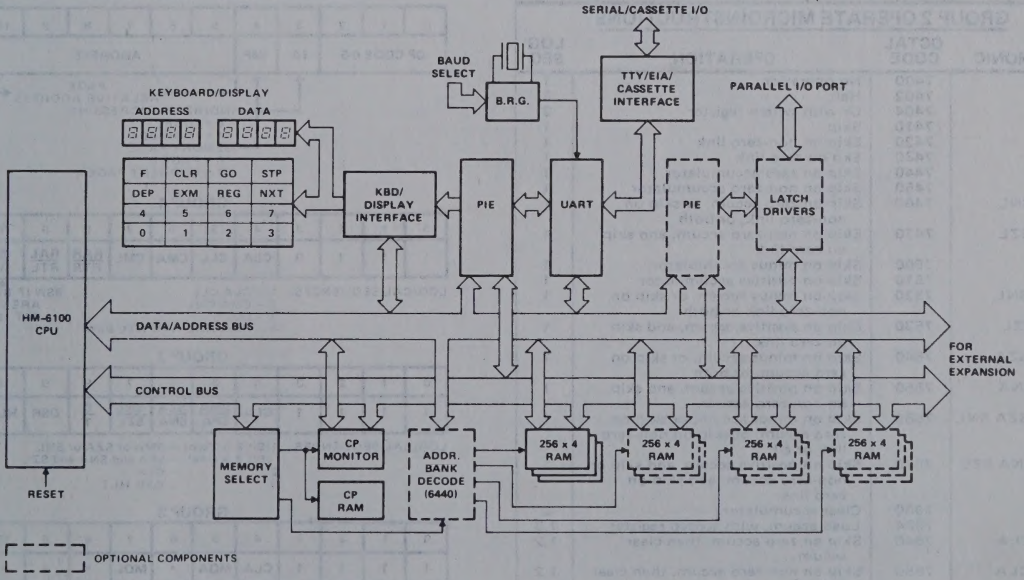
- **EXAMINE** – Allow user to inspect memory data at keyed in address.
- **DEPOSIT** – Alters data at data address.
- **REGISTER EXAMINE** – Allows the user to examine PC, AC, MQ & LINK.
- **NEXT (INSTRUCTION)** – Increments present address.
- **EXECUTE** – Allows the user program to be executed.
- **SINGLE CYCLE** – Allows program to execute single instruction at a time.
- **FUNCTION** – Causes entry to be second function routines.
- **CLEAR** – Clears accumulator, MQ registers, LINK, and Breakpoints (P.C. address is set to 7777).

FUNCTION COMMANDS:

- **BINARY LOAD** – Allows TTY reader or cassette entry of user program.
- **BINARY PUNCH** – Allows TTY punching or cassette loading of users program.
- **OCTAL LISTING** – Allows TTY printing of user program.
- **BREAKPOINT SET** – Examine/alter any of four software breakpoints.

Documentation package includes detailed information on using the control panel, how the system operates and users manual which contains circuit diagrams and a listing of the control panel program. Several hardware and software examples are included. The Micro-12 User Manual can be ordered from Harris for more detailed information.

Functional Block Diagram


SERIAL/CASSETTE I/O
BAUD SELECT
B.R.G.
TTY/EIA/ CASSETTE INTERFACE
PARALLEL I/O PORT
KEYBOARD/DISPLAY
ADDRESS
DATA
F
CLR
GO
STP
DEP
EXM
REG
NXT
4
5
6
7
0
1
2
3
KBD/ DISPLAY INTERFACE
PIE
UART
PIE
LATCH DRIVERS
HM-6100 CPU
DATA/ADDRESS BUS
CONTROL BUS
FOR EXTERNAL EXPANSION
RESET
MEMORY SELECT
CP MONITOR
CP RAM
ADDR. BANK DECODE (6440)
256 x 4 RAM
256 x 4 RAM
256 x 4 RAM
256 x 4 RAM
OPTIONAL COMPONENTS

HM-6100 Microprocessor

The HM-6100 CMOS Microprocessor is a single address, fixed word length, parallel transfer 12 bit microprocessor. It is a member of a broad based CMOS product line which comprises 6100 peripheral devices, RAMs, PROMs, ROMS and a full logic family. The processor recognizes the PDP-8* instruction set and utilizes two's complement arithmetic logic. The device is completely static and may be operated from DC to its rated frequency. No external clock generators or controllers are required.

The support chips, Peripheral Interface Element (PIE), Universal Asynchronous Receiver Transmitter (UART), Bit Rate Generator, Read Only Memories (ROM), Random Access Memories (RAM) and Programmable Read Only Memories (PROM) are completely compatible with the microprocessor. All devices are available in either an industrial or a military temperature range.

* Trademark of Digital Equipment Corp., Maynard Ma.

Table of Instruction Set

BASIC INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
AND	0XXX	Logical AND
TAD	1XXX	Binary ADD
ISZ	2XXX	Increment, and skip if zero
DCA	3XXX	Deposit and clear AC
JMS	4XXX	Jump to subroutine
JMP	5XXX	Jump
IOT	6XXX	In/out transfer
OPR	7XXX	Operate

GROUP 1 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7000	No operation	1
IAC	7001	Increment accumulator	3
RAL	7004	Rotate accumulator left	4
RTL	7006	Rotate two left	4
RAR	7010	Rotate accumulator right	4
RTR	7012	Rotate two right	4
BSW	7002	Byte swap	4
CML	7020	Complement link	2
CMA	7040	Complement accumulator	2
CIA	7041	Complement and increment accum.	2,3
CLL	7100	Clear link	1
CLL RAL	7104	Clear link-rotate accum. left	1,4
CLL RTL	7106	Clear link-rotate two left	1,4
CLL RAR	7110	Clear link-rotate accum. right	1,4
CLL RTR	7112	Clear link-rotate two right	1,4
STL	7120	Set the link	1,2
CLA	7200	Clear accumulator	1
CLA IAC	7201	Clear accum. -increment accum.	1,3
GLK	7204	Get the link	1,4
CLA CLL	7300	Clear accumulator-clear link	1
STA	7240	Set the accumulator	1,2

GROUP 2 OPERATE MICROINSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7400	No operation	1
HLT	7402	Halt	3
OSR	7404	Or with switch register	3
SKP	7410	Skip	1
SNL	7420	Skip on non-zero link	1
SZL	7430	Skp on zero link	1
SZA	7440	Skip on zero accumulator	1
SNA	7450	Skip on non-zero accumulator	1
SZA SNL	7460	Skip on zero accum, or skip on non-zero link, or both	1
SNA SZL	7470	Skip on non-zero accum. and skip on zero link	1
SMA	7500	Skip on minus accumulator	1
SPA	7510	Skip on positive accumulator	1
SMA SNL	7520	Skip on minus accum. or skip on non-zero link or both	1
SPA SZL	7530	Skip on positive accum. and skip on zero link	1
SMA SZA	7540	Skip on minus accum. or skip on zero accum. or both	1
SPA SNA	7550	Skip on positive accum. and skip on non-zero accum.	1
SMA SZA SNL	7560	Skip on minus accum. or skip on zero accum. or skip on non-zero link or all	1
SPA SNA SZL	7570	Skip on positive accum. and skip on non-zero accum. and skip on zero link	1
CLA	7600	Clear accumulator	2
LAS	7604	Load accum. with switch register	1,3
SZA CLA	7640	Skip on zero accum. then clear accum.	1,2
SNA CLA	7650	Skip on non-zero accum. then clear accum.	1,2
SMA CLA	7700	Skip on minus accum. then clear accum.	1,2
SPA CLA	7710	Skip on positive accum. then clear accum.	1,2

GROUP 3 OPERATE MICROINSTRUCTIONS

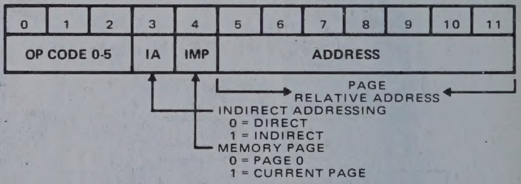
MNEMONIC	OCTAL CODE	OPERATION	LOG SEQ
NOP	7401	No operation	3
MQL	7421	MQ register load	2
MQA	7501	MQ register into accumulator	2
SWP	7521	Swap accum. and MQ register	3
CLA	7601	Clear accumulator	1
CAM	7621	Clear accum. and MQ register	3
ACL	7701	Clear accum. and load MQ register into accumulator	3
CLA SWP	7721	Clear accum. and swap accum. and MQ register	3

PROCESSOR IOT INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
SKON	6000	Skip if interruption on
ION	6001	Interrupt turn on
IOF	6002	Interrupt turn off
SRQ	6003	Skip if INT request
GTF	6004	Get flags
RTF	6005	Return flags
SGT	6006	Operation is determined by external devices if any
CAF	6007	Clear all flags

Bit Assignments

MEMORY REFERENCE INSTRUCTION FORMAT



GROUP 1

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	RAR RTR	RAL RTL	0 1	IAC

LOGICAL SEQUENCES:
1 – CLA CLL
2 – CMA CML
3 – IAC
4 – RAR RAL RTR RTL BSW

BSW IF BITS 8 & 9 ARE 0 AND BIT 10 IS 1

GROUP 2

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA SPA	SZA SNA	SNL SZL	0 1	OSR	HLT	0

LOGICAL SEQUENCES:
1 (Bit 8 is Zero) – SMA or SZA or SNL
(Bit 8 is One) – SPA and SNA and SZL
2 – CLA
3 – OSR HLT

GROUP 3

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

LOGICAL SEQUENCES:
1 – CLA
2 – MQA MQL
3 – ALL OTHERS

* DON'T CARE

Specifications

CENTRAL PROCESSOR

HM-6100

- Crystal Controlled 2.45MHz
- Single Power Supply . . . . +5 Volts
- CMOS . . . . TTL Compatible

MEMORY

ROM — 1K x 12 Bits Monitor (Resident in control panel memory does not use user address space.)

RAM — 256 x 12 Bits (Expandable to 1K words.)

INTERFACES

SERIAL I/O:	20mA Current Loop TTY RS-232 (Jumper Selectable) Baud Rate 50 thru 9600 (Jumper Selectable)
BUS:	CMOS Compatible (Dual 22 Pin Connector Provided)
PARALLEL I/O:	12 Bit Input (Optional) 12 Bit Output (Optional) Large User Wirewrap Area Provided for Additional I/O

SOFTWARE

System monitor provided in ROM with resident keyboard, display and serial output control. Allows user to load, dump and display programs.

LITERATURE (Provided with Micro-12)

- Micro-12 User Manual
- Microprocessor Systems Design Manual
- Introduction to Programming
- Assembly Language Reference Card
- Introduction to DECUS

PHYSICAL CHARACTERISTICS

- Height . . . . 8.4 Inches
- Width . . . . 11.6 Inches
- Depth . . . . 0.75 Inches
- Weight. . . . . 14 Oz.

ELECTRICAL CHARACTERISTICS

- V_{CC} = ...(+)5 Volts ±10%
- V_{TTY} = ... (–) 12 Volts ±20%, 30mA (Req. only if TTY is connected.)
- I_{CC} = ...40mA (System), 160mA (Display)

OPTIONS:

- 1K Memory
- 4K Memory
- Parallel I/O
- Downloader Software

HB-61001
CMOS MEMORY BOARD

Features

- SINGLE SUPPLY, 5V
- ALL CMOS SYSTEM, HIGH NOISE IMMUNITY
- LOW POWER, < 12mW MAXIMUM STANDBY
- DATA RETENTION @ 2 VOLTS
- BUS COMPATIBLE WITH HB-61000 MICROCOMPUTER BOARD
- 4096 x 12 RAM
- 2048 x 12 OPTION – ADDRESS SELECTABLE

Description

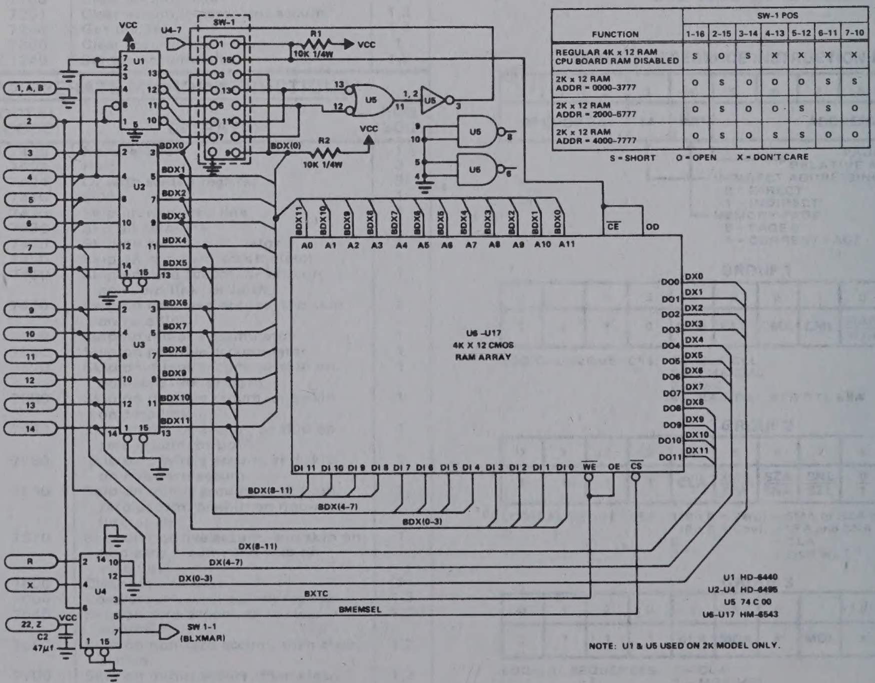
The HB-61001 is a fully assembled and tested all-CMOS memory board, designed to interface directly with the HB-61000 (MICRO-12) single board computer.

The board uses Harris' high performance HM-6543 fully static CMOS RAM's. The HB-61001 comes with either 4K x 12 or 2K x 12 organizations with address selectable by jumper options.

Interfacing the board to other systems is extremely easy, only three (3) control signals and a 12-bit multiplexed address/data bus are needed. See bus signals definition for details. There is no field control logic for extended memory.

A wire wrap area (1.7 x 4″^{2}) with .1″ center holes are provided on the board for custom interface circuitrys, battery back-up circuitry, etc.

Functional Block Diagram


VCC
U1
U4-7
SW-1
R1
10K 1/4W
VCC
U5
1, 2
U5
1, A, B
2
3
4
5
6
7
8
9
10
11
12
13
14
R
X
22, Z
C2
47µf
U2
U3
U4
BDX0
BDX1
BDX2
BDX3
BDX4
BDX5
BDX6
BDX7
BDX8
BDX9
BDX10
BDX11
BDX(0)
R2
10K 1/4W
CE
OD
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
U6 -U17
4K X 12 CMOS
RAM ARRAY
DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8 DO9 DO10 DO11
DX0 DX1 DX2 DX3 DX4 DX5 DX6 DX7 DX8 DX9 DX10 DX11
DI 11 DI 10 DI 9 DI 8 DI 7 DI 6 DI 5 DI 4 DI 3 DI 2 DI 1 DI 0 WE OE CS
BDX(8-11)
BDX(4-7)
BDX(0-3)
DX(8-11)
DX(4-7)
DX(0-3)
BXTC
BMEMSEL
SW 1-1
(BLXMAR)

FUNCTION	SW-1 POS 1-16	2-15	3-14	4-13	5-12	6-11	7-10
REGULAR 4K x 12 RAM CPU BOARD RAM DISABLED	S	O	S	X	X	X	X
2K x 12 RAM ADDR = 0000-3777	O	S	O	O	O	S	S
2K x 12 RAM ADDR = 2000-6777	O	S	O	O	S	S	O
2K x 12 RAM ADDR = 4000-7777	O	S	O	S	S	O	O

S = SHORT O = OPEN X = DON'T CARE

U1 HD-6440
U2-U4 HD-6495
U5 74 C 00
U6-U17 HM-6543

NOTE: U1 & U5 USED ON 2K MODEL ONLY.

Specifications HB-61001

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage	(VCC - GND) -0.3V to +8.0V	Operating Supply Voltage	4.5V to 5.5V
Applied Input or Output Voltage	(GND -0.3V) to (VCC +0.3V)	Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +100°C	Physical Characteristics	4.5″ x 7.0″ x .6″ Weight: 5 oz.

ELECTRICAL CHARACTERISTICS

VCC = 5V ±10% TA = Operating Range

	SYMBOL	PARAMETER	HB-61001-1		HB-61001-2		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
D.C.	ICCSB	Standby Supply Current		1.0		1.0	mA	VI = VCC or GND IO = HIZ
	ICCOP	Operating Supply Current ①		15		15	mA	f = 125kHz
	VCCDR	Data Retention Supply Voltage	2.0		2.0		V	
	ICCDR	Data Retention Supply Current		1.0		1.0	mA	VCC = 3.0 VI = VCC or GND
	VIH	Input High Voltage	70% VCC	VCC +0.3	70% VCC	VCC +0.3	V	
	VIL	Input Low Voltage	GND -0.3	20% VCC	GND -0.3	20% VCC	V	
	VOH	Output High Voltage	2.4		2.4		V	IOH = -2.0mA
	VOL	Output Low Voltage		0.4		0.4	V	IOL = 2.0mA
	II	Input Leakage Current	-1.0	+1.0	-1.0	+1.0	µA	GND ⩽ VI ⩾ VCC
	IOZ	Output Leakage Current	-20	+20	-20	+20	µA	GND ⩽ VO ⩾ VCC
	CI	Input Capacitance ②		15		15	pF	f = 1MHz I/O = HIZ
	CI/O	Input/Output Capacitance ②		30		30	pF	
A.C.	TAS	Address Set Up Time	25		25		ns	③
	TAH	Address Hold Time	75		165		ns	
	TLX	LXMAR Pulse Width (Positive)	200		200		ns	
	$\overline{\text{TLX}}$	LXMAR Pulse Width (Negative)	450		575		ns	
	TAL	Access Time from LXMAR		450		575	ns	
	TCY	Read or Write Cycle Time	650		775		ns	
	TEN	Output Enable Time		250		250	ns	
	TDIS	Output Disable Time		150		150	ns	
	TDS	Write Data Set Up Time	130		130		ns	
	TDH	Write Data Hold Time	50		50		ns	
	TWP	Write Pulse Width	220		220		ns	

NOTES:

① Operating current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP 80mA/MHz.

② Capacitance sampled and guaranteed but not 100% tested.

③ AC test conditions: Inputs TRISE = TFALL ⩽ 100ns; Outputs — CLOAD =: and 100pF.

Timing Diagrams

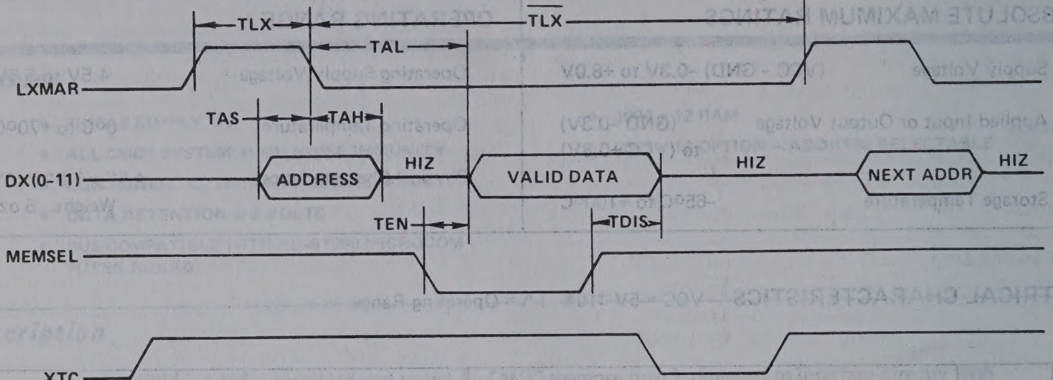

TLX
$\overline{TLX}$
TAL
LXMAR
TAS
TAH
DX(0-11)
ADDRESS
HIZ
VALID DATA
HIZ
NEXT ADDR
HIZ
TEN
TDIS
MEMSEL
XTC

FIGURE 1-1 – Read Cycle Timing

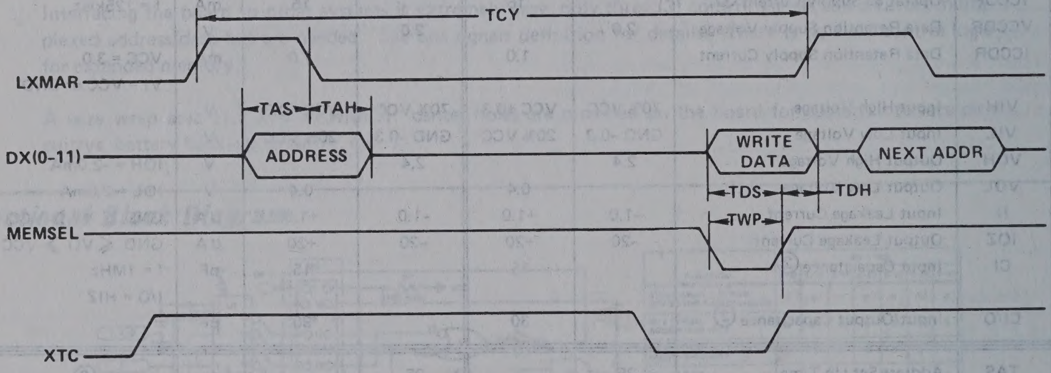

TCY
LXMAR
TAS
TAH
DX(0-11)
ADDRESS
WRITE DATA
NEXT ADDR
TDS
TDH
TWP
MEMSEL
XTC

FIGURE 1-2 – Write Cycle Timing

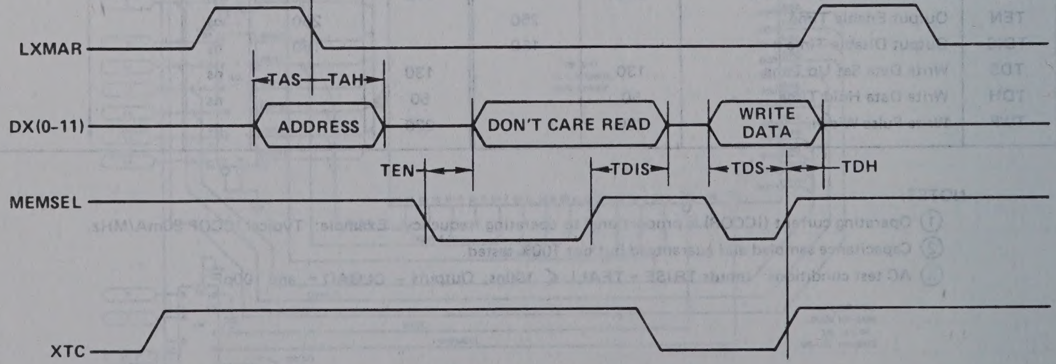

LXMAR
TAS
TAH
DX(0-11)
ADDRESS
DON'T CARE READ
WRITE DATA
TEN
TDIS
TDS
TDH
MEMSEL
XTC

FIGURE 1-3 – MICRO-12 Compatible Timing Read Modify Write Cycle

Installing the HB-61001 in the MICRO-12

BASIC INSTALLATION

To install the HB-61001 memory board in the MICRO-12, first determine the amount of RAM that exists on the CPU board.

If there are 256 words of onboard RAM, and no HD-6440 in U14, installing the HB-61001 is accomplished by removing the jumper from pin 8 to 10 of U14 on the MICRO-12 and replacing it with a jumper from pin 10 to pin 6 of U14. Next plug the memory board into the edge connector with the components facing the keypad.

If there are more than 256 words of RAM and a HD-6440 in U14 on the MICRO-12 replace the jumper from pin 2 to 7 of DSW-1 on the MICRO-12 with one from pin 8 to ground of DSW-1 and plug in the memory board.

SPECIAL HINTS FOR 2K VERSION USERS

It is possible for users of the 2K version (HB-61001-2) to actually have up to 3K of useable read write memory. This is accomplished by utilizing both the MICRO-12 onboard memory and the external memory board. Setting the HB-61001 memory board to reside at locations 2000-5777 octal and leaving the MICRO-12 memory enabled allows the use of all available memory. See the truth table on the first page for details on setting the address of the HB-61001-2. Refer to the MICRO-12 manual, page A-61 for details of the onboard memory circuits.

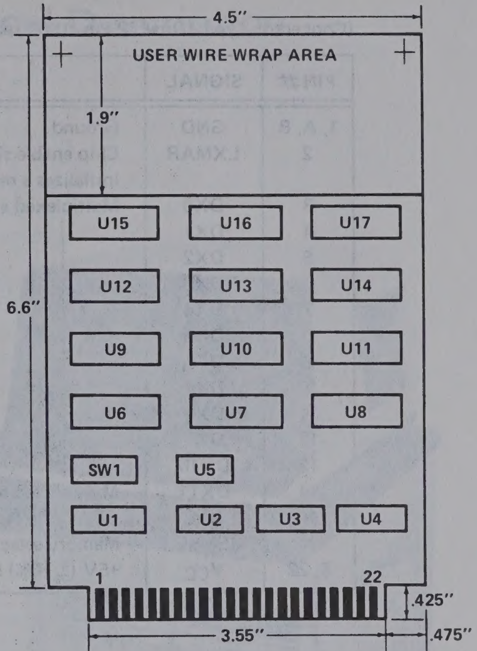


FIGURE 2 – HB-61001 Dimensions

Battery Back-Up

In many applications it is desireable to provide for data retention during power interruptions. The circuit shown in Figure 3 will provide power to the memory during power outages and doubles as a battery charging circuit during normal operation.

In addition to providing a standby supply, the user must take precautions to guarantee that none of the CMOS inputs are left floating during the power outage. The easiest way to accomplish this, is to add 100K pull-down resistors from all board inputs to CMOS VCC.

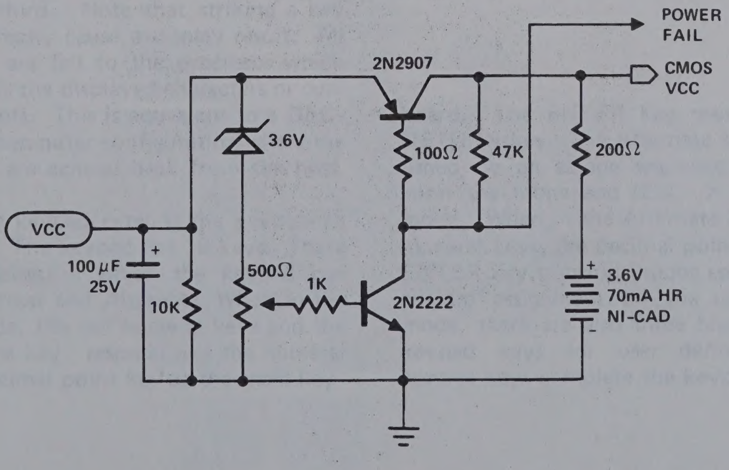


FIGURE 3 – A Typical Battery Back-Up Circuit

Bus Signal Definitions

(Connector Type: Dual 22 Pin .156" spacing)

PIN #	SIGNAL	DESCRIPTION
1, A, B	GND	Ground
2	LXMAR	Chip enable signal; the negative going edge latches address in RAM and initializes a memory cycle.
3	DX0	Multiplexed address/data bus, most significant bit.
4	DX1	
5	DX2	
6	DX3	
7	DX4	
8	DX5	
9	DX6	
10	DX7	
11	DX8	
12	DX9	
13	DX10	
14	DX11	Multiplexed address/data bus, least significant bit.
R	XTC	READ/$\overline{\text{WRITE}}$ control signal (READ = High, WRITE = Low)
X	MEMSEL	Memory select, active low.
Z, 22	V_{CC}	+5V (± 10%) Supply

DECstation-78 Technical Description

In DECstation-78 the computer and terminal are a single compact unit, designated as a VT78 Video Data Processor. The processor and display are interconnected over a high-speed serial line with the processor physically located inside the video display's case. A single START switch activates the entire system. At system power-up, the display and keyboard are automatically tested.

VIDEO DISPLAY AND KEYBOARD

The keyboard/video display is basically a DECscope in origin but has some added features to tailor it to DECstation-78. The same clarity of displayed characters, adjustability of screen intensity, and glare-free screen popular in DECscope products are carried over in DECstation-78. The display system includes a 24-line by 80 character screen format, the complete ASCII upper and lower character set, 33 special symbols, and nineteen user-defined special function keys.

The keyboard is standard typewriter (ANSII) and produces a key-stroke click for audible feedback of key operation. Three-key rollover protection eliminates fast typing errors. Should three keys be depressed simultaneously, transmission will still be correct if one of the first two key typed is released before the third. Note that striking a key does not directly cause a display result. All instructions are fed to the processor which then controls the displayed characters or cursor movements. This is equivalent to a DECscope-Host computer configuration where the instructions are echoed back from the host.

An auxiliary keypad extends the keyboard's capabilities. The keypad has 19 keys. There are two modes in which the keypad can operate, Normal and Alternate. When in the Normal Mode, the ten numeral keys and the decimal point key, respond like the numeral keys and decimal point key on the main keyboard. The ENTER key responds like the RETURN key. The Alternate Mode is established by an escape sequence (ESC =) to enter the mode and (ESC >) to exit the mode. When in the Alternate Mode, the ten numeral keys, the decimal point key, and the ENTER key transmit unique escape codes for custom assignment by the user. In either mode, there are also three blank unassigned keypad keys for user definition. Cursor control keys complete the keypad's function.

PROCESSOR

The overall organization of DECstation-78 is shown in the Figure below. An LSI (large scale integration) version of the powerful PDP-8 minicomputer contained on a 15 3/4" x 11 7/8" printed circuit board is mounted inside of DECstation-78's video display unit. This is the processor for the system. It includes a 12-bit CPU with memory extension control, 16,384 words (32 bytes) of Random Access Memory, complete peripheral interfacing, internal bootstrap facilities, and a 100Hz real-time clock. The CPU has the same powerful instruction set as the PDP-8A. Cycle time is approximately 3.6 microseconds.

Three general purpose processor registers are provided:

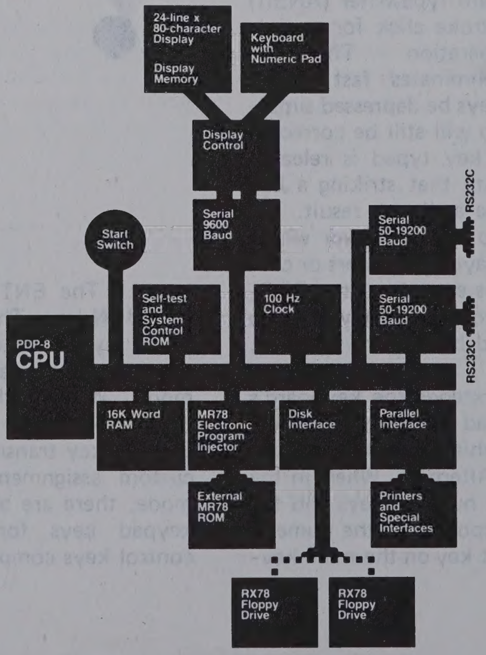
- PC. The 12-bit program counter points to the location from which the next instruction will be fetched.
- AC, L. The 12-bit accumulator and its 1-bit carry extension, the Link, form the register where all arithemtic calculations take place.
- MQ. The 12-bit Multiplier Quotient register serves as a temporary storage register.

Memory

Main memory is 12-bits by 16K words of Random Access NMOS Memory organized as 4 fields of 4K words each. Each field consists of 32 pages of 128 words.

An on-board ROM permits several important features to be included. These are:

- Automatic self-test procedure.
  Processor status display.
- Terminal emulation mode, which alllows DECstation-78 to be used as a stand alone computer terminal without independent processing capability.
- Internal disk bootstrap.
  Preselection of baud rates on primary communications port.


24-line x 80-character Display
Display Memory
Keyboard with Numeric Pad
Display Control
Serial 9600 Baud
Start Switch
Serial 50-19200 Baud
RS232C
Serial 50-19200 Baud
RS232C
Self-test and System Control ROM
100 Hz Clock
PDP-8 CPU
16K Word RAM
MR78 Electronic Program Injector
Disk Interface
Parallel Interface
External MR78 ROM
Printers and Special Interfaces
RX78 Floppy Drive
RX78 Floppy Drive

Instructions

There are two basic groups of instructions: memory reference and microinstructions. Memory reference instructions require an operand; microinstructions do not. The DECstation-78 processor features indirect addressing capability up to 4K and 8 auto-index registers. Three groups of operate microinstructions perform a variety of program operations without any need for reference to memory location. Groups 1 and 2 allow the programmer to manipulate and/or test the data that is located in the accumulator or link. Group 3 operate instructions allow the programmer to manipulate the MQ register. Many of these operate microinstructions may be combined by the experienced programmer in order to use the DECstation-78 processor more efficiently.

Input/Output (IOT) instructions are used to control the operation of the computer's interrupt system and clock and to make all exchanges of data to the system display, keyboard, and externally connected peripherals.

Interface Ports

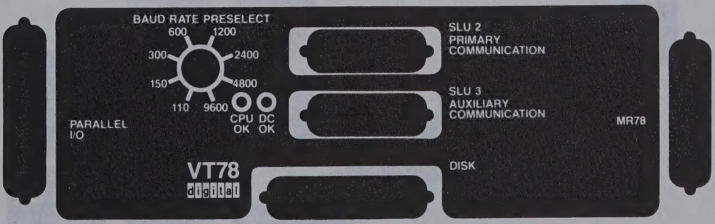
There are six interface ports for DECstation-78: a parallel port, a disk interface port, a electronic program injection port and three asynchronous serial ports.

Parallel I/O Port — is for printers and custom interfacing. It provides bi-directional 12-bit transfers at rates up to 15K words per second.

Serial Line Unit-1 (SLU-1) — connects the central processor to the display subsystem internally and is not externally accessible. The two other asynchronous serial EIA RS-232C interface ports are suitable for primary and secondary communications applications, terminals, and the attachment of a variety of devices. These ports (SLU-2 and SLU-3) features 16 program selectable baud rates ranging from 50 to 19,200 baud and programmable loopback for maintenance. One port, SLU-3, provides programmable parity generation and overrun detection, variable width stop-bit selection and programmable character length. The other port, SLU-2, is equipped for full modem control.

Disk Interface Port — allows connection between the DECstation-78 processor and two independent dual drive disk units (RX78). It provides both 8- and 12-bit data formats for maximum flexibility.

MR78 Electronic Program Injection Port — allows the mounting of an external Read Only Memory program capsule. The MR78 provides high speed loading under control of a preprogrammed ROM unit. Loading is automatically initiated when the DECstation-78 START button is pressed.



RX78 FLOPPY DISK DRIVE

The RX78 Floppy Disk System is an inexpensive mass storage subsystem, I/O and random access file device characterized by speed and reliability. Either one or two compact, self-contained units may be interfaced with the processor via a high-speed data port on the external connector panel.

Track-to-track moves require six milliseconds for the move plus twenty milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360-rpm, with an average latency time of 83 milliseconds. The total average access time is only 263 milliseconds.

The RX78 Floppy Disk System uses IBM-standard diskettes — thin, flexible oxide-coated disks about the size of a 45-rpm phonograph record. The disk is recorded only on one side and is permanently contained in an 8-inch square flexible protective envelope. The diskette contains 77 tracks with 26 sectors per track. Each sector can store 256 8-bit bytes or 128 12-bit words for a total formatted capacity of 512,512 bytes or 256,256 words. The diskette is a portable, convenient storage, interchange and software distribution medium which allows DECstation-78 users to store large amounts of data in a small space.

PRINTERS

For local on-site output, the LA78 DECprinter-1 180-cps line printer is recommended. This printer interfaces via a parallel port on DECstation-78. For word processing applications, the LQP78 letter quality printer is available.

Support Software

Harris supports its microprocessor-based systems through an extensive variety of proven PDP-8 software. For the DECstation-78, there are three major operating system packages available. These are: the OS/78 operating system that is included in the price of the basic DECstation-78 package; an optional commercial operating system, COS-310, for small business applications; and a word processing system, WPS-8, for documentation and other text editing needs. For real-time multitasking, RTS/8 can also be added.

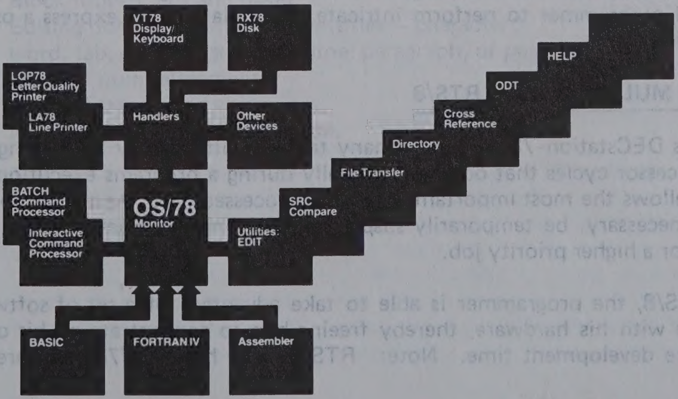
In addition to these basic software support packages, Harris can provide the user application software for linking the DECstation-78 to a hardware development system, such as the MICRO-12. Harris also has a software package to link the DECstation-78 to a Data I/O Model 9 PROM Programmer. PAL-8 based cross assemblers for the popular 8-bit microprocessors can be obtained from various sources, thus increasing the functionality of the DECstation-78. The user also has access to the extensive DECUS library of PDP-8 programs which in many cases can reduce development efforts.

MULTILANGUAGE OPERATING SYSTEM OS/78

OS/78 provides DECstation-78 users with power and flexibility in both interactive and batch programming environments. OS/78 is based on DIGITAL's proven OS/8 and offers many features previously available only on larger computer systems. OS/78 maximizes utilization of DECstation-78 main memory because the resident portion of the operating system requires only 256 words of memory. Non-resident portions of the system are swapped into memory from the RX78 floppy disk automatically as required.

OS/78 is easy to use and provides the development programmer with a complete, logical interface to program and file structures. All data files and executable programs are stored in one or more floppy disks where they may be accessed for loading, modification or execution by simple keyboard commands.

OS/78 incorporates Commercial BASIC and FORTRAN IV and provides a comprehensive set of software tools and utility programs that help make DECstation-78 an excellent program development and calculations tool in the single-user environment. These include EDIT, PAL8, CREF, ODT and BATCH PROCESSING, among others.


VT78 Display/ Keyboard
RX78 Disk
LQP78 Letter Quality Printer
LA78 Line Printer
Handlers
Other Devices
HELP
ODT
Cross Reference
Directory
File Transfer
BATCH Command Processor
OS/78 Monitor
SRC Compare
Interactive Command Processor
Utilities: EDIT
BASIC
FORTRAN IV
Assembler

EDIT — is a line-oriented text editor that allows the user to enter and modify ASCII files. It supports commands to list, insert, delete, change and move text as well as to search for character strings.

PAL 8 — is a two-pass language assembler that provides the programmer with the capability of coding directly in machine-oriented symbolic instructions. Its features include: 1) conditional assembly which enables a single source file to produce different binaries for different purposes; 2) paginated listings, page headings and page numbering to improve program documentation; and 3) a symbol table which lists all program labels and their memory location or value.

CREF (Cross-Reference Utility Program) — aids the programmer in writing, debugging and maintaining assembly language programs by providing the ability to pinpoint all references to a particular symbol. CREF provides an alphabetical cross-reference table for PAL8 assembly listings and numbers each line in the listing. Program symbols and literals are printed alphabetically along with the numbers of the lines that reference to them. Optional two-pass operations doubles the number of symbols that can be accommodated in a program.

BITMAP — is an OS/78 utility used to construct a table, or map, showing the memory locations used by a given binary file. BITMAP will accept any absolute binary file as input and route its output to any supported I/O device.

ODT (Octal Debugging Technique) — is invisibly co-resident with the user program so that there is no need to allocate more than 3 words in each 4K field for a debugging package during development. Breakpoints can be set anywhere in a program to allow the programmer to trace the execution of his program. Whenever program execution is suspended, ODT provides the capability to examine and optionally modify memory locations or registers. Specified areas of memory may be searched by means of ODT's binary memory search mechanism.

OS/78's Batch Processing utility — allows lengthy sequences of commands or frequently used programs to be run automatically on DECstation-78.

OS/78 BASIC — is high level, easily learned programming language compatible with Dartmouth BASIC. It uses simple English words, abbreviations and familar mathematical symbols to specify operations. BASIC can be used for executing large data processing tasks as well as performing quick, one-time calculations.

BASIC consists of an editor, compiler, and a runtime system, all three supporting BASIC's dual functions as an interactive program development tool and a system for interactive and batch execution. The BASIC instruction set includes powerful, yet simply learned commands which allow novices to do useful programming in a relatively short time. Extended operations and functions, such as program chaining and string operations, allow the more experienced programmer to perform intricate manipulations or express a problem efficiently and concisely.

REAL-TIME MULTITASKING RTS/8

RTS/8 allows DECstation-78 to handle many tasks simultaneously by making use of the otherwise idle processor cycles that occur periodically during a programs execution. A user-defined priority list allows the most important jobs to be processed first. As a result, programs in execution can, if necessary, be temporarily suspended and removed from memory (swapped out) to make room for a higher priority job.

By using RTS/8, the programmer is able to take advantage of a set of software modules that will interface with his hardware, thereby freeing him to concentrate on his own programs and greatly reduce development time. Note: RTS/8 must have OS/78 software as the operating system.

WORD PROCESSING SOFTWARE WPS-8

Word Station 78 is a complete word processing and visual text editing package for use in both stand alone and shared-logic environments. It can be added to the DECstation-78 and includes proven turnkey word processing software. Options include the LQP 78 letter quality printer and a Communications/Optical Character Reader interface which permits the word station to communicate over various grades of communications facilities with host computers or other word stations.

WS78 is powerful yet inexpensive enough to be used as a free-standing word processing system with its own processing capability, local storage and printers. The software is conveniently stored on the system floppy disk. Additonal space on the system floppy disk is reserved for a boilerplate library and a shorthand dictionary. "Shorthand" expressions might be names, addresses, titles, technical words or other standard short units of text that an organization uses repeatedly. These expressions may be stored on floppy disk, recalled with a few keystrokes and automatically inserted into the current text, thereby saving hours of retyping and increasing operator productivity. More than one hundred full pages of typing in as many as 200 separate files may be stored on a document diskette.

Because all the "programming" is in the software, DIGITAL word stations can be used by anyone for productive work after only a day's familiarization with the equipment. A typical stand-alone application, for example, might involve the use a a Word Station 78 in a development facility for the production of reports, documents and correspondence.

Word Station 78 Features:

Software Features:

- "Cue card" prompting of commands via visual display.
- Prestored rulers for margin, printer spacing and tabbing control.
- Format information stored with each document.
- Variety of printer output for mailing labels, envelopes, letterhead, technical manuals, etc.
- Simultaneous printing and editing.
- Justified margins.
- Underlined and overstruck printout.
- Time and date indexing of documents.
- Mailing list generation.
- Form letter merge.
- Insertion of boilerplate material.

Full Editing Features:

- Bi-directional search capabilities.
- Block move ("cut and paste").
- Editing done by grammatical entities — character, word, tab, column, sentence, line, paragraph, or page.
- Decimal point alignment.
- Swap of transposed characters.
- Manual or automatic pagination.

System Software

DIGITAL's Commercial Operating System (COS-310) is a self-contained, disk-resident operating system for small to medium-sized commercial applications. System features include:

- A comprehensive business programming language, DIGITAL's Business-Oriented Language (DIBOL).
- Numerous utilities to simplify program development and create, update, sort/merge and back-up data files.
- Sequential or random file accessing from disk storage.
- User file directories.
- A large system message library.
- Multivolume file support.
- Batch and interactive data processing.

Applications Flexibility

One of the most important characteristics designed and built into DEC COS-310 is flexibility — flexibility that lets 310 tackle a wide range of data processing problems and produce solutions quickly, efficiently, and economically. COS-310's flexibility is shown in its many uses:

- A stand-alone computer system.
- A remote job entry station.
- A "brilliant" terminal functioning as a satellite to a central computer system but having its own totally independent power.

COS-310 also services a wide range of users. Small companies can use COS-310 as their total processing system to perform payroll and other necessary accounting functions. Larger companies can use several DECstation-78's with COS-310 to decentralize their data processing by placing a DECstation-78 at each branch office to handle remote job entry while providing complete formatting and batch processing capabilities on a local level. Banks, insurance companies, manufacturers, warehousing operations — these are just a few of the many users who can profit from the cost-effective performance of COS-310. Standard applications programs are available from DEC as well as from numerous software firms.

The System for Small Companies

In small companies, COS-310 can be used in many applications areas — from order entry and inventory control to accounts payable, accounts receivable, and payroll. It can maintain credit files and information on outstanding orders, accept order entry information keyed in at the video terminal, print the packing tickets, update the inventory file, and generate invoices. COS-310 can also be used to report on back orders and future orders, to describe the company's overall sales picture, to keep track of salesmen's commissions, and to perform sales analysis and related processing tasks.

COS-310 can provide small companies with immediate information when it is needed, not sometime later when the "crisis" has passed. Customers are happier because their orders can be filled faster and more accurately. They receive up-to-date billing information and account statements with no delays — a benefit that means a good cash flow back from customers who want to maintain their credit ratings and/or discounts. Special discounts are easily handled by the system with each customer's account reflecting information that is unique to that company. Customer orders for the future can be entered into COS-310 and automatically processed at the exact time they were requested.

Support Literature

① **HARRIS DATA BOOKS**

- Digital Data Book
- Analog Data Book

② **HARRIS MANUALS**

- Harris Microprocessor Systems Design Manual
- MICRO-12 User's Manual

② **DEC MANUAL**

- Introduction to Programming

③ **DEC SYSTEM MANUALS**

- DECstation User's Guide
- DECstation Technical Manual
- OS/78 User's Manual
- RTS-8 User's Manual
- Word Processing System Reference Manual
- COS-310 System Reference Manual

NOTES:

① Data Books are available from Harris sales representatives and distributors.

② Manuals can be purchased from Harris Semiconductor, Melbourne, Fla. (see order form in back of this Data Book.

③ DEC Systems Manuals are available from DIGITAL Equipment Corporation.

Introduction to DECUS™

OVERVIEW

Since the HM-6100 microprocessor was designed to recognize the instruction set of the Digital Equipment Corporation (DIGITAL) ™ PDP-8/E ™ minicomputer, most programs written for the PDP-8 family are also usable with the HM-6100. The Digital Equipment Computer Users Society (DECUS) provides the vehicle through which HM-6100 and PDP-8 users can exchange ideas, information and user written programs. Harris Semiconductor supports the HM-6100 through participation in the 12-Bit Special Interest Group of DECUS.

HISTORY

DECUS was established in 1961 to " . . . advance the effcient use of DIGITAL computers. It is a voluntary, not-for-profit users group, supported in part by Digital Equipment Corporation."$_1$

ACTIVITIES

Symposia

The symposia, which are held throughout the year, provide a forum for users to meet with each other and with DIGITAL management. The papers and presentations are published as DECUS Proceedings shortly after each symposium and provide a permanent record of the meetings activities.

Special Interest Groups (SIGs)

The SIGs promote the interchange of specialized information through the publication of newsletters and the coordination of symposia sessions. At the symposiums they sponser business meetings, tutorials, and workshops which fulfill the two-fold purpose of fostering communication among users and between users and DIGITAL. User submitted articles, minutes of local meetings, and letters comprise the major portion of the newselters. Suggestions, hints, bug fixes, program plans, or questions of a non-commercial nature are suitable material for SIG newsletters.

The 12-Bit Special Interest Group is the vehicle through which users interested in 12-Bit hardware and software can share their ideas. Focus on user interest in HM-6100 related material (such as the DECstation-78) is provided by the MICRO-8 Working Group within the 12-Bit SIG. Various application notes, and hardware and software suggestions are covered in the MICRO-8 section of the 12-Bit SIG newsletter and at the symposia.

Program Library

One of the services performed by DECUS is the maintainence of a large library of programs for DIGITAL computers. The DECUS PDP-8 Program Library Catalog lists over 1200 assembly language and FOCAL ™ programs organized into 17 categories. Included are text editors, assemblers, debuggers, high-level languages (BASIC, FOCAL, ALGOL, SNOBOL, LISP, etc.), operating systems, input/output device handlers, mathematical packages, and various other types of application software.

MEMBERSHIP

Associate

An individual who wishes to join DECUS is eligible for an Associate (non-voting) membership if he has " . . . a bonifide interest in DECUS . . ."[1]. Associate Members receive DECUSCOPE, the Society's Newsletter, automatically. They may receive other DECUS material, such as the 12-Bit SIG Newsletter and the PDP-8 Library Catalog, on request.

Installation

An organization, institution, or individual that has purchased, leased, or has on order a computer manufactured by Digital Equipment Corporation (such as a DECstation-78) is elgible for Installation Membership in DECUS.

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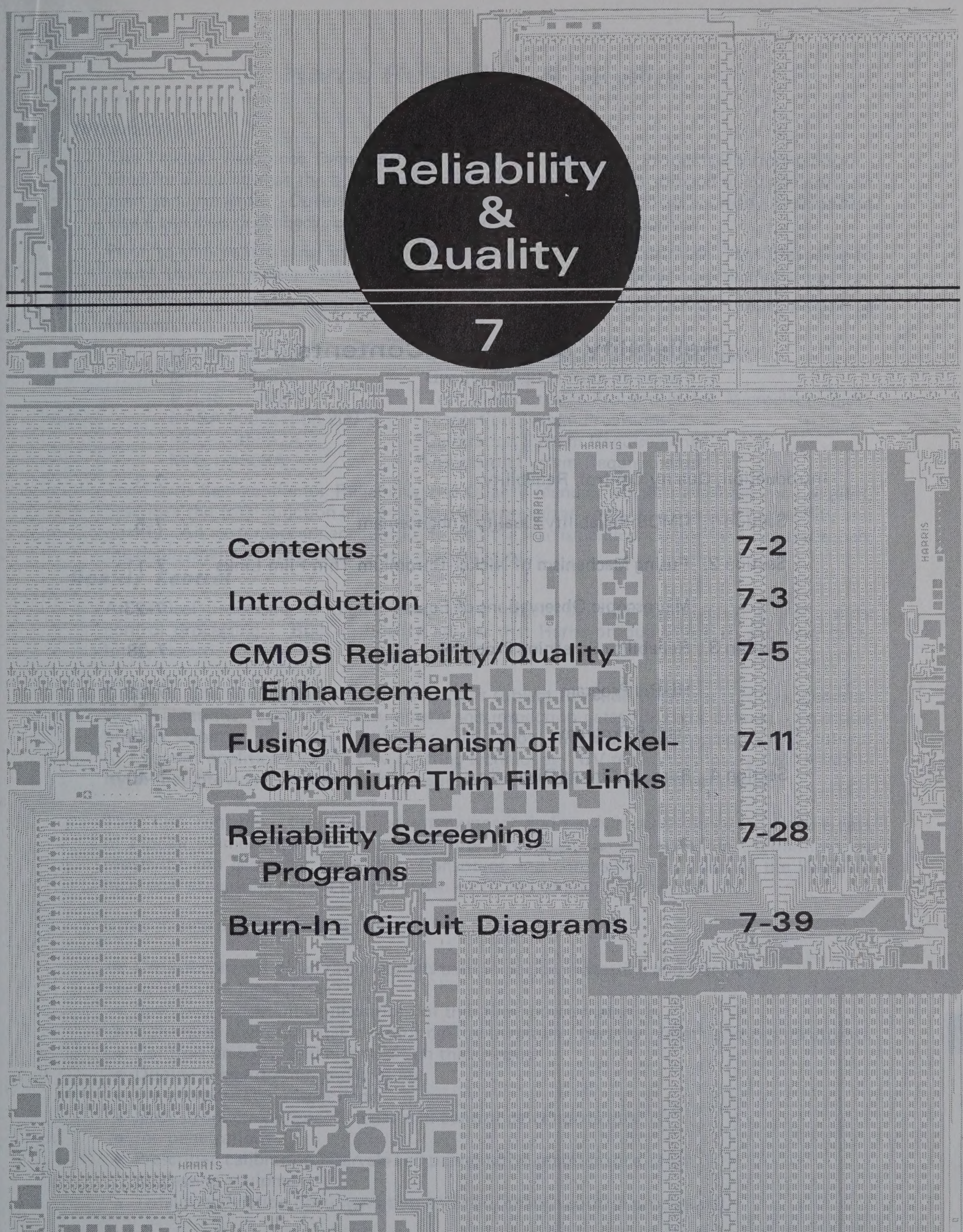
[1] DECUS Membership Brochure



Reliability & Quality

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Harris Reliability & Quality

Introduction

The Product Assurance Department at Harris Semiconductor Products Division is responsible for assuring that the quality and reliability of all products shipped to customers meet their requirements. During all phases of product fabrication, there are many independent visual and electrical checks performed by Product Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for HARRIS Product Assurance Program.

MIL-M-38510D	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883B	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662A	"Calibration System Requirements"
MIL-I-4508A	"Inspection System Requirements"

The Harris Semiconductor Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the Harris Semiconductor facilities and survey the deployment of the Product Assurance function.

Quality Control

All critical processing of digital products is subject to rigid manufacturing and quality control processing. Built-in quality assures that Harris products have an excellent reliabitlity record.

Diffusion and ion implantation processing is subject to oxide thickness controls, penetration evaluations, resistivity measurement and inspection gates for visual defects. To insure process stability, diffusion furnaces, metallization and passivation equipment is subject to frequent qualifications via C-V plotting techniques. CV techniques insure CMOS stability as they provide a very sensitive measure of the concentration of ionic species.

Thin film controls insure specified interconnect and passivation thicknesses. In the case of bipolar memory circuits, the NiCr fuse processing is very carefully monitored via resistivity and geometry controls. Consistent and controlled execution of the HARRIS nichrome processing has led to very reliable PROMS of high programmability.

Other in-line process controls include:

- Critical controls on all raw materials used in device processing and assembly
- In line SEM inspections
- Specified consistent compositions of thin film source materials
- Continual environmental monitoring for humidity, particle counts and temperatures
- Controls on oxide and metallization thicknesses
- Doping concentration and profiles
- Pre and post etch inspections
- Mask production inspection gates to control defect densities
- Ion penetrations
- Prescribed calibration intervals and preventative maintenance of all processing equipment
- Total specification documentation and rigid change control procedures

Harris maintains a well equipped Analytical Services Dept. which is managed by Quality Control. This area consists of a microscopy laboratory and a complete wet chemical analysis facility. The microscopy lab includes a Scanning electron microscope with energy dispersive X-ray analysis capability, electron microprobe, Scanning Auger with ESCA attachment, SIMS and all sample preparation equipment.

Equipment also includes atomic absorption and optical emission spectrocopy, UV visible and infra red and a profilometer. This laboratory has the capability to do quantitative and qualitative analyses of all semiconductor materials. This on-site facility assures Harris built-in quality and reliability.

Reliability

The reliability approach at Harris Semiconductor is based on designing in reliability rather than testing for reliability only. The latter is applied to confirm that sound design with quality and reliability based ground rules are observed and correctly executed in a new product design.

Reliability engineering becomes involved as early as concept review of new products and continues to remain involved through design and layout reviews. At these critical development points of a new design, basic reliability oriented layout guidelines are invoked to insure an all-around reliable design. This concept is reflected by the Harris reliability requirement procedures which encompass mandatory first run product evaluation. This is done at not only the circuit level, but also at the process technology and package level. Reliability engineering approval is required before new product designs are released to manufacturing.

Tests at both maximum rated and accelerated stress levels are performed. Acceleration is important to determine how and at what stress level a new design would fail. From this information, necessary design changes can be implemented to insure a wider and safer margin between the maximum rated stress condition and the device's stress limitation.

The notably low failure rates for the Bipolar and CMOS Memory products are a direct result of the application of this reliability concept. For the PROM circuits, the high standards for reliability and quality; have yielded the industry's high programmability yields. Our demonstrated expertise in NiCr fusing has resulted in observed failure rates which are less than equivalently complex TTL LSI circuits. For example, derating according to the arrhenius reaction rate (1.0eV activation energy) gives a failure rate of 0.0002%/1000 hours or 2 FITs at +50°C ambient for programmed bipolar PROMs. For the 65XX CMOS Memory products the +50°C derated failure rate is 0.0001%/1000 hours or 1 FIT (based on 1.2 e.V).

The excellent reliability peformance is further exemplified by our customers. Analysis of parts returned to Harris indicates the following results. For the CMOS Memory products, the returns constiture 0.2% of the total volume shipped, while for the Bipolar Memory products this figure is 1.5%. This number includes all programmability rejects for the PROMs.

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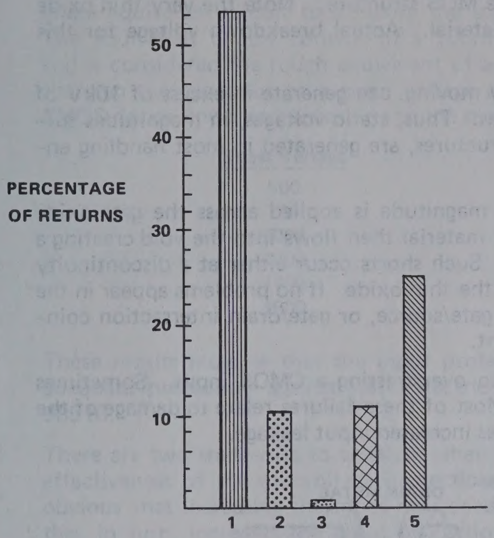
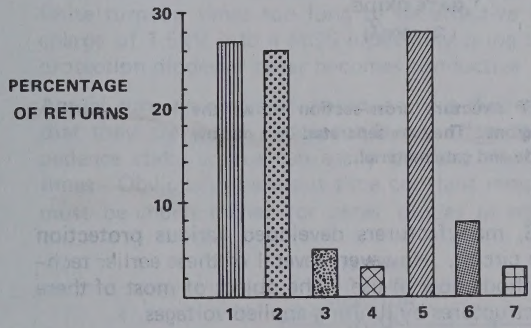
The accompanying charts illustrates the distribution of categories for why devices are returned. Note that 60-70% of these returned are devices that were not defective when they were shipped. These units failed due to electrostatic damage (ESD), electrical overstress (EOS), or were good devices which were incorrectly identified as board or system level failures. The latter category is defined as invalid returns and represents 30-40% of the total number of returned units.



CMOS FAILURE CATEGORIES
(TYPICAL REPRESENTATION)

CUSTOMER INDUCED PROBLEMS: 66%	
1. INVALID RETURNS	56%
2. EOS/ESD	1%
OBSERVED FAILURE MODES : 34%	
3. ASSEMBLY	1%
4. TEST ESCAPES	10%
5. PROCESSING FLAWS	24%

RETURNED UNITS EQUAL≃1.5% OF TOTAL PARTS SHIPPED



BIPOLAR FAILURE CATEGORIES

(TYPICAL REPRESENTATION)

CUSTOMER INDUCED PROBLEMS: OF RETURNED UNITS	61%
1. INVALID RETURNS	27%
2. CUSTOMER PROGRAMMING PROBLEMS	26%
3. BLOWN BOND WIRES (REVERSE INSERTION)	5%
4. EOS, V_{CC} SPIKES	3%
OBSERVED FAILURES MODES:	
5. PROCESSING FLAWS	28%
6. ASSEMBLY	8%
7. TEST ESCAPES	3%

RETURNED UNITS EQUAL ≃ 1.5% OF TOTAL PARTS SHIPPED

Section 1. CMOS Reliability/Quality Enhancement

To ensure a totally reliable product and system, the design engineer needs to understand the capabilities and limitations of CMOS product. In addition, a clear understanding of the techniques employed to improve reliability is essential for High Reliability system goals. The following describes the necessary tools to enhance CMOS reliability.

DESIGNING OUT FAILURE MODES

Static Charge

Since the introduction of MOS, manufacturers have searched for effective and safe ways of handling this voltage sensitive device. High input impedance of CMOS, coupled with gate-oxide breakdown characteristics, result in susceptibility to electrostatic charge damage.

Figure 1 shows a cross-section of a silicon gate MOS structure. Note the very thin oxide layer (≈ 1000Å)* present under the gate material. Actual breakdown voltage for this insulating layer ranges from 70V to 100V.

Handling equipment and personnel, by simply moving, can generate in excess of 10kV of static potential in a low humidity environment. Thus, static voltages, in magnitudes sufficient to damage delicate MOS input gate structures, are generated in most handling environments.

A failure occurs when a voltage of sufficient magnitude is applied across the gate oxide causing it to breakdown and destruct. Molten material then flows into the void creating a short from the gate to the underlying silicon. Such shorts occur either at a discontinuity in doping concentration, or at a defect site in the thin oxide. If no problems appear in the oxide, breakdown would most likely occur at gate/source, or gate/drain intersection coincidence due to the doping concentration gradient.

Noncatastrophic degradation may result due to overstressing a CMOS input. Sometimes an input may be damaged, but not shorted. Most of these failures relate to damage of the protection network, not the gate, and show up as increased input leakage.

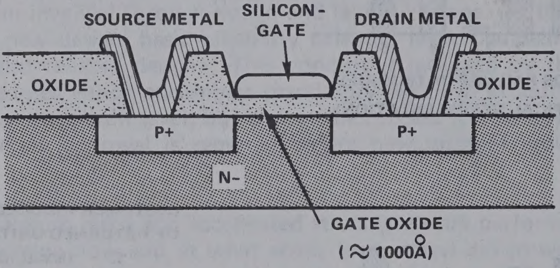


FIGURE 1 — Silicon-gate PFET structure cross-section shows the heavily doped source and drain regions. They are separated by a narrow gap over which lies a thin-gate oxide and gate material.

Voltage Limiting Input Protection

During the evolution of monolithic MOS, manufacturers developed various protection mechanisms that are an integral part of the circuit. However, several of these earlier techniques have been replaced by improved methods now in use. The object of most of these schemes is to prevent damage to input-gate structures by limiting applied voltages.

Recent CMOS designs employ a dual-diode concept in their input protection networks. Figure 2 illustrates such a protection circuit.

One characteristic of junction-isolated CMOS protection circuits is the ≈ 200Ω current limiting resistor. Cross sectional area of the metallization leading to the resistor, and the area of the resistor are, therefore, designed to absorb discharge energy without sustaining permanent damage. This dual-diode protection has proved very effective and is the most commonly used method in production today.

HARRIS INPUT GATE PROTECTION

To protect input device gates against destructive overstress by static electricity accumulating during handling and insertion of CMOS products, Harris provides a protection circuit on all inputs. The general configuration of this protection circuit is shown in Figure 2.

Both diodes to the V_{DD} and V_{SS} lines have breakdown voltages averaging between 35 and 40 volts. Excessive static charge accumulated on the input pin is thus effectively discharged through these diodes which limit the voltage applied from gate to drain and source. The 200 ohm resistor provides current limiting during discharge. Depending on the polarity of the input static charge and on which of the supply pins are grounded, the protective diodes may either conduct in the forward direction or breakdown in the reverse direction.

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*1Å (Angstrom = 10^{-8}cm)

In order to test this concept, step stress tests have been performed at Harris using an approximate equivalent circuit to simulate the static charge encountered in handling operations. The equivalent circuit consists of a 100pF capacitor in series with a 1.5K ohm resistor and is considered the rough equivalent of a human body. Step stressing takes the form of charging the capacitor to a given voltage and then discharging it into an input pin of the CMOS device under test according to the sequence given in MIL-M-38510.

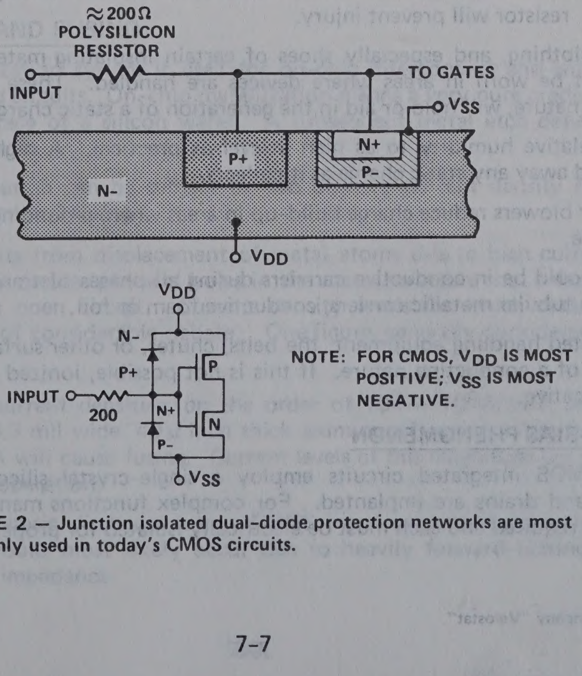
Stress Voltage	Cumulative Failures
500	0
700	0
1000	0
1500	1
1700	3
1800	4

These results indicate that the input protection used for Harris CMOS products provides adequate protection against static electricity based on the limits specified in MIL-M-38510.

There are two trade-offs to consider when fabricating an input protection scheme, namely effectiveness of the overvoltage protection and performance of the overall circuit. It is obvious that increasing the series resistance and capacitance at an input limits current and this, in turn, increases the input protection's ability to absorb the shock of a static discharge. However, such an approach to protection can have a significant effect on circuit speed and input leakage. The input protection selected must therefore provide a useful performance level and adequate static-charge protection.

Commonly used MOS-input protection circuits all have basic characteristics that limit their effectiveness. The zener diodes, or forward-biased pn-junctions, employed have finite turn-on times too long to be effective for fast rise-time conditions. A static discharge of 1.5kV into a MOS input may bring the gate past its breakdown level before the protection diodes or zener becomes conductive.

Actual turn-on times of zeners and pn-diodes are difficult to determine. It is estimated that they are a few nanoseconds and a few tens of picoseconds, respectively. A low-impedance static source can easily produce rise times equal to or faster than these turn-on times. Obviously the input time constant required to delay buildup of voltage at the gate must be much higher for zener diodes or other schemes having longer turn-on times.



NOTE: FOR CMOS, V_{DD} IS MOST POSITIVE; V_{SS} IS MOST NEGATIVE.

FIGURE 2 — Junction isolated dual-diode protection networks are most commonly used in today's CMOS circuits.

Consider an example. Figure 3 shows a test circuit that simulates the discharge of a 1.5kV static charge into a CMOS input. Body capacitance and resistance of the average person is represented by a 100pF capacitor through 1.5kΩ. Switch A is initially closed, charging 100pF to 1.5kV with switch B open. Switch A is opened, then B is closed, starting the discharge. With the 1.5KΩ x 5pF time constant to limit the charge rate at the DUT input, it would take approximately 350psec to charge to 70V above V_{DD}. Diode turn-on time is much shorter than 350psec, hence the gate node would be clamped before any damage could be sustained.

There is no completely foolproof system of chip-input protection presently in production. If static discharge is of high enough magnitude, or of sufficiently short rise-time, some damage or degradation may occur. It is evident, therefore, that proper handling procedures should be adopted at all times.

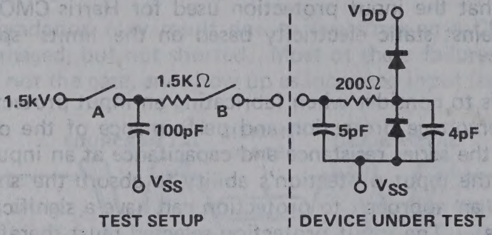


FIGURE 3 — Input protection network test setup illustrates how diode clamping prevents excessive voltages from damaging the CMOS device.

HANDLING RULES

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground. The 1MΩ resistor will prevent injury.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge.
- Control relative humidity to as high a level as practical. A higher level of humidity helps bleed away any static charge as it collects.
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.
- Devices should be in conductive carrriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces the leads contact should be of a conducting nature. If this is not possible, ionized air blowers may be a good alternative.

THE FORWARD-BIAS PHENOMENON

Monolithic CMOS integrated circuits employ a single-crystal silicon wafer into which FET sources and drains are implanted. For complex functions many thousands of transistors may be required and each must be electrically isolated for proper operation.

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*Supplier: 3M Company "Velostat".

Junction techniques are commonly used to provide the required isolation – each switching node operating reverse-biased to its respective substrate material. Additionally, as previously mentioned, protection diodes are provided to prevent static-charge related damage where inputs interface to package pins. Forward-biasing any of these junctions with or without power applied may result in malfunction, parametric degradation, or damage to the circuit.

Before proceeding, it should be pointed out that junction isolation, in the classical sense, is not implemented in the CMOS structure. Although commonly called junction isolation, the CMOS technique varies substantially from that used in bipolar TTL (Figure 4).

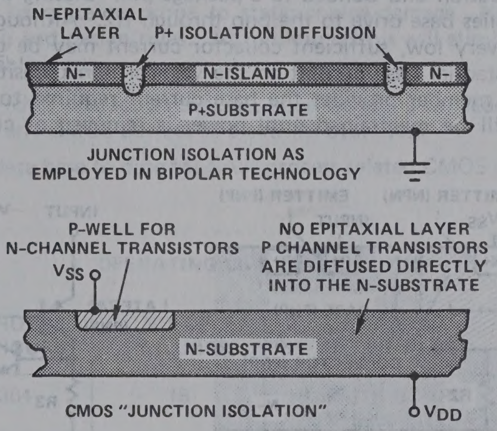
N-EPITAXIAL LAYER
P+ ISOLATION DIFFUSION
N-
N-ISLAND
N-
P+SUBSTRATE
JUNCTION ISOLATION AS EMPLOYED IN BIPOLAR TECHNOLOGY
P-WELL FOR N-CHANNEL TRANSISTORS
NO EPITAXIAL LAYER P CHANNEL TRANSISTORS ARE DIFFUSED DIRECTLY INTO THE N-SUBSTRATE
V_{SS}
N-SUBSTRATE
CMOS "JUNCTION ISOLATION"
V_{DD}

FIGURE 4 – Junction isolation for bipolar and CMOS differ considerably. CMOS utilizes a simpler technique that takes advantage of its less complex processing.

ELECTROMIGRATION AND FUSING

An aluminum metallization system is used for on-chip interconnect and wire bonding of most CMOS integrated circuits. On-chip metallization means a very pure grade of aluminum deposited on the surface of a silicon wafer. A subsequent metal etch defines the interconnect pattern.

This on-chip metallization can be subject to two primary current density related failure modes, electromigration and fusing.

Electromigration results from displacement of metal atoms due to high current densities. Displacement of atoms creates physical holes in the metal structure that enlarge with time, eventually causing an open circuit. Current density levels for which circuit life is not impaired are subjects of considerable debate. One figure, generally considered to be ultra-safe, is 10^5A/cm^2.

Considerably higher current densities, on the order of $10^6 - 10^8$A/cm^2, are required to cause fusing. For a 0.3 mil wide 40 μ inch thick aluminum line and a fuse current density of 10^7A/cm^2, 775mA will cause fusing. Current levels of this magnitude are not generated during normal CMOS operation.

Could a high-energy static discharge into a CMOS input or output cause fusing ? Yes, but such a failure would most likely occur due to heavily forward-biasing an input or output through a low impedance.

High currents resulting from an excessive forward-bias can cause severe overheating localized to the area of a junction. Damage to the silicon, overlying oxide and metallization can result.

BIPOLAR PARASITICS

Care must always be exercised not to forward-bias junctions from input or output pads.

A complex and potential defect phenomenon is the interaction of a npn/pnp combination a la SCR (Figure 5). Forward-biasing the base-emitter junction of either bipolar component can cause the pair to latch up if $\beta_{npn} \times \beta_{pnp} \geq 1$. The resultant low impedance between supply pins can cause fusing of metallization or over-dissipation of the chip.

Figure 5 shows how an SCR might be formed. The p+ diffusion labeled INPUT is connected to aluminum metallization and bonded to a package pin. Biasing this point positive with respect to V_{DD} supplies base drive to the pnp through R2. Although gain of these lateral devices is normally very low, sufficient collector current may be generated to forward-bias and supply substantial base current to the vertical npn parasitic. Once the pair has been activated, each member provides the base current required to sustain the other. A latched condition will be maintained until power is removed or circuit damage disables further operation.

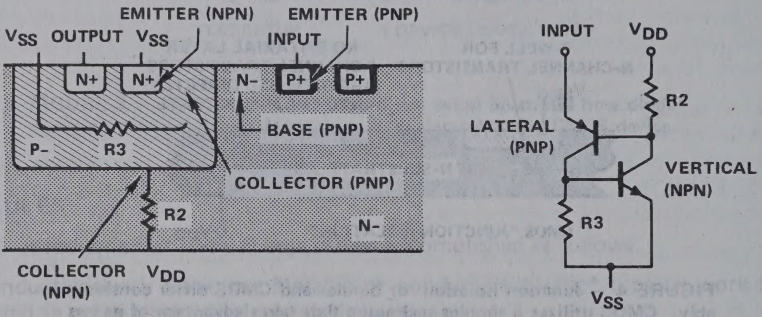

FIGURE 5 – Improper biasing can latch-up this SCR configuration. A p+ guard ring is commonly used to kill lateral pnp action. This ring is diffused into the surface at the junction of p- and n- silicon.

DESIGN RULES EQUALLY IMPORTANT AS HANDLING RULES

A system using CMOS devices must have reliability designed in. No amount of testing can guarantee long term reliability when poor design practices are evident.

- Never apply signals to a CMOS circuit before power has been turned on (to prevent latch-up)
- Supply filter capacitance should be distributed such that some filtering is in close proximity to the supply pins of each package. Testing has shown 0.01 μF/package to be effective in filtering noise generated by most CMOS functions.
- CMOS signal lines are terminated at the driving end by a relatively high impedance when operating at the low end of the supply voltage range. This high-impedance termination results in vulnerability to high-energy or high-frequency noise generated by bipolar or other non-CMOS components. Such noise must be held down to manageable levels on both CMOS power and signal lines.
- Where CMOS must interface between logic frames or between different equipments, ground differences must be controlled in order to maintain operation within absolute maximum ratings.

- Capacitance on a CMOS input or output will result in a forward-bias condition when power is turned off. This capacitance must discharge through forward-biased input or output to substrate junctions as the bus voltage collapses. Excessive capacitance (thousands of pF) should be avoided as discharging the stored energy may generate excessive current densities during power-down.
- Where forward-biasing is inevitable, current limiting should be provided. Current should not be permitted to exceed 1mA on any package pin excluding supply pins.

All CMOS is susceptible to damage due to electrical overstress. It is the user's responsibility to follow a few simple rules in order to minimize device losses.

He should first select a source for the CMOS device that employs an effective input protection scheme. This will allow a greater margin of safety at all levels of device handling since the devices will not be quite so prone to static charge damage. Next, he should apply a sound set of handling and design rules. At minimum, this will eliminate electrical stressing or hold it to manageable levels.

With an effective on-chip protection scheme, good handling procedures and sound design, users should not lose any CMOS devices to electrical overstress.

The total reliability data base to date for SAJI process related CMOS products is represented as follows:

OPERATING LIFE TEST RESULTS

NO. OF DEVICES	DEVICE-HOURS DEVICE-HOURS	NO. OF FAILURES	OBSERVED FAILURE RATE	DERATED TO 50°C (1)
2,332	2,634,304	18	0.68%/1K HOURS OR 6800 FITs	0.0003%/1K HOURS OR 3 FITs
POST 168 HOURS		2	0.07%/1K HOURS OR 700 FITs	0.00003%/1K HOURS OR 0.3 FITs

(1) Derating is based on activation energy of 1.2eV.
Above data reflects dynamic operating life at V_{DD}=5.5V, f_0=1MHz
@ T_A=+125°C using unburned in product.
1 FIT (failure unit)=1 failure in 10^9 device-hours.

Section 2. Fusing Mechanism of Nickel-Chromium Thin Film Links

Nickel-chromium fusible link programmable read-only memories, PROMs have been developed and utilized since their inception during the early 1970's [1]. The physical mechanism of fusing these links has been generally described as melting,[2] but with the advent of a successful transmission electron microscopy technique [3], has detailed information on the structure of the programmed fuse gap become available. These observations, coupled with electrical and thermodynamic characterization of the fusing event, have led to a clearer understanding of this phenomenon with concurrent definition of programming conditions for reliable operation of programmed PROMs.

SOME RELEVANT GENERAL PROPERTIES OF NICKEL-CHROMIUM

Fundamental to the mechanism of NiCr fusing are those physical properties that make it an excellent registor material from processing, design and applications perspective. It is no accident of history that NiCr is widely used for resistors on solid state devices.

To begin with, NiCr is a resistive material comprised of two transition metals-nickel and chromium. In transition metals, the outer electron shells contain only one or two electrons and some of the conduction electrons must come from inner shells. The inner shell conduction electrons are shielded by the outer shell resulting in a high scattering and trapping site density. Thus, transition metals are inherently less conductive than normal metals[4]. In the case of NiCr, an **alloy** effect[4] occurs to further enhance electron scattering. The result is that the resistance of the alloy is much higher than the arithmetic average of its two components[5] as illustrated in Figure 1**.

The resistivity of NiCr makes it well suited for small geometry thin film resistors that are size compatible with high density fuse design requirements. Due to its high resistivity the thickness of NiCr that is necessary to achieve a typical fuse resistance of 300 ohms is an advantageous property for a fuse, as will be described later. There is also the elimination of step coverage problems where the metallization (aluminum) contacts the NiCr.

A consequence of the extensive electron scattering in NiCr is a short mean free path of the conduction electrons. For example, the mean free path in gold is 380Å[6] compared to an estimated 40Å for NiCr. As a consequence, films greater than 100Å thick have bulk resistivity properties (i.e., surface effects are not dominant). As Figure 2 shows, surface scattering effects which reduce conduction are absent by the time the resistor film is greater than 100Å[7] in thickness. The practical ramification of this property is reproducibility in the fabrication process. Because there is no dependence on surface effects to achieve the desired sheet resistivity, thin film resistors may be produced with excellent tolerance and stability[8].

The short mean free path is also relevant to describing the fusing mechanism, discussed in the Mass Transport Models section.

NiCr is a material that forms a self-limiting oxide skin. That is, the oxide of NiCr is known to be a coherent spinel[9,10], see Figure 3. It is postulated that in the course of processing NiCr resistors, this thin spinel sheath will form around the NiCr to a thickness of Δ 20Å. This sheath serves to stabilize the resistors and is partly responsible for the excellent thermal stability (absence of ≃ R(T) effects) of NiCr[11]. This spinel may also be a factor in the fusing pehnomenon.

MICROSTRUCTURE OF A PROGRAMMED NICKEL-CHROMIUM FUSE

The technique of using transmission electron microscopy (TEM) to examine programmed fuse gaps was developed by Dr. Kinsey Jones at C.S. Draper Labs[3,12]. It is the only technique which mutually satisfies the requirements of sufficient resolution to analyze the gap and not destroy in sample preparation the structure to be analyzed. It is this latter point that has severely limited the utility of the scanning electron microscope (SEM) in endeavors to analyze programmed NiCr fuses. In depassivating devices, necessary with the SEM, microstructural details of the fuse gap are destroyed. Many interpretations of the fusing phenomenon based on SEM results have been erroneous or misleading because what was seen was an artifact of sample preparation.

Figure 4 illustrates schematically the utilization of transmission electron microscopy for fuse gap analysis. Of course, besides direct structure observation, composition of various phases may be ascertained by electron probing.

The microstructure of a programmed fuse gap in a PROM circuit via TEM is shown in Figure 5. The relevance of those programming conditions will be discussed further in following sections, but Figure 5 is representative of the gapcreated in aNiCr fuse under programming power conditions specified[13] for PROM's.

The TEM micro photograph indicates the elemental distribution found by microprobing. The following observations are made:

a. The visual appearance indicates that the neck of the fuse was in the molten state during programming.

b. Mass transport of the nickel and chromium from the gap region has occurred.

c. There is asymmetry to the melted NiCr distribution. That is, there is more densified NiCr on what was the cathode (negative) side of the fuse which suggests the molten NiCr moved in a direction opposite to electron flow during programming.

d. The gray phase (region C) of the gap which comprises the insulative separation of the two sides of the fuse is devoid of nickel and composed of oxides of silicon and chromium[14]. The typical separation is 0.6-1.0 microns. The resistance across the gap is > 10 megohms and it will not break down, electrically or structurally to voltages in excess of 100 volts.

e. The white spots, dark spots and filaments are described by the fluid dynamics of a disintegrating liquid sheet[12]. Briefly, that model describes how minute discontinuities in a liquid sheet, perterbate into larger holes and finally into droplets and filaments because of surface tension effects. The structure looks similar to a "frozen splash".

MASS TRANSPORT MODELS

In the previous section, it has been demonstrated that programmed NiCr fuses melt and that mass transport takes place. But what is the mechanism, the driving force for mass transport ? Table 1 lists the possibilities.

Table 1

(1) Electromigration (Huntington & Grone[15]): Mass flux occurs under the influence of high current flow because electron collisions with atoms of the conducting medium provide a net motion vector in the direction of electron flow.

(2) Thermal gradient (Soret[16]): In the presence of a thermal differential, material will diffuse from the high temperature to the low temperature region.

(3) Concentration gradient (Fick[17]): In an imbalanced distribution of concentration, mass will diffuse from regions of higher concentration to lower concentration.

(4) Field enhanced ionic mobility (Eyring and Jost[18]): Molten metals will ionize, lose electrons and become cations. In the presence of an electric field, they will be driven towards the cathode.

Considering each possible mechanism in turn:

(1) Electromigration — On the surface, this seems a most logical explanation for programming. It is known that the current densities in a fuse neck at programming are very high ($\sim 5 \times 10^7$ amps/cm^2) and it could be postulated that this electron flux sweeps the nickel and chromium from the gap. But empirical data and theoretical considerations show this not to be the case.

   a. TEM of the fuse gap indicates the molten NiCr has moved in a direction opposite to electron flow.

   b. Theoretical calculations of the kinetic energy of conduction electrons in NiCr demonstrate that because the mean free path is short and the lattice binding energy is high (transition metals typically have high melting points), the electrons have insufficient energy to impart the mobility to the nickel and chromium atoms necessary for electromigration in the direction of electron flow.

However, general treatments of electromigration theory[15, 24] identify two forces acting on atoms of the conducting medium. One is the aforementioned electron momentum ("electron wind") in the direction of electron flow. The other is the electrostatic force from the applied electric field that causes ions of the conducting material to move opposite to the direction of electron flow. See mechanism (4).

Obviously, the joule heating that leads to melting the fuse is coming from electron interaction with the NiCr film. There is no incongruity with the fact that this is not leading to electromigration such as observed in aluminum. Because the mean free path is short, the energy exchanged per collision is small. But because electron scattering is a dominant factor in resistive materials, the frequency of collisions is high. Thus, thermal energy (lattice vibration) is added to the metal atoms. The electron collisions increase the amplitude of the atomic vibration and increase the temperature. This is why NiCr is an efficient material for converting electrical energy into thermal energy (toaster effect).

(2) Thermal Gradient – From an analysis of heat flow in a fuse, it has been shown (see the Transient Heat Flow Analysis section), Figure 6, that the temperature profile across a fuse neck is flat. The gradient occurs at the neck-to-fuse body interface. But the programmed gap occurs in a region where there is no temperature gradient. Further, this model would predict a symmetric distribution of mass, post-programming which is not observed. Temperature gradient does not cause the mass transport.

(3) Concentration Gradient – It has been shown in unprogrammed fuses that no concentration gradient exists. Laterally in the fuse film this is borne out by the TEM/probe analysis. That is, no nickel or chromium concentration variations are observed across an unprogrammed fuse. Vertically (distribution of nickel, chromium through a cross section of the resistor) it has been shown[20], from sputter etching Auger analysis that the nickel and chromium are distributed uniformly through the film (no concentration layering effects).

Because there is no concentration gradient initially, this is ruled out as a starting mechanism for fusing.

(4) Field Enhanced Ionic Mobility – Eyring and Jost[18] have observed that liquids have a fixed ratio between their energy as a liquid and the energy required for vaporization, see Figure 7. Stated simply, the principal is, the more cohesive the liquid, the more energy is required to transform it to the gaseous phase, and the ratio is a constant. This rule held for all types of liquids (gases, solvents, organics, etc.) except metals. But by accounting for ionization of molten metals and the subsequent reduction in atomic radii, see Table II, they found that metals obeyed the liquid:gas constant energy ratio. In other words, molten metals are ionic.

It follows then that these positive ions (they have given up outer shell electrons) will move in the presence of an electric field (from the programming pulse) toward the negative terminal, opposite to the direction of electron flow. This is consistent with the TEM observations and with some investigations of electromigration. For example, Wever[25] observed in copper above 950°C, that mass flux was toward the cathode.

In summary, NiCr fuses program as follows: **A programming pulse of sufficient power is applied across the fuse. Power dissipation in the fuse neck heats this region into the molten state and the nickel and chromium atoms become ionized. They move toward the negative side of the fuse and the liquid film begins to disintegrate. The film becomes electrically discontinuous and rapidly returns to the solid state, the final structure resembling a frozen splash described by fluid dynamics. The fuse gap consists of insulative oxides of silicon and chrome, with resistance >10 megohms.**

Footnote: Arguments have also been advanced that oxidation is the mechanism of fusing[19]. If this were so, the probe data, which discerns elemental presence, would not show nickel and chromium depletion in the gap region, i. e., mass transport, per se, would not have occured. Because the TEM data clearly indicates mass transport, attention is focused here on identifying the driving force for that mass transport.

TRANSIENT HEAT FLOW ANALYSIS

The previous discussions dealt with the fusing event postfacto, describing the microscopic material structure created by programming. The dynamics of the fusing event can also be characterized. By modeling the fuse structure and its environment in terms of classical heat flow, the connection between electrical and material behavior of fuses can be established.

A computer thermal analysis program called "THEROS"[21] was used to calculate the dynamic temperature effects in a PROM-fuse structure as a function of applied power density.

This computer program can thermally model a multicomponent structure and calculate the temperature as a function of time for given power dissipation conditions. The program takes into account temperature dependent thermal properties of the various materials and models a 2-dimensional multimaterial, multigeometrical structure into a RC circuit network that can be analyzed by sophisticated transient circuit analysis programs. This approach is convenient because the differential equations that describe heat flow problems have the same form as differential equations for RC circuit networks. For example, specific heat is analogous to capacitance, thermal conductivity is analogous to the inverse of resistance, temperature is analogous to voltage and heat flow is analogous to current. By way of the "THEROS" heat flow to electrical analog program, the sophistication available with present circuit analysis programs can be utilized to solve complex heat flow problems without consuming hours of computer time and without the errors prevalent in more simplified calculations. For the heat flow model to be truly representative of the actual device, the immediate environment of the fuse must be completely accounted for. For example, the passivating oxide layer on top of the fuse will affect the heat flow and the subsequent structure of the programmed fuse. Programming a fuse without the passivating oxide[22] will result in a different structure than occurs in an actual PROM circuit.

The term "power density" is defined as the amount of power that is dissipated in the fuse neck region divided by the area of the fuse neck (watts/mil^2), see Figure 8. The concept of defining power density as power per unit surface area is applicable to thin film heat flow problems where the heat is dissipated through a surface. (The concept is analogous to defining current density as current per cross sectional area). Figure 9 shows a plot of the computer results giving the temperature in the center of the NiCr fuse that would be achieved if a constant power were applied for a time t. The curves show that the fuse can easily reach the melt temperature of NiCr[23] within microseconds for power densities > 2.5 watts/mil^2.

Figure 10 is a plot of the intercept of the time to reach the melt temperature (1450°C) vs. the power density. This theoretical prediction of the power density versus time to reach the melt temperatures compares well with experimental data on time to fuse. The data in Figure 10 was taken from test vehicle fuses, processed identically to circuit fuses, but free of interfacing circuitry. This allowed precise characterization of fuse-pulse interactions. The data matches for long fusing time but deviates for short fusing time. This difference can be accounted for by considering the definition of "time to fuse". The experimental data points represent total time to fuse which includes rise time of the programming pulse, time for the fuse to heat to sufficient temperature, and time of the actual fusing event. For example, Figure 11 shows a typical current trace for a fuse programmed under constant voltage conditions. The trace shows a fixed rise time, t_r (about 100 nanoseconds for this data), a response time, t_m, for the NiCr to reach the melt temperature, and a time for the fuse neck to enter the melt phase and program, t_f. Plotting the time defined as t_m shows excellent correlation with the theoretical prediction of the time to reach melt temperature. The difference between the theoretical prediction to reach melt and the actual time to fuse agrees with the measured values of $t_r + t_f$. Figure 10, therefore, shows that fusing follows a heat flow dependence that requires the NiCr to achieve melt. Proper PROM design necessitates taking into account thermal factors that affect the heat flow conditions in the neighborhood of the fuse. Concentrating power by optimum fuse geometry and ensuring sufficient power to the fuse will achieve fast, uniform programming.

For power density conditions below the programming threshold level, the fuse temperature as a function of power density into a fuse for a sustained pulse (t ⟶ ∞) is shown in Figure 12. There is good agreement of the computer model with experimental data. The experimental data was derived from measuring the fuse resistance (at reduced current, avoiding I^2R heating) of an externally heated fuse and comparing that to the power necessary to generate the same resistance at an ambient temperature of 25°C. The agreement between model and experimental data is a further indication that the heat flow analysis is correctly projecting the temperature in the fuse.

It is also relevant to note the low power density on a fuse in the read mode, 5% of the threshold power density to melt the NiCr fuse. Test vehicle fuses were stressed at 1 watt/mil^2 which is 65% of the fusing threshold level and equivalent to a fuse temperature of 800°C. No failure occured after 4000 hours of continuous operation. Thus, the designed power density for PROM operation in the read mode avoids the occurence of unprogrammed fuses becoming open.

In summary, the power density vs. time to program curve, Figure 10, agrees with the heat flow model and implies a single mechanism, melting for both fast and slow fusing. High power fusing (fast blow) approaches adiabatic heating conditions and therefore gives a large melted region and wide gap. Restricted power programming (slow blow) allows much of the heat to diffuse away taking longer for the fuse to reach melt.

MARGINALLY PROGRAMMED FUSE

By grossly violating recommended programming procedures for fuses, it is possible to create a marginal fuse gap that may be subject to reverting state ("growback"). This anomaly was induced in a test vehicle fuse by restricting the power input to a value on the t ⟶ ∞ asymptote (~ 1.5 watts / mil^2) of the power density vs. time to fuse curve (Ref. previous section, Figure 10). Under these conditions, a fuse was induced to program, become electrically discontinuous, after 5 minutes of sustained power. This effect, programming under an anomalously reduced power, was not found to be reproducible. Many fuses at this power would not program after days.

This deliberately improperly programmed fuse was subsequently subjected to a slowly applied DC voltage ramp under current limited conditions (10M resistor in series). At 12 volts, the fuse resistance dropped to ~ 5000 ohms. The TEM photograph of this fuse is shown in Figure 13. It is obvious from this photograph that the reduced power condition has resulted in a fuse that has marginally programmed. That is, the gap created after programming is very narrow (approximately a few hundred angstroms) and subject to a voltage breakdown effect.

Fuses programmed per the recommended power levels will program rapidly with a wide gap as illustrated in the Mass Transport Models section. These fuses can be subjected to more that 100 volts and will undergo no change in electrical or physical condition.

As indicated in Figure 13, if a restricted amount of power is applied to a fuse, it is possible to create a very narrow gap. Under the presence of high voltage and extreme current limiting, it is then possible to force a voltage breakdown across the gap. It is postulated that this voltage discharge results in the establishment of a low conductivity relink at one or a few points of closest approach in the marginally blown gap. This specific structure could not be confirmed with the TEM study because even the TEM did not have resolution to examine microstructure at < 300 angstroms.

This mechanism of marginal programming is precluded from occuring in an actual PROM circuit because the programming specification, specifically the power and pulse widths, have been established to only generate well blown, wide gap fuses. That is, if the power actually reaching a fuse is lower than that required to blow the fuse properly, the fuse will not program in the time allotted for the programming pulse. The device, therefore, becomes a programming reject (won't program) and is scrapped.

In summary, the observation that a NiCr fuse can be marginally programmed has no connection with the reliability of the PROM circuit. Recall, to generate this anomaly, a power density four times less than the designed value and a program time $\sim 10^8$ times longer than the maximum specified programming time was required. Further, a voltage $\sim$10 times higher than the maximum that would be seen in an actual PROM, (with current limiting) was required to cause the relink.

Obviously, these observations and conclusions are based on NiCr fuses, PROM design, and control procedures as deployed by Harris. Contentions by others that a specific fuse material, NiCr or something else, is more or less reliable must be interpreted in perspective of the manufacturer's technology and not necessarily be construed as being generally representative.

LIFE TEST RESULTS

Life testing data of programmed PROMs has been accumulated for several years of production. The data in Table III summarizes those results. The total sample base represents a multiplicity of designs and configurations (0512, HPROM series 2nd state-of-the art GPROMs). These samples were selected from unburned in production runs that had passed the standard final test program and were programmed to data sheet programming procedure. The life test conditions are representative of typical applications (except for elevated temperature). The results indicate that the level of reliability of these PROM circuits is equivalent to circuits of similar complexity that do not utilize fusible links.

SUMMARY

(1) Conduction electrons in NiCr have a short mean-free path. This maximizes I^2R heating and precludes electromigration in the direction of electron flow as a fusing mechanism.

(2) Transmission electron microscopy is the only effective analytical tool to characterize the programmed fuse gap structure.

(3) NiCr fuses program by molten metal (nickel, chrome), ions moving in the presence of an electric field. The final structure resembles a frozen splash and is described by fluid dynamics.

(4) Thermal analysis coupled with empirical programmed fuse data indicate a threshold power density for fusing. If this power density is exceeded, which can be assured if the programming time utilized is as specified, the fuse gap will be wide and reliable. If this power density threshold is only matched, it is possible to create a marginal fuse.

(5) Life test results indicate programmed PROM reliability is equivalent to devices of the same complexity that do not utilize fusible links.

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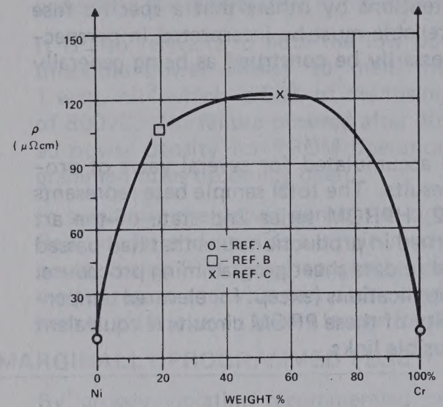
CONDUCTION PROPERTIES OF NiCr

- NICKEL AND CHROMIUM ARE TRANSITION METALS.
- INNER SHELL ELECTRONS CONDUCT, OUTER SHELL SHIELDS. HIGHER RESISTANCE.
- ALLOY EFFECT ENHANCES SHIELDING/RESISTIVITY.

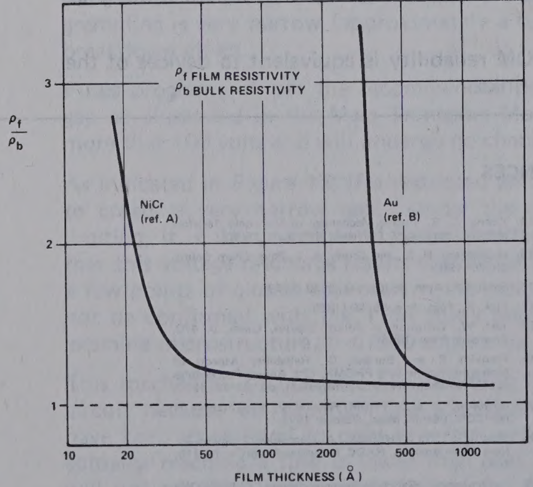


A – Handbook of Chemistry and Physics.
B – Thin Film Technology, R. W. Berry, et. al.
C – Japanese Metal Material Handbook, Y. Yamamoto, et. al.

Figure 1

FILM VS. BULK PROPERTIES

- SHORT MEAN FREE PATH LENGTH OF ELECTRONS
- BULK RESISTIVITY IN THIN FILM
- GOOD FILM REPRODUCIBILITY

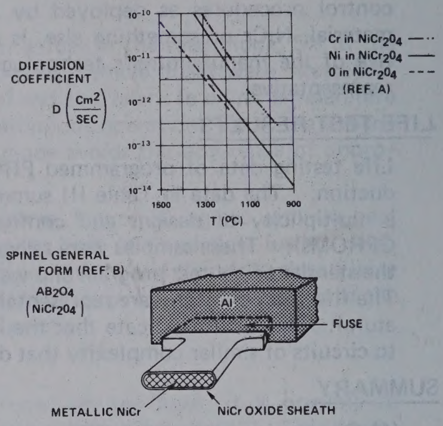


A – M. Nagata, et. al., Proc. Elec. Comp. Conf., 1969.
B – K. L. Chopra, Thin Film Phenomena, McGraw–Hill, 1969.

Figure 2

OXIDATION OF NiCr

- NiCr FORMS SELF LIMITING SKIN OXIDE
- SPINEL THICKNESS ≃ 20 Å
- PROMOTES RESISTOR STABILITY



Ref. A – "Mass Transport in Oxides," NBS Publ. 296, (1968).
Ref. B – A. F. Wells, "Structural Inorganic Chemistry", Oxford Press (1950).

Figure 3

SCANNING TRANSMISSION ELECTRON MICROSCOPY ANALYSIS OF FUSES

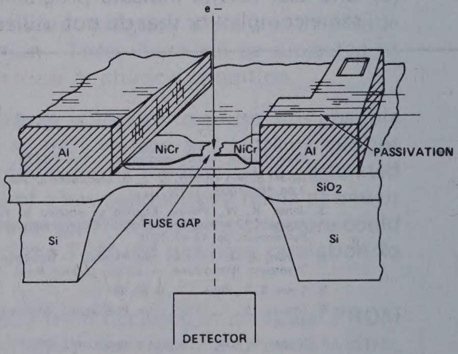
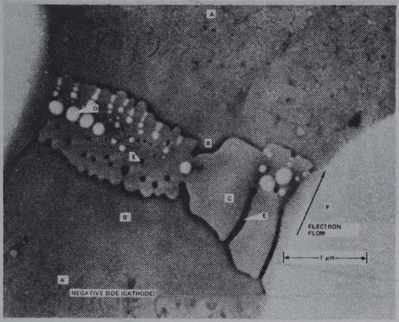


Figure 4

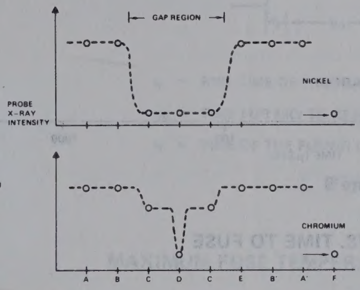
STEM PROGRAMMED FUSE

OGRAMMING CONDITIONS:
WER = 150 mW.
IE TO FUSE = 2 µSEC.


A
D
B
E
C
B'
E
F
ELECTRON FLOW
1 µm
A'
NEGATIVE SIDE (CATHODE)

POINT MICROPROBE ANALYSIS

– NiCr
– MELTED NiCr
– SiO2, CHROMIUM OXIDE
– SiO2
– DENSIFIED NiCr
– FIELD OXIDE (SiO2)



OTE: (A) "FROZEN SPLASH" EFFECT PROGRAMMING HAS MELTED NiCr IN GAP REGION.
(B) MASS TRANSPORT IN GAP.
(C) MASS ASYMMETRY TO NEGATIVE TERMINAL.

Figure 5

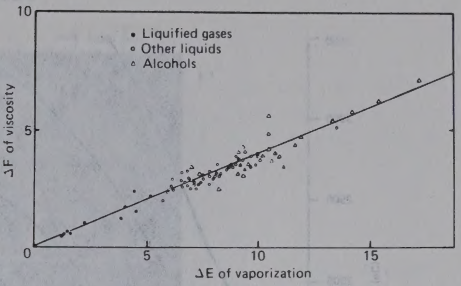


Fig. 11-24. Empirical relation between free energy of activation in liquids, ΔF, and energy of evaporation, ΔE, Rosevaere, Powell and Eyring.

TABLE II

Corrected ratio of energy of vaporization and activation for viscous flow

Metal	Average temp. °C.	ΔE_{vap} kcal.	ΔE_{visc} kcal.	$\frac{\Delta E_{vap}}{\Delta E_{visc}}$	$\frac{\Delta E_{vap}}{\Delta E_{visc}}\left(\frac{r_{ion}}{r_{atom}}\right)^3$
Na	500	23.4	1.45	16.1	2.52
K	480	19.0	1.13	16.7	3.41
Ag	1400	60.7	4.82	12.5	3.79
Zn	850	26.5	3.09	8.6	2.10
Cd	750	22.5	1.65	13.5	3.96
Ga	800	34.1	1.13	30.3	2.53
Pb	700	42.6	2.80	15.9	4.97
Hg	250	13.6	0.65	20.8	2.37
Hg	600	12.3	0.55	22.2	3.54
Sn	600	15.3	1.44	10.6	4.07
Sn	1000	14.5	1.70	8.6	3.30

From "Diffusion in Solids, Liquids, Gases", W. Jost.

Figure 7

TEMPERATURE PROFILE IN FUSE NECK FROM HEAT FLOW MODEL

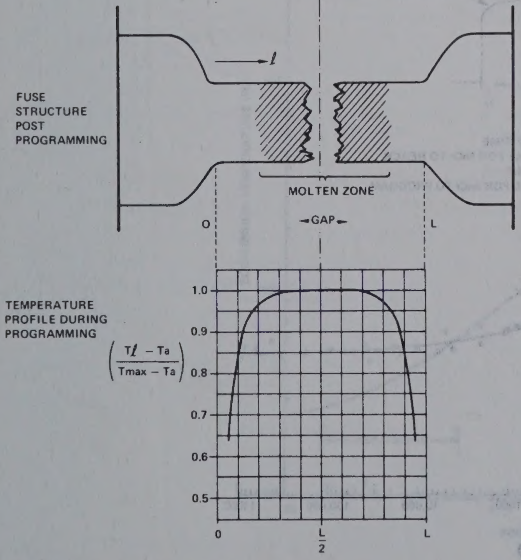
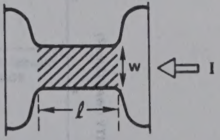

ℓ
FUSE STRUCTURE POST PROGRAMMING
MOLTEN ZONE
O
GAP
L
TEMPERATURE PROFILE DURING PROGRAMMING
(Tℓ – Ta) / (Tmax – Ta)
1.0
0.9
0.8
0.7
0.6
0.5
0
L/2
L

Figure 6

POWER DENSITY IN FUSE NECK REGION



$$\text{POWER DENSITY} = \frac{I^2\,(\rho_s \ell / w)}{(\ell \cdot w)}$$

$\rho_s \ell/w$ = RESISTANCE OF THE FUSE NECK (OHMS)

ρ_s = SHEET RESISTIVITY OF NICHROME (OHMS/SQ)

$\ell \cdot w$ = AREA OF FUSE NECK (MIL.^{2})

ℓ = LENGTH OF FUSE NECK

w = WIDTH OF FUSE NECK

I = PROGRAMMING CURRENT ($I = V_F/R_F$)

Figure 8

DYNAMIC HEATING OF NiCr FUSE VS. POWER DENSITY

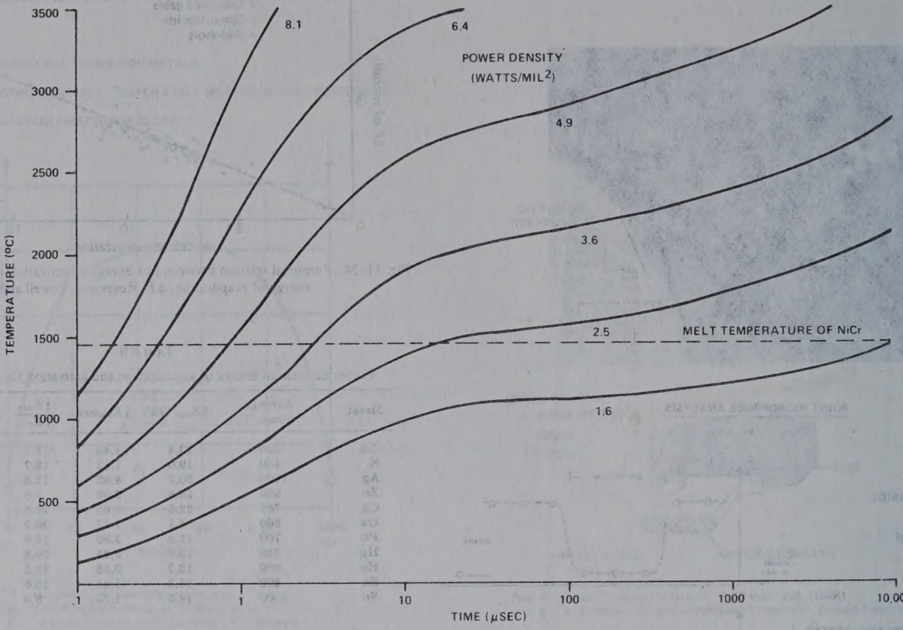


Figure 9

POWER DENSITY VS. TIME TO FUSE

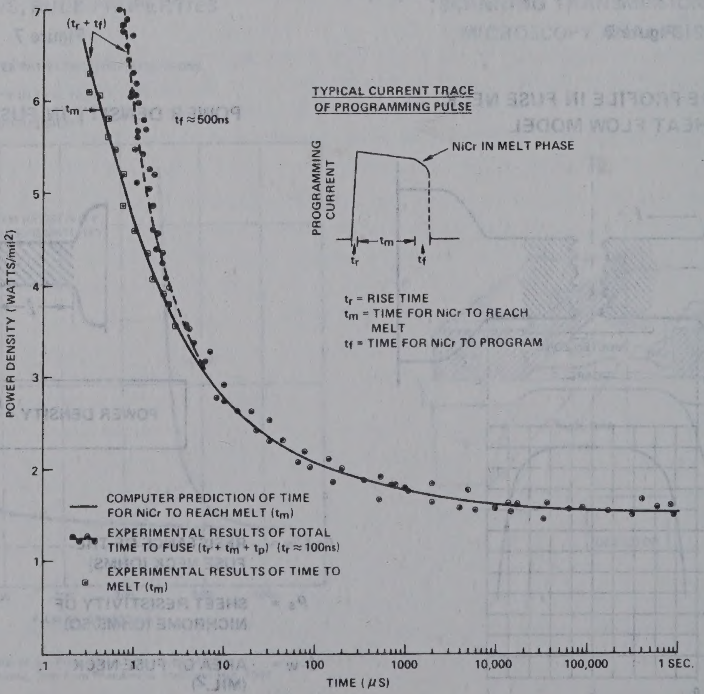
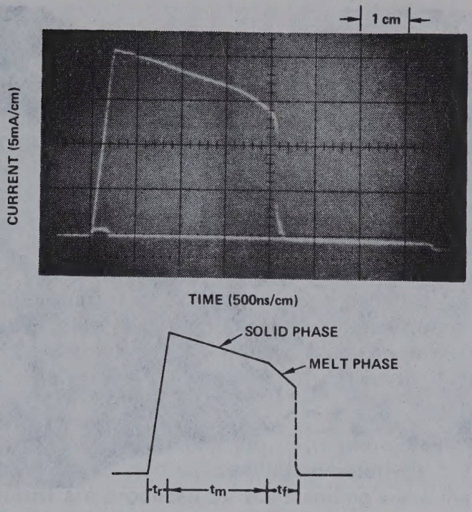


Figure 10

PROGRAMMING PULSE CHARACTERISTICS



t_r = RISE TIME OF PROGRAMMING PULSE

t_m = TIME FOR NiCr TO REACH MELT

t_f = TIME OF THE FUSING EVENT (IONIC MASS TRANSPORT)

Figure 11

MAXIMUM FUSE TEMPERATURE VS. POWER DENSITY

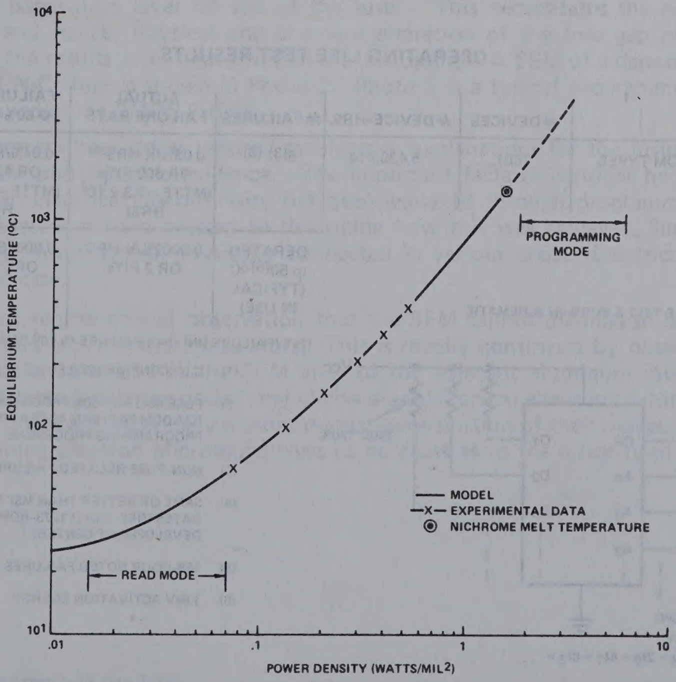
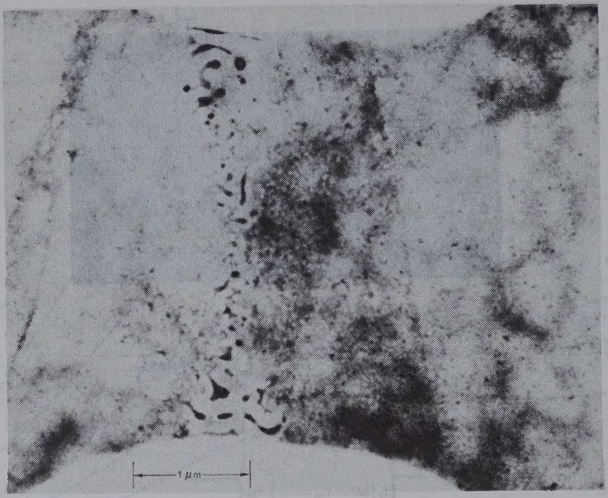


Figure 12

MARGINALLY PROGRAMMED TEST VEHICLE FUSE

PROGRAMMING CONDITIONS:
POWER DENSITY = 1.5 WATTS/MIL^2
TIME TO FUSE = 300 SEC.



FORCED RELINK OF MARGINALLY PROGRAMMED TEST FUSE

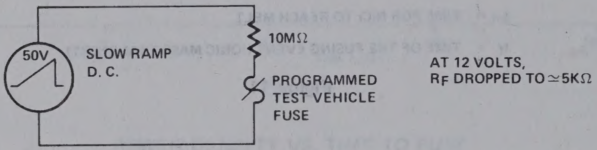

50V
SLOW RAMP
D. C.
10MΩ
PROGRAMMED
TEST VEHICLE
FUSE
AT 12 VOLTS,
R_F DROPPED TO ≃5KΩ

Figure 13

OPERATING LIFE TEST RESULTS

	#DEVICES	#DEVICE-HRS.	#FAILURES	ACTUAL FAILURE RATE	FAILURE RATE @ 60% C. L. (1)
ALL PROM TYPES	7681	15,439,914	5$^{(3)}$ (5)	0.03%/K HRS$^{(4)}$ OR 300 FITs (MTTF - 3.3 x 10^6 HRS)	0.04%/K HRS$^{(4)}$ OR 400 FITs (MTTF - 2.5 x 10^6 HRS)
			DERATED to 50$^{(6)}$°C (TYPICAL IN USE)	0.0002%/K HRS OR 2 FITs	0.00026%/K HRS OR 2.6 FITs

1FIT (FAILURE UNIT) = 1 FAILURE IN 10^9 DEVICE-HOURS

(1) C.L. (CONFIDENCE LEVEL)

(2) FUSE MATRIX: 50% PROGRAMMED RANDOM PATTERN AS PER PRESCRIBED PROGRAMMING PROCEDURE.

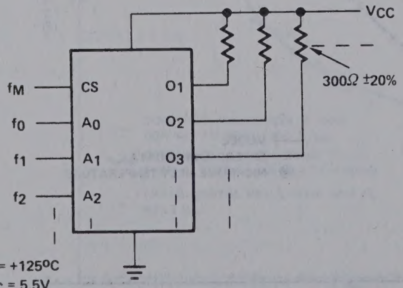
(3) NON-FUSE RELATED FAILURES

(4) SAME OR BETTER THAN MSI FAILURE RATES (REF. MDFR 1273-ROME AIR DEVELOPMENT CENTER)

(5) 168-HOUR NOTED FAILURES

(6) 1.0eV ACTIVATION ENERGY

LIFE TEST & BURN-IN SCHEMATIC


VCC
300Ω ±20%
f_M
f_0
f_1
f_2
CS
A0
A1
A2
O1
O2
O3

T_A = +125°C
V_{CC} = 5.5V
1KHz = f_M = $2f_0$ = $4f_1$ = $8f_2$ = ...

Table III

Microscopic Observations of Fuses

Beauty is in the eye of the beholder. When the eye is attached to a microscope, beauty can take strange forms. Nowhere is this more evident than when the realm of blown fuses in PROMs is entered. This paper will ''shed some light'' on the misinformation which has been generated regarding the nature of NiCr fuse gaps as viewed by different microscopic techniques.

WHAT YOU SEE OPTICALLY

Using a light microscope to examine fuse structures is a futile exercise because the wavelength of visible light is within an order of magnitude of the total fuse dimensions. The microstructure of the fusing process reaction zone contains formations that are smaller than a wavelength of light. In addition, the overlying passivation acts like an aberrant lens and distorts the image which is visible. The most that can be reliably ascertained regarding the nature of a fuse with optical microscopy is whether the fuse is physically present or absent.

Photo 1* illustrates this physical phenomenon. The photograph is of photoresist after exposure to ultraviolet light and normal developing solutions. The ridges in the vertical portion of the photoresist are produced by the standing wave that is present due to reflection of the U.V. light from the oxidized silicon during resist exposure. As can be seen, the ridge pattern has a wavelength λ of the incident light (λ = 3650nm), the index of refraction of the photoresist is $n = 1.58$; thus, for visible light on the order of λ= 5000nm, less than ten wavelengths are needed to span the fuse neck region.

WHAT THE SCANNING ELECTRON MICROSCOPE SHOWS

The SEM is a useful analytical tool for many applications. This is amply demonstrated by Photo 1 that showed us the standing wave pattern in photoresist.

The SEM does have limitations in observing fuses, however. For one, it cannot ''see'' through the passivation layer on top of the fuse. This necessitates the removal of the glassivation and hence, physical and chemical alteration of the fuse gap microstructure. In addition, the results after depassivation are misleading. A SEM of a depassivated typical programmed NiCr fuse is shown in Photo 2. Photo 3 is a typical programmed polysilicon fuse as deployed in the CMOS PROM.

Previous observers have never reached satisfactory explanations for the fusing phenomena based on SEM photographic evidence. The important facts to consider here are that for both fuses, an electrical discontinuity has been achieved through programming. In both cases, the observer is hard pressed to determine how this was achieved, for his eyes tell him that both fuses appear physically connected in various areas. Electrically, we know this is not the case.

This brings us to the crucial observation that the SEM cannot distinguish between electrical conductors and electrical insulators. This is readily confirmed by observing the lack of differentiation afforded in the SEM view of the adjacent aluminum interconnect (an excellent conductor) and the underlying silicon dioxide (an excellent insulator). Since both of the above fuses are electrically discontinuous, some portion of their makeup is insulative, but the Scanning Electron Microscope gives us no clues as to the integrity of the insulator.

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*Photos found on pages 7-25 thru 7-27.

TRANSMISSION ELECTRON MICROSCOPY ANALYSIS OF FUSES

A fresh approach in fuse analysis has been developed to view a fuse without disturbing the conditions present at the time of programming. Basically, the technique uses a thinned specimen PROM with the fuses sandwiched between the two normal glass sheets found on the PROM (the passivation above and thermal oxide below) with the underlying silicon substrate etched away as shown in Photo 4 . Now standard high resolution bright and dark field TEM (Transmission Electron Microscopy) analytical techniques are available.

Photo 4 is a TEM photograph of a typical programmed NiCr fuse. Now we can see which regions of the blown fuse are conductive metal and which are not. The well-defined darkened regions are metallic while the overlying gray, which is all that was seen by SEM, has proven by electron diffraction analysis to be a stable insulating oxide compound with crystalline order that resembles a $NiCr_2O_4$ spinel. The surrounding region of high transmission are characteristic of the undisturbed passivation and underlying thermal SiO_2.

Therefore, Transmission Electron Microscopy has the capability of determining the true chemistry of programmed NiCr fuses.

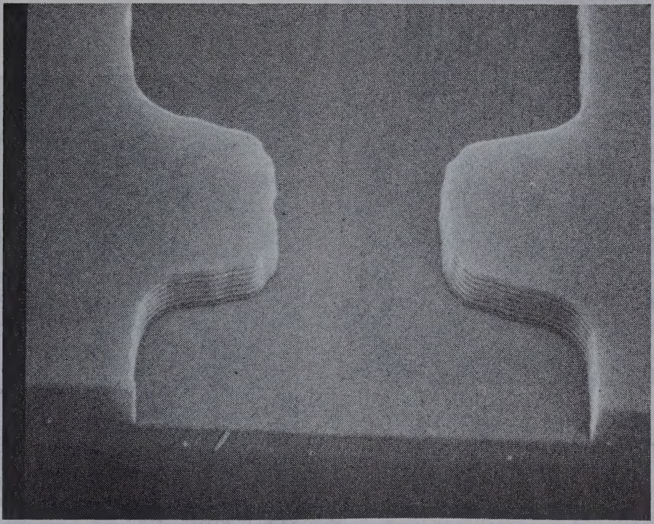


PHOTO 1A

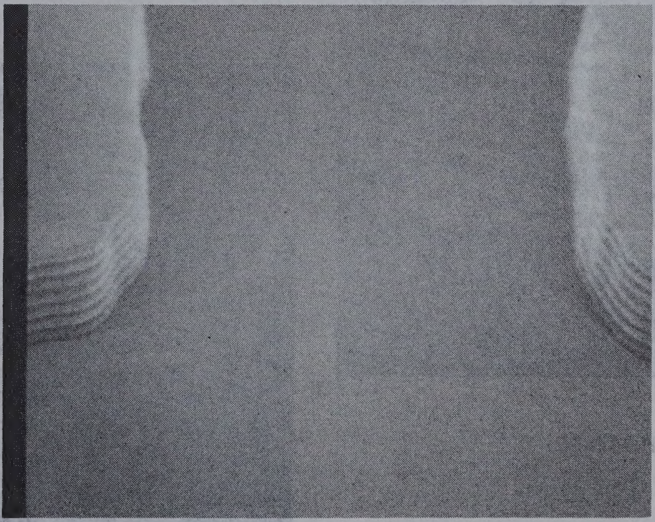


PHOTO 1B

SEM Photographs of Programmed Fuses

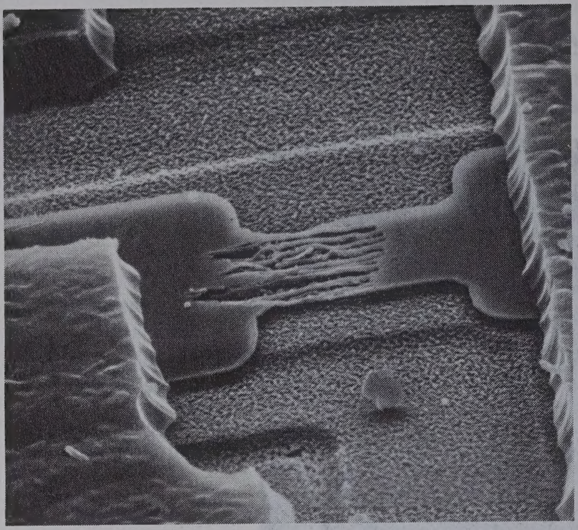


PHOTO 2A

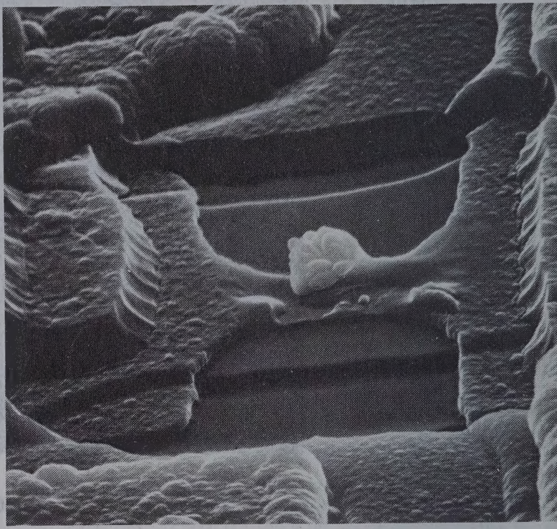


PHOTO 3A

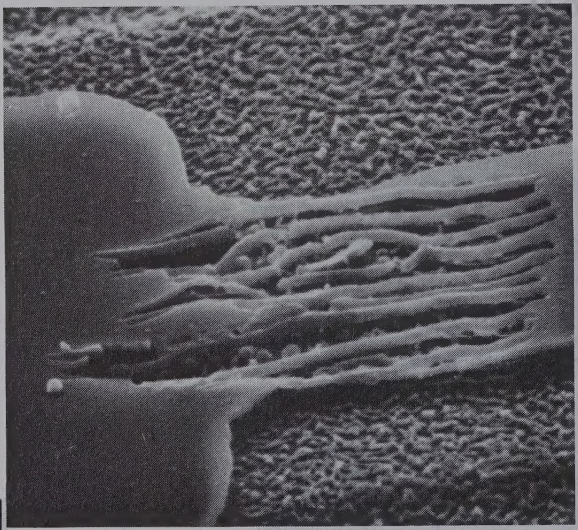


PHOTO 2B

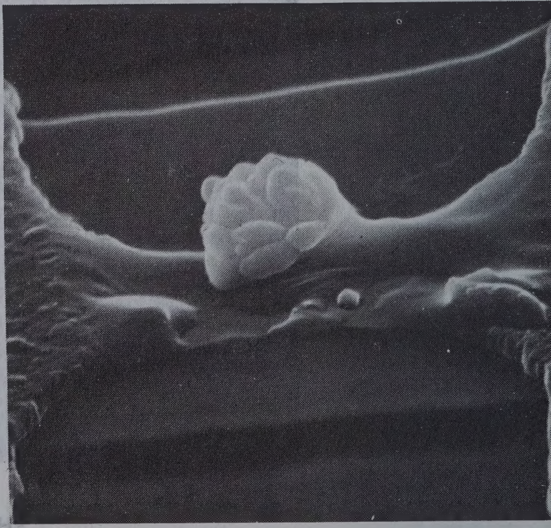


PHOTO 3B

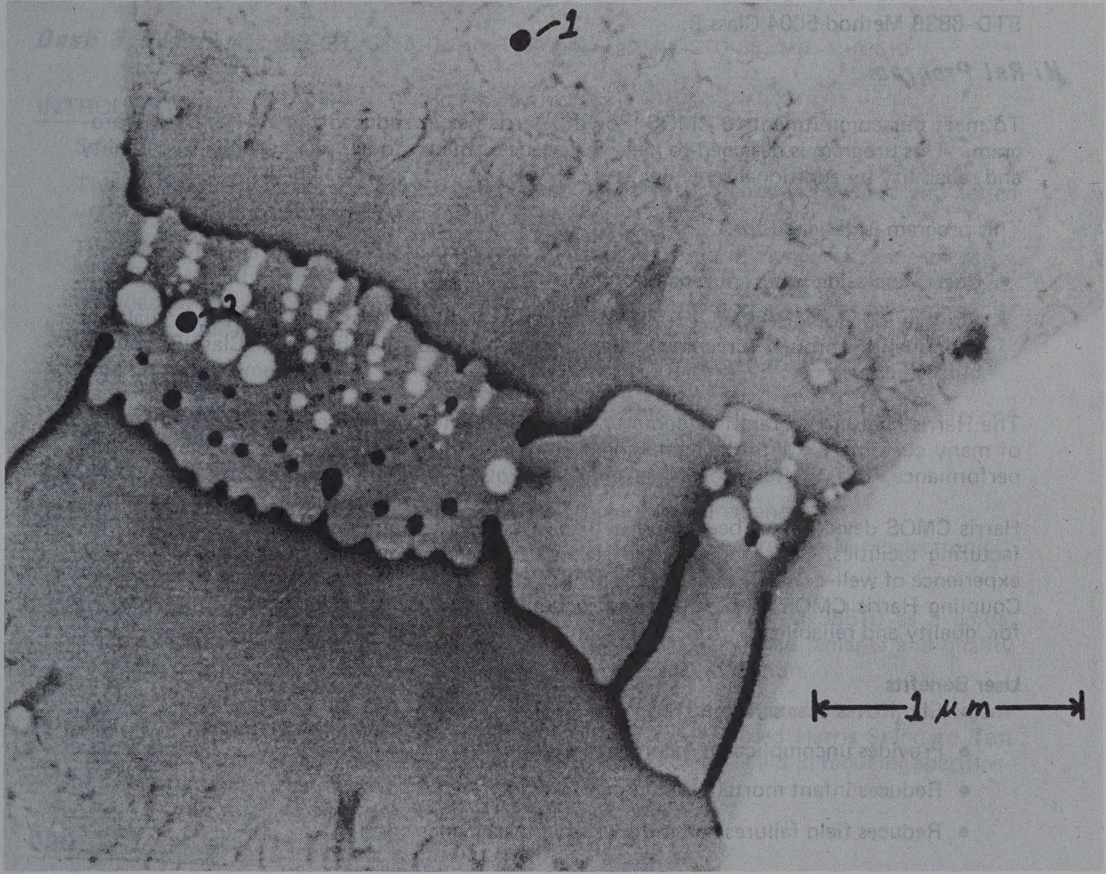


PHOTO 4

Reliability Screening Programs

Facility Qualification

Harris is closely attuned to the requirements of military quality and reliability manufacturing programs. Our facilities and its quality plan is well accepted at all major companies. In addition, we have JAN qualification in the Bipolar Memory area and have JAN qualifications in process on CMOS Memory and Analog products.

MIL-STD-883B-Class B (Dash 8)

As a special service to users of Hi-Rel products Harris makes instantly available high reliability on many of our product lines. Simply by adding its postscript -8 to appropriate Harris part numbers "off the shelf" delivery can be obtained of products screened to MIL-STD-883B Method 5004 Class B.

Hi-Rel Program

To meet our commitment to CMOS growth, Harris has introduced the Hi-Rel Dash 8 program. This program is designed to meet the needs of the customer seeking enhanced quality and reliability by additional screening steps.

This program is designed for:

- Customers using a current reliability add-on program.
- For the individual seeking a trade-off between additional cost and improved reliability and quality through screening - Harris gives a broad selection from Class B flow to burn-in only.

The Harris Hi-Rel Program is a comprehensive program aimed at serving the various needs of many customers. With the increasing need for improved IC systems mean time to failure performance, the Hi-Rel program assures high quality and reliability of CMOS circuits.

Harris CMOS devices have been produced for over 6 years in modern state of the art manufacturing facilities. Our implemented second and third generation mask designs with the experience of well-controlled processes, results in standard products with built-in reliability. Coupling Harris CMOS with a Hi-Rel Program will result in an enhanced combinations for quality and reliability.

User Benefits

- Eliminates user screening programs
- Provides uncomplicated incoming inspection
- Reduces infant mortality and board rework
- Reduces field failures and unnecessary maintenance costs

Quality

In theory, parts tested 100 percent should upon receipt at the user's site be 100 percent good. Due to volume production there may exist a small percentage of parts which escape 100 percent tests. The AQL or LTPD outgoing sampling plans at Harris have been very successful in stopping the DOA's (Dead on Arrival). For the user with complex systems using large quantities of products, a quality enhancement can be tailored into your specific Hi-Rel Program by choosing tightened sampling plans. The tightened quality test plan ensures close maintenance of the improved quality level through careful product segregation and retesting.

Reliability

Experience and perfected process controls have built reliability into a standard Harris CMOS product. Reliability cannot be tested into a part. Quality level may be improved by retesting and tighter sampling plans. However, reliability is improved by proper design and observance of sound ground rules, controlled processes and finally by stress testing to confirm claimed reliability performance. The Hi-Rel program offers a varied mix of stress tests to compress time and weed out devices subject to infant mortality. The equivalent early life failures are removed by the various screens such as temperature cycling, stabilization bake, burn-in and high temperature functional testing. Some or all of these stress tests will remove early failures and thus improve overall system reliability.

Dash 8 Program – MIL-STD-883B; Off-the-Shelf Delivery; MIL-STD-883/MIL-M-38510,

INTRODUCTION

Statement of Scope

This section establishes the detail requirements for HARRIS circuits screened and tested under the Product Assurance Program.

The Harris DASH 8 Devices pass the screening requirements of the latest issue of MIL-STD-883B, Method 5004, Class B, and the requirements as specified in this document. Included in this section are the quality standards and screening methods for commercial parts which must perform reliably in the field.

Applicable Documents

The following Military documents form a part of this section to the extent referenced herein and provide the foundation for Harris Products Assurance Program.

MIL-M-38510	"General Specification for Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-833B	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"

Harris maintains a Product Assurance Program (PAP) using MIL-M-38510 as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

The DASH 8 Program will also be found useful by those Harris customers who must generate their own procurement specifications. Use of the enclosed Harris Standard Test Tables, Test Parameters, and Burn-In as described in Section 4 will aid in reducing specification negotiation time.

PRODUCT ASSURANCE AT HARRIS

Our Product Assurance Department strives to assure that the quality and reliability of products shipped to customers is of a high level and consistent with customer requirements. During product processing, there are several independent visual and electrical checks performed by Reliability and Quality Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met. The system and procedures used and implemented are in accordance with MIL-M-38510, MIL-Q-9858A, MIL-STD-883B, MIL-C-45662 and MIL-I-45208.

The Harris Semiconductor Products Division Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality.

HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
①	Internal Visual	2010 Cond. B.
②	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
③	Temperature Cycling	1010 Cond. C
④	Constant Acceleration	2001 Cond. E; Y1 plane
⑤	Seal: Ⓐ Fine Ⓑ Gross	1014 Cond. A or B 1014 Cond. C
⑥	Initial Electrical	Harris Specifications
⑦	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
⑧	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
⑨	External Visual	2009 Sample Inspection
⑩	Lot Acceptance	Table I, Group A Elect. Tests

NOTE: **Group A, Subgroup 1, 2, 3, & 9 for Bipolar–Table 1, Subgroup 2 & 10 for CMOS.**

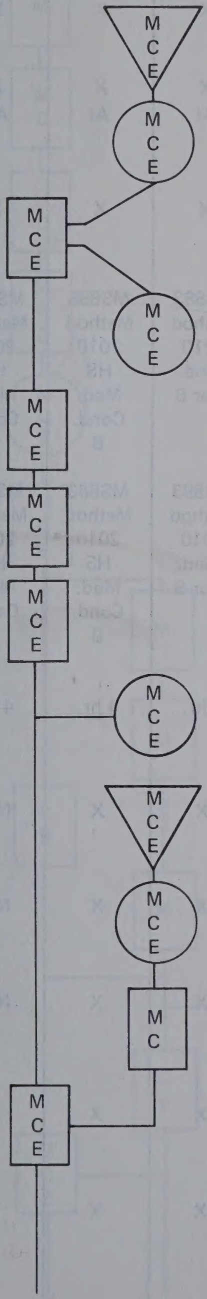
Traceability:	All devices are assigned date code identification that provides traceability back to the inspection lot.
Branding:	All devices are branded with the HX-XXXX-8 and EIA date code.
Aged Products:	Product that has been held for more than 24 months will be reinspected to group A inspection requirements prior to shipment.
Additional Requirements:	Attributes data on Group A Lot Acceptance will be supplied upon request.

Generic data from Harris' Reliability Add-On Program is available upon request. The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all products families in manufacturing. This program provides life test performance results to fullfill reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

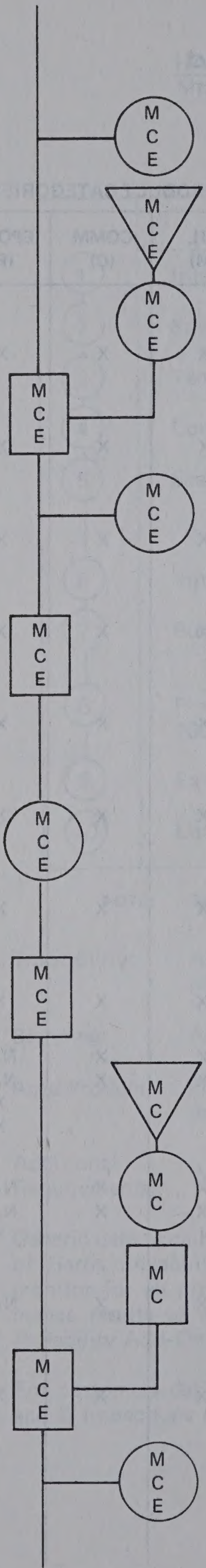
For customers desiring Lot Qualification, Harris Semiconductor will perform Group A, B, C and D inspections to MIL-STD-883, Method 5005 as defined herein for an additional charge.

Standard Products Screening and Inspection Procedure

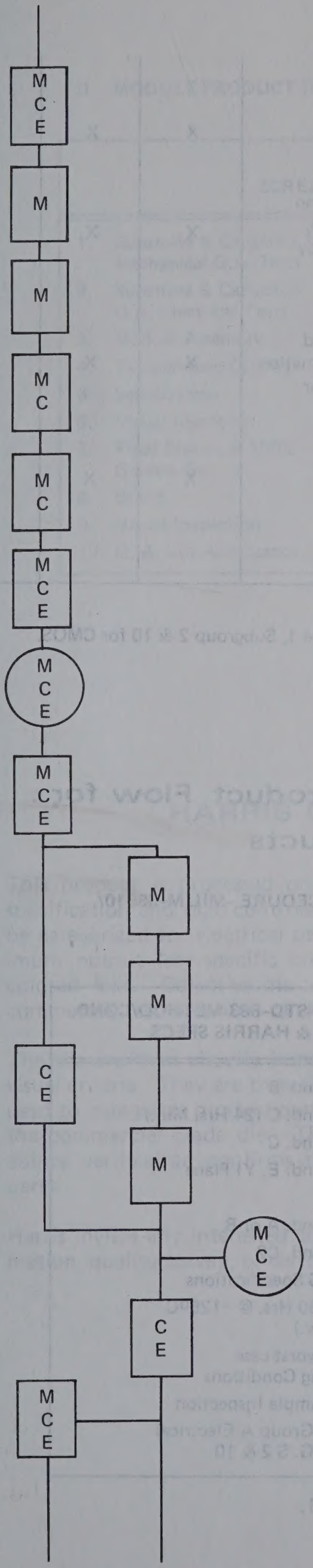
OPER. SEQ.



OPER. DESCRIPTION	PRODUCT CATEGORIES MIL (M)	PRODUCT CATEGORIES COMM (C)	PRODUCT CATEGORIES EPOXY (E)
Incoming Material Silicon and Chemical Procurement.	X	X	X
Q.C. Incoming Inspection. Materials are Inspected for Conformance to Specified Requirements.	X	X	X
Manufacturing Wafer Fabrication	X	X	X
QC • DIH_2O & Gas Monitor • SEM Process Control • Wafer Process Control	X	X	X
Manufacturing, Wafer Electrical Probe (100%)	X	X	X
Manufacturing, Wafer Scribe, Break (100%)	X	X	X
Manufacturing Dice Screen (100%)	X	X	X
QA Dice Inspection Control	X	X	X
Preform Procurement	X	X	N/A
Package Procurement	X	X	N/A
Leadframe Procurement			X
Epoxy Compound Procurement			X
Q.C. Preform Inspection	X	X	N/A
Q.C. Package Inspection	X	X	N/A
Q.C. Leadframe Inspection			X
Manufacturing Package Clean	X	X	N/A
Manufacturing Die Mounting	X	X	X



QA Die Mount Control (continuous sampling) • Visual Die Inspection	X	X	X
Bond Wire Procurement	X	X	X
Q.C. Wire Inspection (receiving)	X	X	X
Manufacturing Wire Bonding	X Al	X Al	X Au
QA Bond Control (continuous sampling) • Visual Die & Bond Inspection • Wire and Pull Test	X	X	X
Manufacturing Pre-Seal Screen (100%)	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
QA Pre-Seal Inspection Lot Acceptance	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
Preseal Bake Per MS-883, Method 1008, Cond. C	8 hr.	4 hr.	4 hr.
Package Lid Procurement	X	X	N/A
Package Lid Inspection	X	X	N/A
Package Lid Clean	X	X	N/A
Package Seal/Encapsulation	X	X	X
QA Package Seal/Encapsulated Control (continuous sampling)	X	X	X



Stabilization Bake MS-883, Method 1008, Cond. C.	24 hr.	8 hr.	8 hr.
Temperature Cycle, MS-883, Method 1010, Cond. C,	X	X	N/A
Centrifuge, MS-883, Method 1010, (Y1) Plane 30 KG's min.	100%	X	N/A
Fine Leak, MS-883, Method 1014	100%	X	N/A
Gross Leak, MS-883, Method 1014	100%	X	N/A
Frame Removal & Loading Units In Carriers/Sticks	X	X	X
Final QA Lot Inspection, MS-883 Method 1014 • Fine & Gross Leak • Visual/Mechanical Inspection	X	X	X
Group A Initial Tests Table 1	X	X	X
Brand Device Type/Date Code Serialize, If Applicable	X	N/A	N/A
Burn-In (100%), MS-883, Method 1015	Classes A/B Products	N/A	N/A
Group A Final Test $^{1.}$ (Worst Case Oper. Cond.)	X	N/A	N/A
QA Acceptance Elec. Testing • Visual/Mechanical Method 2009 Lot Sampling	X	X	X
Brand Devices Type/Date Code	N/A	X	X
Controlled Inventory	X	X	X

M C E	Package for Shipment	X	X	X
M C E	Quality Conformance Inspection Group B/C/D Testing, MS-883, Method 5005, Periodically or by Customer P.O. Request	X	X	X
M C E	QA Plant Clearance • Final Visual of Marking and Physical Quantity, Conformation of Product by Inspection or Sample Test	X	X	X
M C E	Ship to Customer	X	X	X

NOTE: 1. Group A, Subgroup 1, 2, 3, & 9 for Bipolar—Table 1, Subgroup 2 & 10 for CMOS.

Harris Semiconductor Dash 8 Product Flow for : CMOS Module Products

I. LEADLESS CHIP CARRIER 100%, SCREENING PROCEDURE -MIL M-38510/ MIL-STD-883, METHOD 5004 CLASS B

SCREEN	MIL-STD-883 METHOD/COND. & HARRIS SPECS.
1. Internal Visual	2010 Cond. B
2. Stabilization Bake	1080 Cond. C (24 Hrs. Min.)
3. Temperature Cycling	1010 Cond. C
4. Constant Acceleration	2001 Cond. E. YI Plane
5. Seal:	
A-Fine	1014 Cond. A or B
B-Gross	1024 Cond. C2
6. Initial Electrical	HARRIS Specifications
7. Burn-In Test	1015, 160 Hrs. @ +125°C (or Equiv.)
8. Final Electrical 100% Go-No-Go	Test at worst case Operating Conditions
9. External Visual	2009, Sample Inspection
10. Q. A. Lot Acceptance	Table I, Group A Electrical Tests S. G.'S 2 & 10

NOTE: Group A, Subgroup 1, 2, 3, & 9 for Bipolar-Table 1, Subgroup 2 & 10 for CMOS

II. MODULE PRODUCT 100% SCREENING PROCEDURE/HARRIS SPECIFICATION.

SCREEN	MIL-STD-883 METHOD/COND. & HARRIS SPECS.
1. Substrate & Capacitor Visual/ Mechanical Q.A. Tests	HARRIS Specifications
2. Substrate & Capacitor Q.A. Electrical Tests	HARRIS Specifications
3. Module Assembly	HARRIS Specifications
4. Temperature Cycling	1010.2 (5 Cycles)
5. Serialization	-
6. Visual Inspection	HARRIS Specifications
7. Final Electrical 100% Go-No-Go	+25°C DC Tests -Q. A. Monitor
8. Brand	-
9. Visual Inspection	HARRIS Semiconductor
10. Q. A. Lot Acceptance	HARRIS Semiconductor

HARRIS Commercial Grade Products

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to a modified Class B visual criteria. They are then assembled in packages on a controlled assembly line. The ink used to categorize product performance, such as the green ink, might not be removed from the commercial grade die. This ink has been chemically characterized as inert and reliability verification confirms there is no effect on performance or operating life of the parts.

Harris invites any interested customer to review our assembly flow and facilities for information, quality survey, or certification.

Table I — Group A Electrical Tests[1]

SUBGROUP [2]	DASH 8 & 2 LTPD * MIL-PRODUCT	LTPD* COMM. PRODUCT
Subgroup 1 Static Test at 25°C	5	5
Subgroup 2 Static Test at Maximum Rated Operating Temperature	7	—
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	7	—
Subgroup 4 Dynamic Tests at 25°C	5	5
Subgroup 5 Functional Tests at 25°C	5	5
Subgroup 6 Functional Tests at Maximum and Minimum Rated Operating Temperatures	10	15
Subgroup 7 Switching Tests at 25°C	7	10

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document or specification sheet. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test to satisfy Group A requirements.
2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed.
3. Group A, Subgroup 1, 2, 3, & 9 for Bipolar—Table 1, Subgroup 2 & 10 for CMOS.

Table II — Group B Tests (Lot Related)[1]

TEST	MIL-STD-883 METHOD	CONDITION	LTPD*
Subgroup 1 Physical Dimensions	2016		2 Devices (No Failures)
Subgroup 2 Resistance to Solvents	2015		4 Devices (No Failures)
Subgroup 3 Solderability [3]	2003	Soldering Temperature of 260 ± 10°C	15
Subgroup 4 Internal Visual and Mechanical	2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document.	1 Device (No Failures)
Subgroup 5 Bond Strength[2] (1) Thermocompression (2) Ultrasonic or Wedge (3) Beam Lead	2011	(1) Test Condition C or D (2) Test Condition C or D (3) Test Condition H	15

NOTES:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.

2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.

3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

4. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note — Table 1 *

Table III — Group C (Die Related Tests)

TEST	MIL-STD-883		LTPD*
	METHOD	CONDITION	
Subgroup 1			
Operating Life Test	1005	Test Condition to be specified (1000 Hrs)	5
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 2			
Temperature Cycling	1010	Test Condition C	15
Constant Acceleration	2001	Test Condition E Y_1 Axis	
Seal (a) Fine (b) Gross [2].	1014	As Applicable	
Visual Examination	1.		
End Point Electrical Parameters		Table I – Subgroup 1	

NOTES:

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
3. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note - Table 1 *

Table IV — Group D (Package Related Tests)

TEST	MIL-STD-883B		LTPD*
	METHOD	CONDITION	
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2[4]			
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
Seal	1014	As Applicable	
(a) Fine			
(b) Gross[6]			
Subgroup 3[1]			
Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum.	15
Temperature Cycling	1010	Test Condition C, 100 Cycles Minimum	
Moisture Resistance	1004	Omit Initial/Conditioning and Vibration	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross[6]			
Visual Examination	2.		
End Point Electrical Parameters		Table I — Subgroup 1	
Subgroup 4[1]			
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross[6]			
Visual Examination	3.		
End Point Electrical Parameters		Table I — Subgroup 1	
Subgroup 5[4]			
Salt Atmosphere	1009	Test Condition A	15
Seal	1014	As Applicable	
(a) Fine			
(b) Gross			
Visual Examination			

NOTES:

1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1004.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Electrical reject devices from that same inspection lot may be used for samples.
5. Visual examination shall be in accordance with method 1009.
6. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
7. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1 *

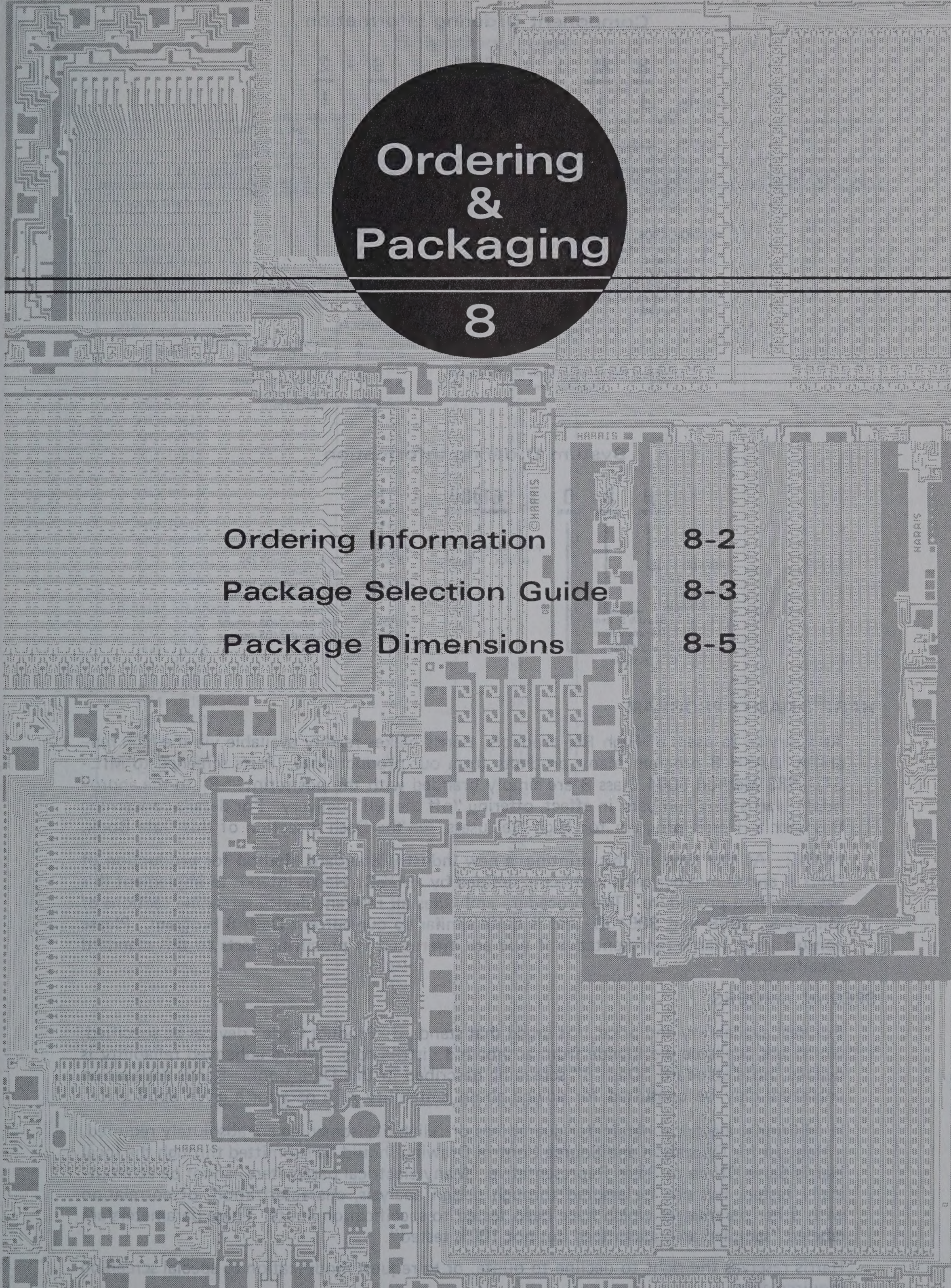
Section 4. Burn-In Circuit Diagrams

MIL-STD-883B, method 1015.2, paragraph 1, states, "The Burn-In test in performed for the purpose of screening or eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations which cause time and stress dependent failures. In the absence of Burn-In, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to stress microcircuits at or above maximum rated operating conditions or to apply equivalent screening conditions which will reveal time and stress dependent failure modes with equal or greater sensitivity without impairing long term reliability of the Burn-In surviving microcircuits.

Typically a dynamic type of Burn-In is preferred at Harris because of its worst case conditions. Static Burn-In is applied only where there is a specific customer requirement.

Capability exists for +125°C through +150°C Burn-In usually at HARRIS option. This enables higher throughput of devices by performing, for an example, a +150°C, 80-hour Burn-In which is equivalent to the standard +125°C, 160-hour cycle.

Actual Burn-In circuits are available on request through Harris field sales office and may include a variety of schematics, due to the differences in Burn-In oven systems, all of which are functionally equivalent with regard to the Burn-In objectives.



Ordering & Packaging

8

Ordering Information 8-2

Package Selection Guide 8-3

Package Dimensions 8-5

Component Ordering Information

H M 1 - 6514 B - 2

PREFIX:
- H - Harris

FAMILY:
- A - Analog
- C - Communications
- D - Digital
- I - Interface
- M - Memory

PACKAGE CODE:
- 0 - Chip Form
- 1 - Ceramic
- 3 - Epoxy
- 4 - Leadless Carrier
- 5 - Substrate and leadless assemby
- 9 - Flatpack

PART NUMBER:
- 0XXX - Diode Matrices
- 61XX - Microprocessor
- 63XX - CMOS ROMs
- 64XX - CMOS Interface
- 65XX - CMOS RAMs
- 66XX - CMOS PROMs
- 67XX - CMOS EPROMs
- 76XX - Bipolar PROMs

VERSION*

CMOS
- A - 10 Volt version
- B - High speed - Low power
- C - Commercial grade
- Blank - Standard product

BIPOLAR
- A - Redesign - Two level metal
- P - Power Down version
- R - Latched outputs
- RP - Latched outputs with Power Down option
- Blank - Standard parts

TEMPERATURE:
- 2 - -55°C to +125°C
- 5 - 0°C to +75°C
- 6 - 100% 25°C Probe
- 8 - Dash 8 Program Mil. Std. 883B
- 9 - -40°C to +85°C

* All versions may not be applicable to every product. Check data sheet.

System Ordering Information

H B 0 - 61000 - 1

PREFIX:
- H - Harris

FAMILY:
- B - Board & Systems
- Z - Documentation

PACKAGE CODE:
- 0 - Systems

PART NUMBER:
- 61XXX - Systems

OPTION:
- 61000-1 - Basic system with 256 words memory
- 61000-4 - Basic system with 1024 words memory & parallel I/O port
- 61001-1 - 4096 word CMOS memory
- 61001-2 - 2048 word CMOS memory

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products, Harris makes readily available via the high reliability DASH 8 program many products from our product lines. Parts screened to MIL-STD-883 Method 5004 Class B are simply branded with the postscript "-8" to the appropriate Harris part numbers, in effect, offering "off the self" delivery. For details concerning this special Harris program for High Rel users, see the Dash 8 section of this Data Book.

NOTE: At the time of this printing, a new industry Standard Method for production of Class B and C microcircuits was being defined by JEDEC. Harris intends to implement this new standard procedure. The procedure embodies all relevant device screening sections of Mil. Spec. 883B and 38510D, and is quite similar to our current Dash 8 program. Please consult your Harris representative if you are interested in procuring parts to this standard specification.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Many electrical parameters cannot be economically tested, but can be assured through design analysis, characterization, or correlation with other parameters which have been tested to specification limits. These parameters are labeled "sampled and guaranteed but not 100% tested".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

Selection Guide

PRODUCT	1* CERDIP	3* EPOXY	4* LEADLESS††	9* CERPACK††
Diode Matrices				
HM-0104	4U			9H
HM-0168	4U			9H
HM-0186	4U			9H
HM-0198				8C
HM-0410	4U			9H
Interface Products				
HD-4702	4Z	3L	LA	
HD-6402	5H	3J	LG	
HD-6408	4K	3F	LG	
HD-6409	4L	3N		
HD-6431	4Z	3L	LA	
HD-6432	4N	3D	LA	
HD-6433	4Z	3L	LA	
HD-6434	4K	3F	LG	
HD-6435	4L	3N	LG	
HD-6436	4L	3N	LG	
HD-6440	4N	3D	LA	
HD-6495	4Z	3L	LA	
HD-15530	4K		LG	8L
HD-15531	5H		LG	
Bipolar Memory				
HD-6600	4D			
HM-7602	4Z	3L		8B
HM-7603	4Z	3L		8B
HM-7608	4K	3F		8F
HM-7610	4Z	3K		8B
HM-7610A	4Z	3L		8B
HM-7611	4Z	3K		8B
HM-7611A	4Z	3L		8B
HM-7616	4K			8L
HM-7620	4Z	3K		8B
HM-7620A	4Z	3K		8B
HM-7621	4Z	3K		8B
HM-7621A	4Z	3K		8B
HM-7640	4K	3F		8F
HM-7640A	4K	3F		8F
HM-7641	4K	3F		8F
HM-7641A	4K	3F		8F
HM-7642	4N	3D		8C
HM-7642A	4N	3D		8C
HM-7642P	4N	3D		8C
HM-7643	4N	3D		8C
HM-7643A	4N	3D		8C
HM-7643P	4N	3D		8C
HM-7644	4P	3K		8C

*These package numbers to be used in product ordering. Other numbers shown in Selection Guide and drawings are internal package numbers.

††Contact factory for latest availability of devices in these packages.

Selection Guide

(Continued)

	1*	3*	4*	9*
PRODUCT	CERDIP	EPOXY	LEADLESS††	CERPACK††
HM-7647R	4K	3F		8F
HM-7648	4L	3N		8D
HM-7649	4L	3N		8D
HM-7680	4K	3F		8F
HM-7680A	4K	3F		8F
HM-7680R	4K	3F		8F
HM-7680P	4K	3F		8F
HM-7680RP	4K	3F		8F
HM-7681	4K	3F		8F
HM-7681A	4K	3F		8F
HM-7681R	4K	3F		8F
HM-7681P	4K	3F		8F
HM-7681RP	4K	3F		8F
HM-7684	5E	3D		8H
HM-7684P	5E	3D		8H
HM-7685	5E	3D		8H
HM-7685P	5E	3D		8H
HM-76160	5F			8L
HM-76161	5F			8L
JAN-0512	4K			
CMOS Memory				
HM-6322	4N	3D		
HM-6501	4M	3E		8E
HM-6503	5E	3T	LB	8H
HM-6504	5E	3T	LB	8H
HM-6505	5E	3T	LB	8H
HM-6508	4P	3K		8B
HM-6512	4N	3D	LA	
HM-6513	5E	3T	LB	8C
HM-6514	5E	3T	LB	8H
HM-6515	5F	3F		
HM-6516	5F	3F	LG	
HM-6518	4N	3D	LA	8C
HM-6551	4M	3E		8E
HM-6561	4N	3D	LA	8C
HM-6562	4P	3K		8B
HM-6564			Leadless Array Package MA	
HM-6611	5C			8B
HM-6641	5F			
HM-6661	4N		LA	8C
HM-6716	5J		LG	
HM-6758	5J		LG	
Microprocessor				
HM-6100	5H	3H	LG	
HD-6101	5H	3J	LG	

*These package numbers to be used in product ordering. Other numbers shown in Selection Guide and drawings are internal package numbers.

††Contact factory for latest availability of devices in these packages.

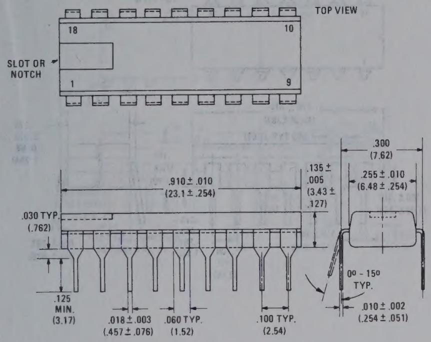
NOTE FOR PACKAGE DRAWINGS ON FOLLOWING PAGES:

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.
3. Internal package codes are shown in black squares.

Package Dimensions

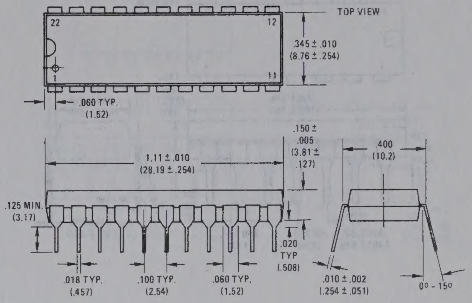
3D **3T**

18 LEAD EPOXY DIP


TOP VIEW
18
10
SLOT OR NOTCH
1
9
.300
(7.62)
.135 ±
.005
(3.43 ±
.127)
.255 ± .010
(6.48 ± .254)
.910 ± .010
(23.1 ± .254)
.030 TYP.
(.762)
0° - 15°
TYP.
.125
MIN.
(3.17)
.018 ± .003
(.457 ± .076)
.060 TYP.
(1.52)
.100 TYP.
(2.54)
.010 ± .002
(.254 ± .051)

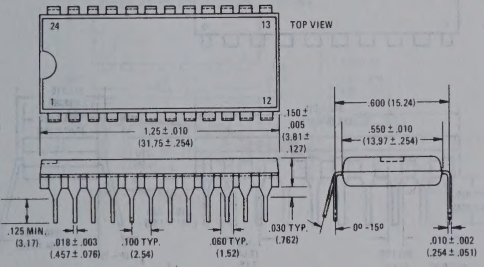
3E

22 LEAD EPOXY DIP


TOP VIEW
22
12
1
11
.345 ± .010
(8.76 ± .254)
.060 TYP.
(1.52)
.150 ±
.005
(3.81 ±
.127)
.400
(10.2)
1.11 ± .010
(28.19 ± .254)
.125 MIN.
(3.17)
.020
TYP
(.508)
.018 TYP.
(.457)
.100 TYP.
(2.54)
.060 TYP.
(1.52)
.010 ± .002
(.254 ± .051)
0° - 15°

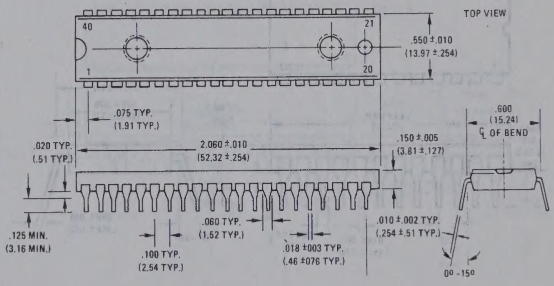
3F

24 LEAD EPOXY DIP


TOP VIEW
24
13
1
12
.600 (15.24)
.150 ±
.005
(3.81 ±
.127)
1.25 ± .010
(31.75 ± .254)
.550 ± .010
(13.97 ± .254)
.125 MIN.
(3.17)
.018 ± .003
(.457 ± .076)
.100 TYP.
(2.54)
.060 TYP.
(1.52)
.030 TYP.
(.762)
0° -15°
.010 ± .002
(.254 ± .051)

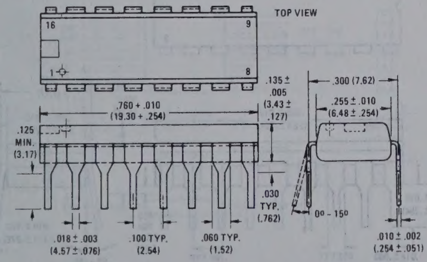
3H **3J**

40 LEAD EPOXY DIP


TOP VIEW
40
21
1
20
.550 ±.010
(13.97 ±.254)
.075 TYP.
(1.91 TYP.)
.600
(15.24)
℄ OF BEND
.020 TYP.
(.51 TYP.)
2.060 ±.010
(52.32 ±.254)
.150 ±.005
(3.81 ±.127)
.125 MIN.
(3.16 MIN.)
.060 TYP.
(1.52 TYP.)
.010 ±.002 TYP.
(.254 ±.51 TYP.)
.018 ±003 TYP.
(.46 ±076 TYP.)
.100 TYP.
(2.54 TYP.)
0° -15°

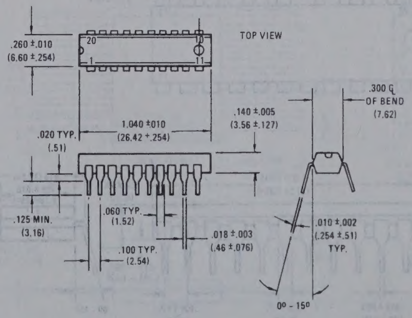
3K **3L**

16 LEAD EPOXY DIP


TOP VIEW
16
9
1
8
.135 ±
.005
(3.43 ±
.127)
.300 (7.62)
.255 ± .010
(6.48 ± .254)
.760 + .010
(19.30 + .254)
.125
MIN.
(3.17)
.030
TYP.
(.762)
0° - 15°
.018 ± .003
(4.57 ± .076)
.100 TYP.
(2.54)
.060 TYP.
(1.52)
.010 ± .002
(.254 ± .051)

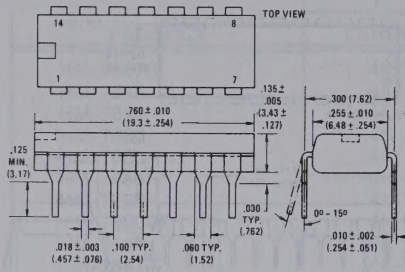
3N

20 LEAD EPOXY DIP


TOP VIEW
20
10
1
11
.260 ±.010
(6.60 ±.254)
.300 ℄
OF BEND
(7.62)
.140 ±.005
(3.56 ±.127)
1.040 ±010
(26.42 +.254)
.020 TYP.
(.51)
.060 TYP.
(1.52)
.125 MIN.
(3.16)
.018 ±.003
(.46 ±.076)
.010 ±.002
(.254 ±.51)
TYP.
.100 TYP.
(2.54)
0° - 15°

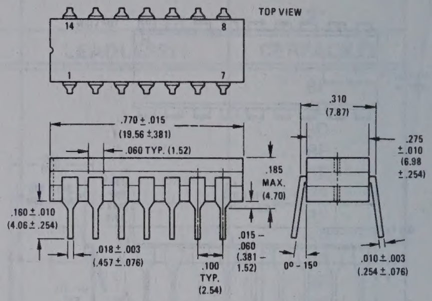
3R

14 LEAD EPOXY DIP


TOP VIEW
14
8
1
7
.760 ± .010
(19.3 ± .254)
.135 ±
.005
(3.43 ±
.127)
.300 (7.62)
.255 ± .010
(6.48 ± .254)
.125
MIN.
(3.17)
.030
TYP.
(.762)
0° - 15°
.010 ± .002
(.254 ± .051)
.018 ± .003
(.457 ± .076)
.100 TYP.
(2.54)
.060 TYP.
(1.52)

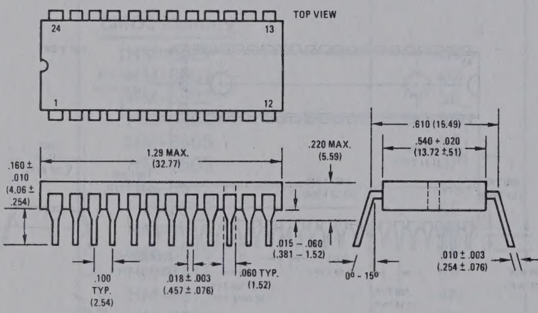
4D

14 LEAD CERDIP


TOP VIEW
14
8
1
7
.770 ± .015
(19.56 ± .381)
.060 TYP. (1.52)
.185
MAX.
(4.70)
.310
(7.87)
.275
± .010
(6.98
± .254)
.160 ± .010
(4.06 ± .254)
.018 ± .003
(.457 ± .076)
.100
TYP.
(2.54)
.015 -
.060
(.381 -
1.52)
0° - 15°
.010 ± .003
(.254 ± .076)

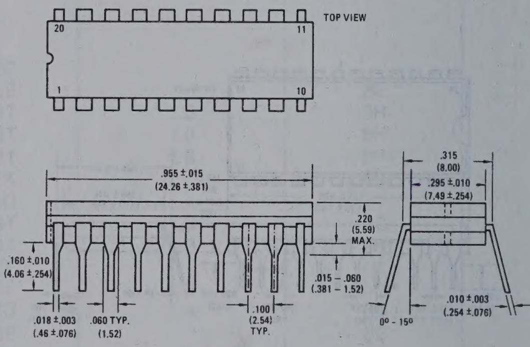
4K **5F**

24 LEAD CERDIP


TOP VIEW
24
13
1
12
1.29 MAX.
(32.77)
.160 ±
.010
(4.06 ±
.254)
.220 MAX.
(5.59)
.610 (15.49)
.540 + .020
(13.72 ± .51)
.015 - .060
(.381 - 1.52)
.100
TYP.
(2.54)
.018 ± .003
(.457 ± .076)
.060 TYP.
(1.52)
0° - 15°
.010 ± .003
(.254 ± .076)

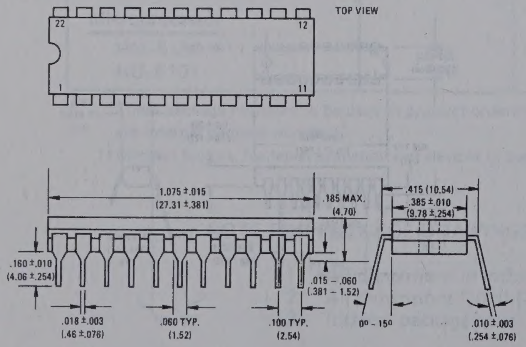
4L

20 LEAD CERDIP


TOP VIEW
20
11
1
10
.955 ± .015
(24.26 ± .381)
.315
(8.00)
.295 ± .010
(7.49 ± .254)
.220
(5.59)
MAX.
.160 ± .010
(4.06 ± .254)
.015 - .060
(.381 - 1.52)
.018 ± .003
(.46 ± .076)
.060 TYP.
(1.52)
.100
(2.54)
TYP.
0° - 15°
.010 ± .003
(.254 ± .076)

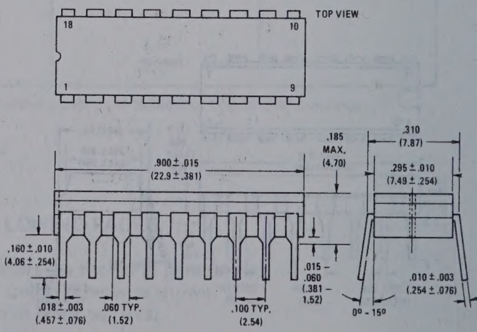
4M

22 LEAD CERDIP


TOP VIEW
22
12
1
11
1.075 ± .015
(27.31 ± .381)
.185 MAX.
(4.70)
.415 (10.54)
.385 ± .010
(9.78 ± .254)
.160 ± .010
(4.06 ± .254)
.015 - .060
(.381 - 1.52)
.018 ± .003
(.46 ± .076)
.060 TYP.
(1.52)
.100 TYP.
(2.54)
0° - 15°
.010 ± .003
(.254 ± .076)

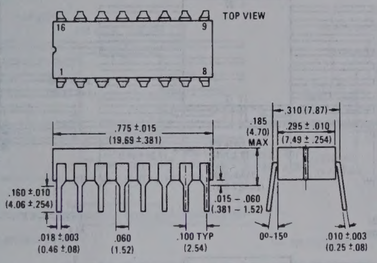
4N **5E**

18 LEAD CERDIP


TOP VIEW
18
10
1
9
.900 ± .015
(22.9 ± .381)
.185
MAX.
(4.70)
.310
(7.87)
.295 ± .010
(7.49 ± .254)
.160 ± .010
(4.06 ± .254)
.015 -
.060
(.381 -
1.52)
.018 ± .003
(.457 ± .076)
.060 TYP.
(1.52)
.100 TYP.
(2.54)
0° - 15°
.010 ± .003
(.254 ± .076)

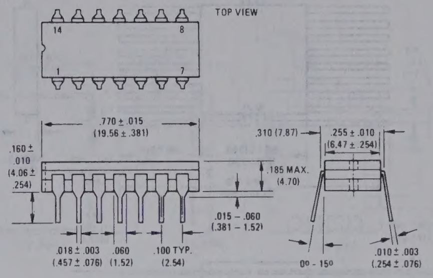
4P **5C**

16 LEAD CERDIP


TOP VIEW
16
9
1
8
.775 ±.015
(19.69 ±.381)
.185
(4.70)
MAX
.310 (7.87)
.295 ± .010
(7.49 ± .254)
.160 ±.010
(4.06 ±.254)
.015 – .060
(.381 – 1.52)
.018 ±.003
(0.46 ±.08)
.060
(1.52)
.100 TYP
(2.54)
0°-15°
.010 ±.003
(0.25 ±.08)

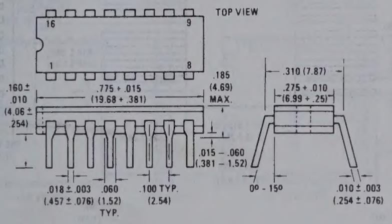
4U

14 LEAD CERDIP


TOP VIEW
14
8
1
7
.770 ± .015
(19.56 ± .381)
.160 ±
.010
(4.06 ±
.254)
.310 (7.87)
.255 ± .010
(6.47 ± .254)
.185 MAX.
(4.70)
.015 – .060
(.381 – 1.52)
.018 ± .003
(.457 ± .076)
.060
(1.52)
.100 TYP.
(2.54)
0° - 15°
.010 ± .003
(.254 ± .076)

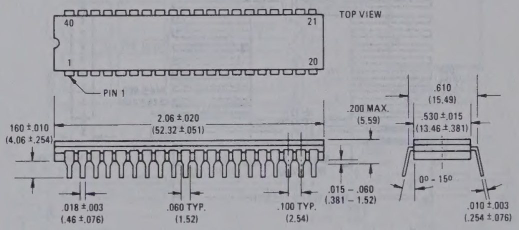
4Z

16 LEAD CERDIP


TOP VIEW
16
9
1
8
.160 ±
.010
(4.06 ±
.254)
.775 + .015
(19.68 + .381)
.185
(4.69)
MAX.
.310 (7.87)
.275 + .010
(6.99 + .25)
.015 – .060
(.381 – 1.52)
.018 ± .003
(.457 ± .076)
.060
(1.52)
TYP.
.100 TYP.
(2.54)
0° - 15°
.010 ± .003
(.254 ± .076)

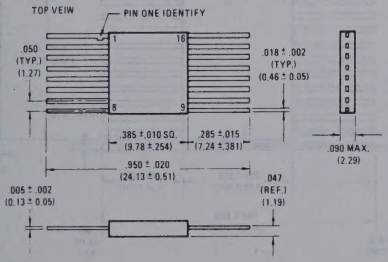
5H

40 LEAD CERDIP


TOP VIEW
40
21
1
20
PIN 1
160 ±.010
(4.06 ±.254)
2.06 ±.020
(52.32 ±.051)
.200 MAX.
(5.59)
.610
(15.49)
.530 ±.015
(13.46 ±.381)
0° - 15°
.015 – .060
(.381 – 1.52)
.018 ±.003
(.46 ±.076)
.060 TYP.
(1.52)
.100 TYP.
(2.54)
.010 ±.003
(.254 ±.076)

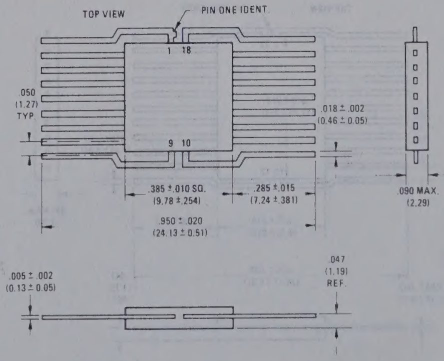
8B

16 LEAD CERPACK


TOP VEIW
PIN ONE IDENTIFY
1
16
8
9
.050
(TYP.)
(1.27)
.018 ± .002
(TYP.)
(0.46 ± 0.05)
.385 ±.010 SQ.
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.090 MAX.
(2.29)
.950 ± .020
(24.13 ± 0.51)
.005 ± .002
(0.13 ± 0.05)
.047
(REF.)
(1.19)

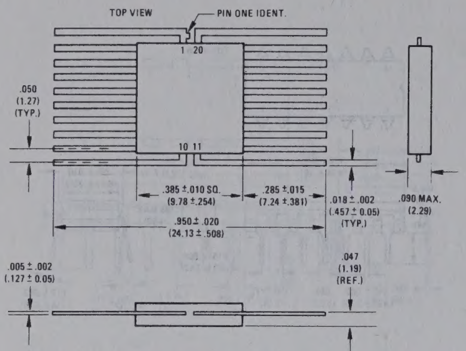
8C

18 LEAD CERPACK


TOP VIEW
PIN ONE IDENT.
1
18
9
10
.050
(1.27)
TYP.
.018 ± .002
(0.46 ± 0.05)
.385 ±.010 SQ.
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.090 MAX.
(2.29)
.950 ± .020
(24.13 ± 0.51)
.005 ± .002
(0.13 ± 0.05)
.047
(1.19)
REF.

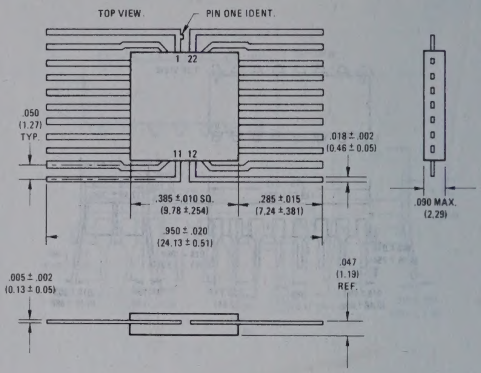
8D

20 LEAD CERPACK


TOP VIEW
PIN ONE IDENT.
1 20
10 11
.050
(1.27)
(TYP.)
.385 ±.010 SQ.
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.018 ± .002
(.457 ± 0.05)
(TYP.)
.090 MAX.
(2.29)
.950 ± .020
(24.13 ± .508)
.047
(1.19)
(REF.)
.005 ± .002
(.127 ± 0.05)

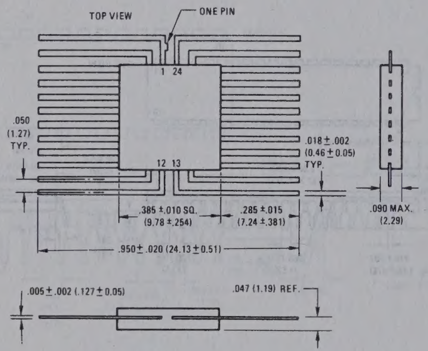
8E

22 LEAD CERPACK


TOP VIEW.
PIN ONE IDENT.
1 22
11 12
.050
(1.27)
TYP.
.018 ± .002
(0.46 ± 0.05)
.385 ±.010 SQ.
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.090 MAX.
(2.29)
.950 ± .020
(24.13 ± 0.51)
.047
(1.19)
REF.
.005 ± .002
(0.13 ± 0.05)

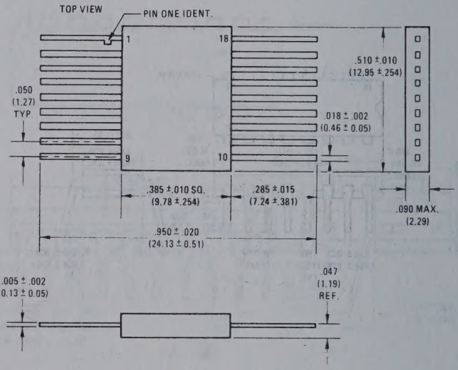
8F

24 LEAD CERPACK


TOP VIEW
ONE PIN
1 24
12 13
.050
(1.27)
TYP.
.018 ± .002
(0.46 ± 0.05)
TYP.
.385 ±.010 SQ.
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.090 MAX.
(2.29)
.950 ± .020 (24.13 ± 0.51)
.005 ± .002 (.127 ± 0.05)
.047 (1.19) REF.

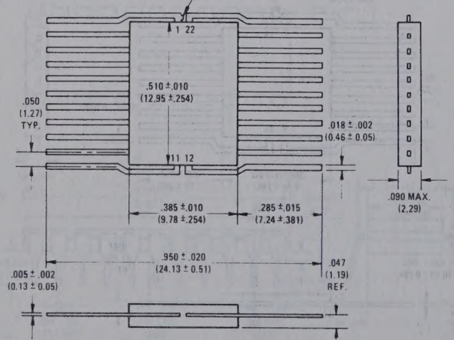
8H

18 LEAD CERPACK


TOP VIEW
PIN ONE IDENT.
1
18
9
10
.510 ±.010
(12.95 ±.254)
.050
(1.27)
TYP.
.018 ± .002
(0.46 ± 0.05)
.385 ±.010 SQ.
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.090 MAX.
(2.29)
.950 ± .020
(24.13 ± 0.51)
.047
(1.19)
REF.
.005 ± .002
(0.13 ± 0.05)

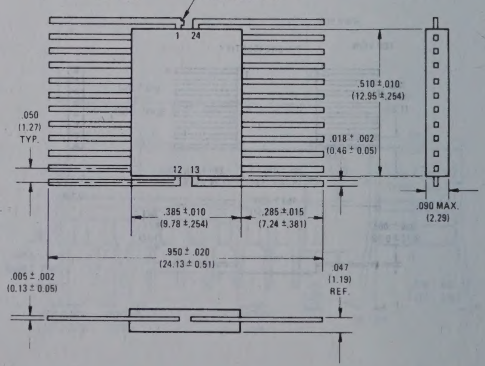
8K

22 LEAD CERPACK


TOP VIEW
PIN ONE IDENT.
1 22
11 12
.510 ±.010
(12.95 ±.254)
.050
(1.27)
TYP.
.018 ± .002
(0.46 ± 0.05)
.090 MAX.
(2.29)
.385 ±.010
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.950 ± .020
(24.13 ± 0.51)
.047
(1.19)
REF.
.005 ± .002
(0.13 ± 0.05)

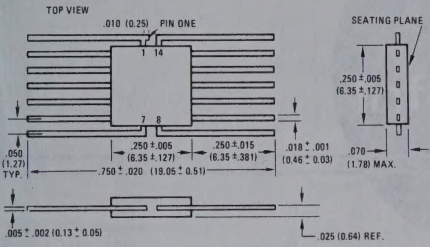
8L

24 LEAD CERPACK


TOP VIEW
PIN ONE IDENT.
1 24
12 13
.510 ±.010
(12.95 ±.254)
.050
(1.27)
TYP.
.018 ± .002
(0.46 ± 0.05)
.090 MAX.
(2.29)
.385 ±.010
(9.78 ±.254)
.285 ±.015
(7.24 ±.381)
.950 ± .020
(24.13 ± 0.51)
.047
(1.19)
REF.
.005 ± .002
(0.13 ± 0.05)

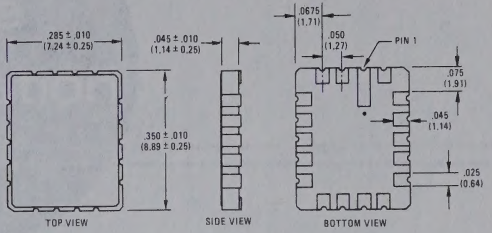
9H

14 LEAD FLATPACK


TOP VIEW
.010 (0.25)
PIN ONE
1
14
7
8
.050
(1.27)
TYP.
.250 ±.005
(6.35 ±.127)
.250 ±.015
(6.35 ±.381)
.750 ± .020 (19.05 ± 0.51)
.018 ± .001
(0.46 ± 0.03)
SEATING PLANE
.250 ±.005
(6.35 ±.127)
.070
(1.78) MAX.
.005 ± .002 (0.13 ± 0.05)
.025 (0.64) REF.

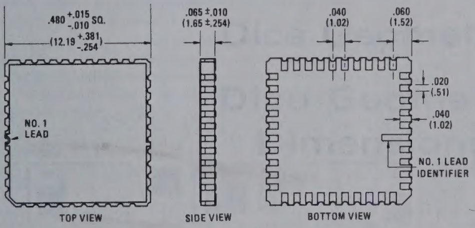
LA **LB**

18 LEAD LEADLESS CHIP CARRIER


.285 ± .010
(7.24 ± 0.25)
.350 ± .010
(8.89 ± 0.25)
TOP VIEW
.045 ± .010
(1.14 ± 0.25)
SIDE VIEW
.0675
(1.71)
.050
(1.27)
PIN 1
.075
(1.91)
.045
(1.14)
.025
(0.64)
BOTTOM VIEW

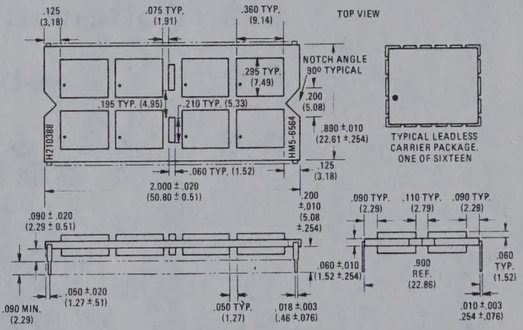
LG

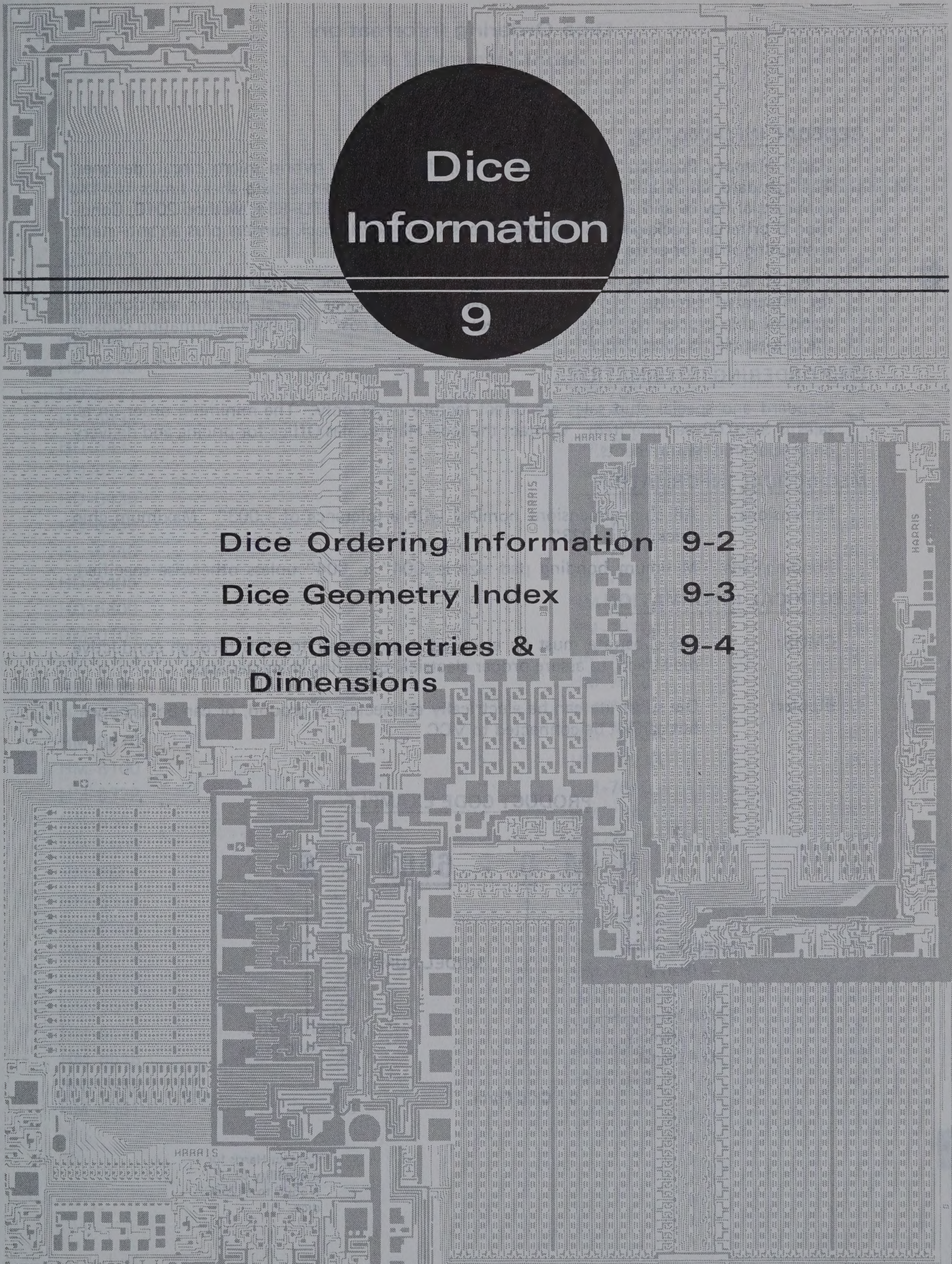
40 LEAD LEADLESS CHIP CARRIER


.480 +.015 -.010 SQ.
(12.19 +.381 -.254)
NO. 1
LEAD
TOP VIEW
.065 ±.010
(1.65 ±.254)
SIDE VIEW
.040
(1.02)
.060
(1.52)
.020
(.51)
.040
(1.02)
NO. 1 LEAD
IDENTIFIER
BOTTOM VIEW

MA

40 LEAD 64K RAM MEMORY MODULE


.125
(3.18)
.075 TYP.
(1.91)
.360 TYP.
(9.14)
TOP VIEW
.295 TYP.
(7.49)
NOTCH ANGLE
90° TYPICAL
.200
(5.08)
.195 TYP. (4.95)
.210 TYP. (5.33)
H210388
HM5-6564
.890 ±.010
(22.61 ±.254)
TYPICAL LEADLESS
CARRIER PACKAGE.
ONE OF SIXTEEN
.060 TYP. (1.52)
.125
(3.18)
2.000 ± .020
(50.80 ± 0.51)
.200
±.010
(5.08
±.254)
.090 ± .020
(2.29 ± 0.51)
.090 TYP.
(2.29)
.110 TYP.
(2.79)
.090 TYP.
(2.29)
.060 ±.010
(1.52 ±.254)
.900
REF.
(22.86)
.060
TYP.
(1.52)
.050 ±.020
(1.27 ±.51)
.090 MIN.
(2.29)
.050 TYP.
(1.27)
.018 ±.003
(.46 ±.076)
.010 ±.003
.254 ±.076)



Dice Information

9

Dice Ordering Information 9-2
Dice Geometry Index 9-3
Dice Geometries & Dimensions 9-4

Dice Ordering Information

GENERAL INFORMATION

Harris Memory Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at +25°C to the data sheet limits for the commercial device and are 100% visually inspected to MIL-STD-883, Method 2010, Condition B criteria. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. For more information consult the nearest Harris Sales Office.

CHIP ORDERING INFORMATION

Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office for pricing and delivery on special chip requirements.

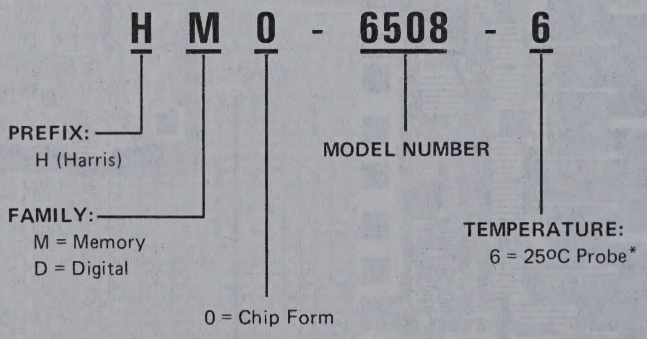
MECHANICAL INFORMATION

Dimensions:	All chip dimensions nominal with a tolerance of ±.003″. Maximum chip thickness is .023″.
Bonding Pads:	Minimum bonding pad size is .004″ x .004″ unless otherwise specified.

ELECTRICAL INFORMATION

CMOS:	Die substrate must be electrically connected to VCC through conductive die attach, to assure proper electrical operating characteristics.
Bipolar:	Die substrate can be electrically connected to ground, or can be left open, but cannot be connected to VCC.

PRODUCT CODE EXAMPLE

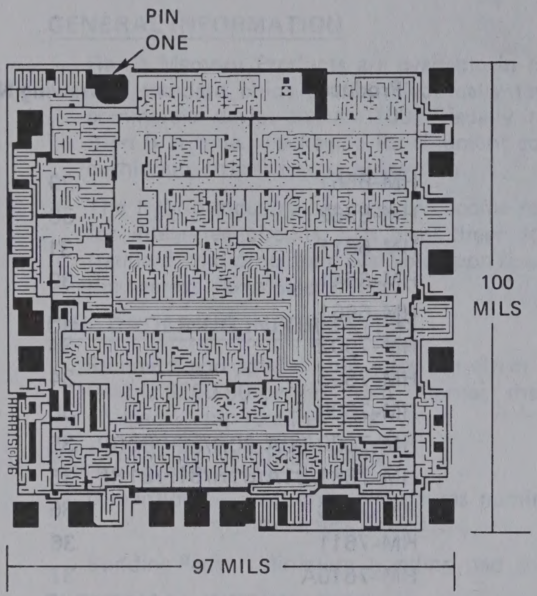


*Contact Harris for availability of -2 (-55°C to +125°C) dice.

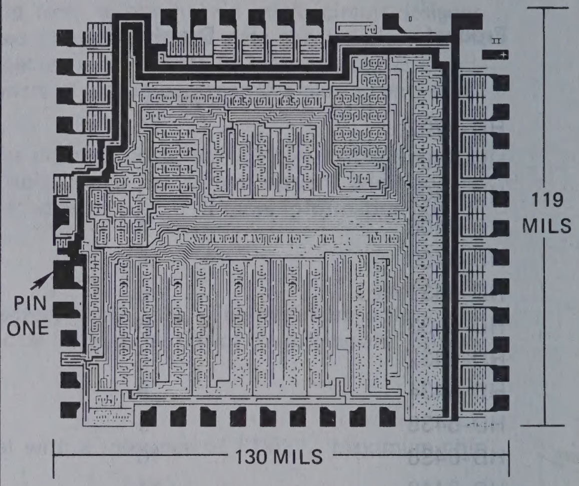
Dice Geometry Index

Product	Drawing No.
HD-4702	1
HD-6101	2
HD-6402	3
HD-6408	4
HD-6409	5
HD-6431	6
HD-6433	6
HD-6432	7
HD-6434	8
HD-6435	9
HD-6436	10
HD-6440	11
HD-6495	6
HD-6600	12
HM-0104	13
HM-0168	14
HM-0186	15
HM-0198	16
HM-0410	17
HM-6100	18
HM-6322	19
HM-6501	20
HM-6503	21
HM-6504	21
HM-6505	22
HM-6508	23
HM-6512	24
HM-6513	25
HM-6514	25
HM-6515	26
HM-6516	26
HM-6518	27
HM-6551	28
HM-6561	29
HM-6562	30
HM-6611	31
HM-6641	32
HM-6661	33
HM-7602	34
HM-7603	34
HM-7608	35
HM-7680/80A/80R/80P/80RP	35
HM-7681/81A/81R/81P/81RP	35
HM-7610	36
HM-7611	36
HM-7610A	37
HM-7611A	37
HM-76160	38
HM-76161	38
HM-7620	39
HM-7621	39
HM-7620A	40
HM-7621A	40
HM-7640	41
HM-7641	41
HM-7642	42
HM-7643	42
HM-7644	42
HM-7642A	43
HM-7642P	43
HM-7643A	43
HM-7643P	43
HM-7647R	44
HM-7648	44
HM-7649	44

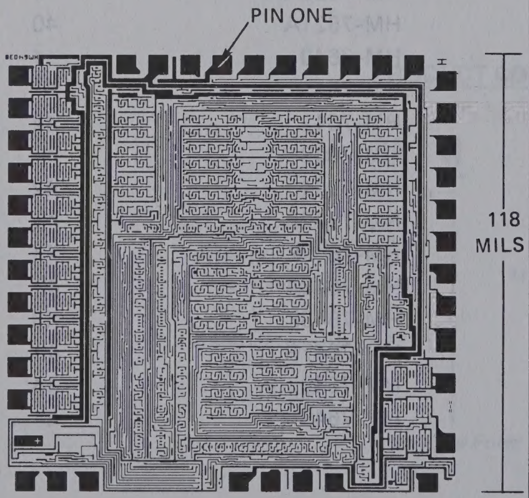
1 **HD-4702**


PIN ONE
100 MILS
97 MILS

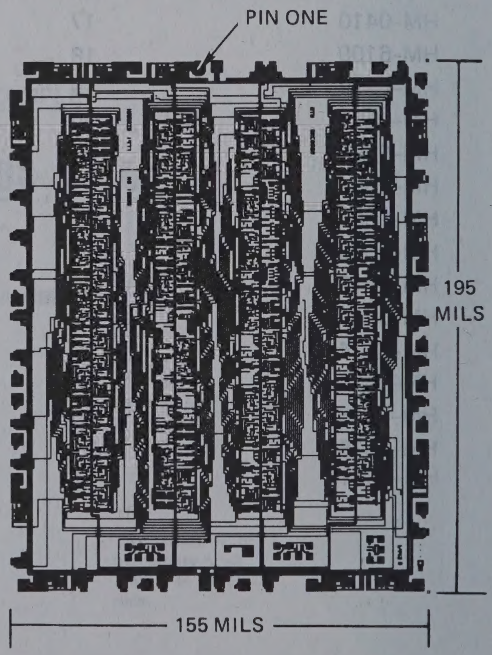
2 **HD-6101**


PIN ONE
119 MILS
130 MILS

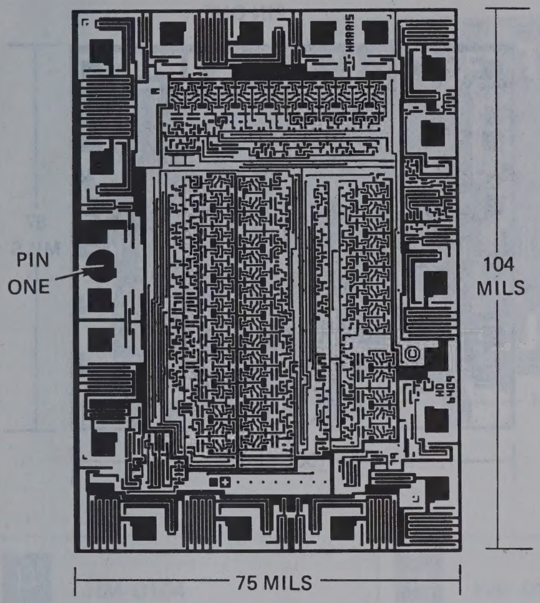
3 **HD 6402**


PIN ONE
118 MILS
115 MILS

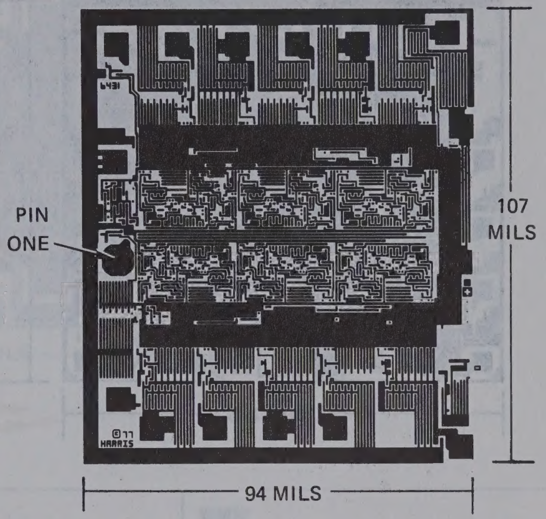
4 **HD-6408**


PIN ONE
195 MILS
155 MILS

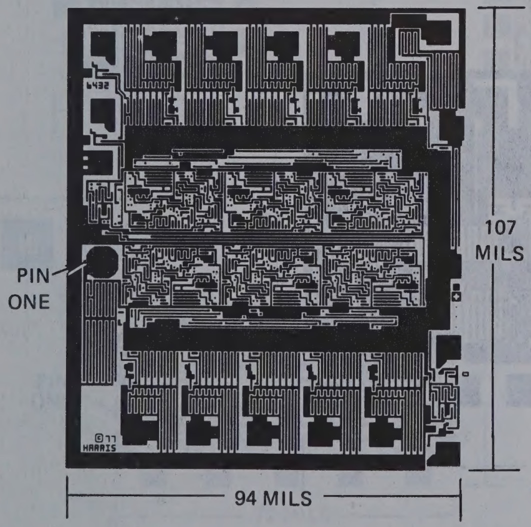
5 HD-6409


HARRIS
HD 6409
PIN ONE
104 MILS
75 MILS

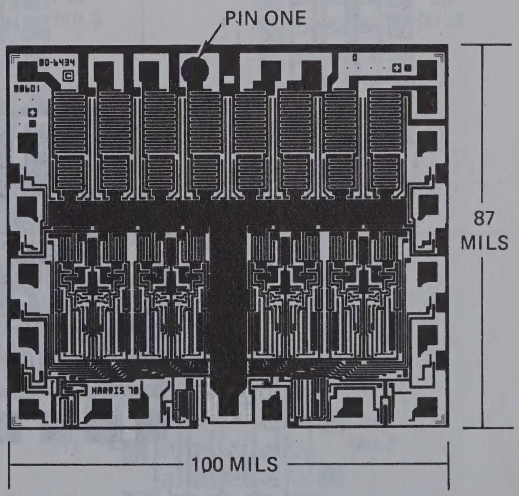
6 HD-6431, HD-6433, HD-6495


6431
©77 HARRIS
PIN ONE
107 MILS
94 MILS

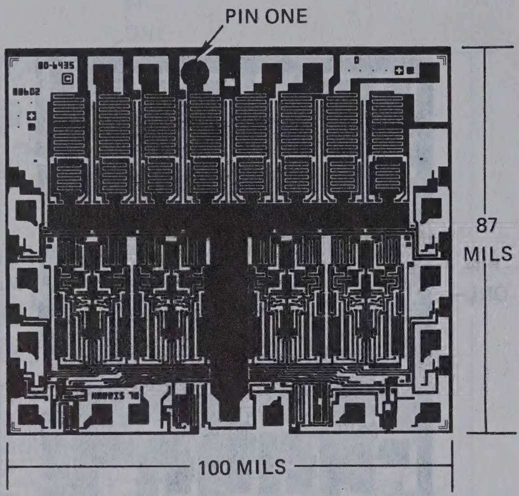
7 HD-6432


6432
©77 HARRIS
PIN ONE
107 MILS
94 MILS

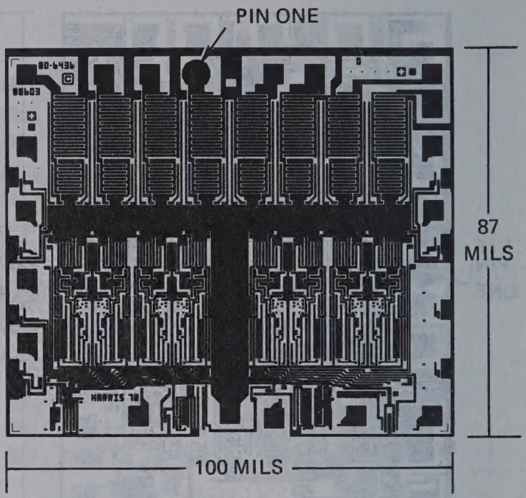
8 HD-6434


PIN ONE
BD-6434
HARRIS 78
87 MILS
100 MILS

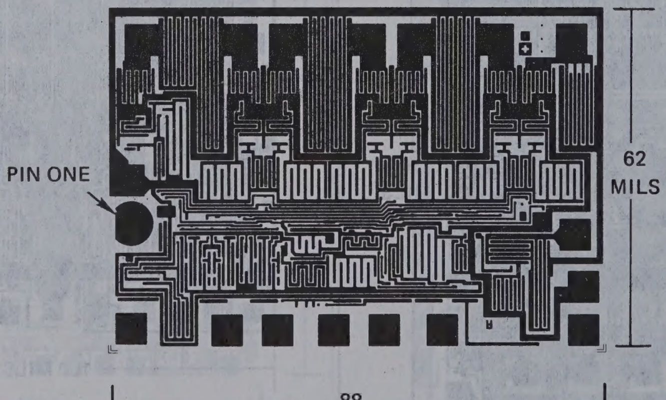
9 HD-6435


PIN ONE
87
MILS
100 MILS

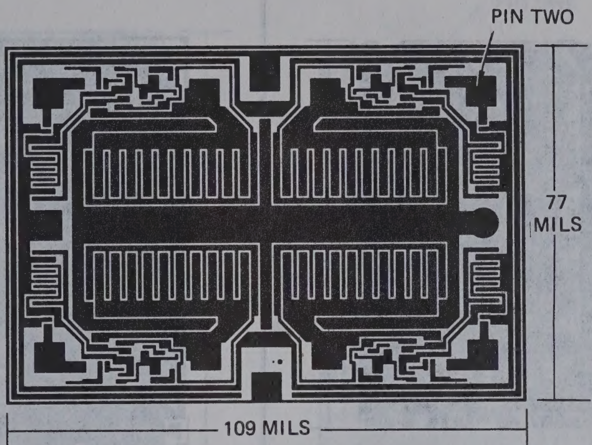
10 HD-6436


PIN ONE
87
MILS
100 MILS

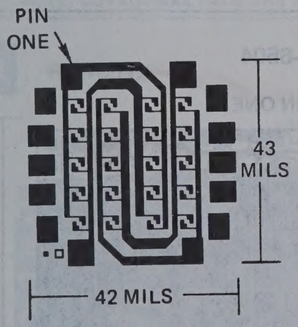
11 HD-6440


PIN ONE
62
MILS
88
MILS

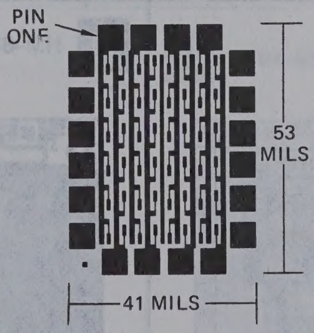
12 **HD-6600**


PIN TWO
77 MILS
109 MILS

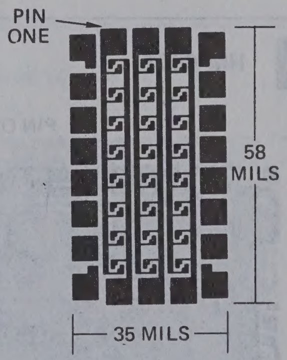
13 **HM-0104**


PIN ONE
43 MILS
42 MILS

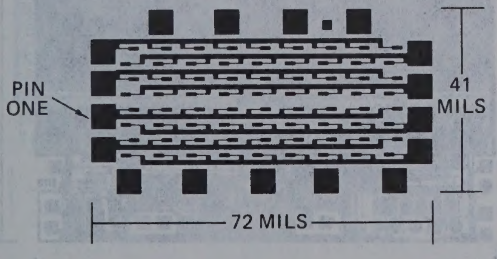
14 **HM-0168**


PIN ONE
53 MILS
41 MILS

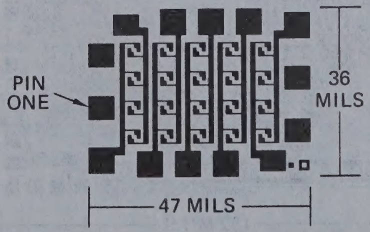
15 **HM-0186**


PIN ONE
58 MILS
35 MILS

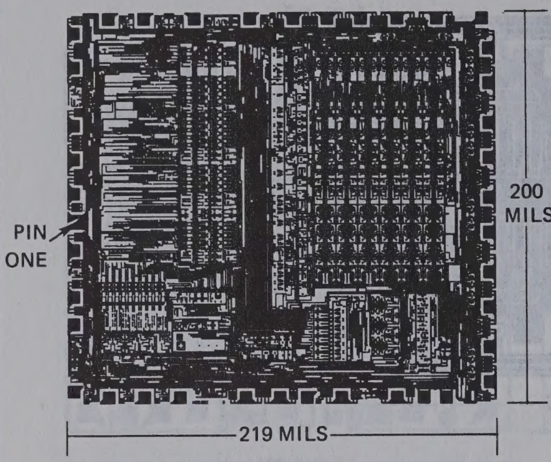
16 **HM-0198**


PIN ONE
41 MILS
72 MILS

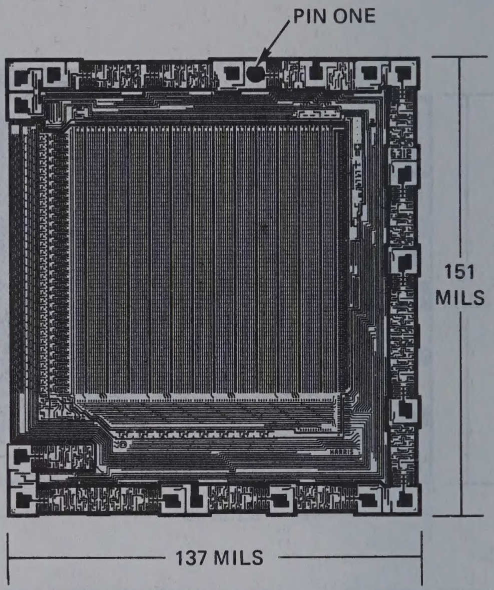
17 **HM-0410**


PIN ONE
36 MILS
47 MILS

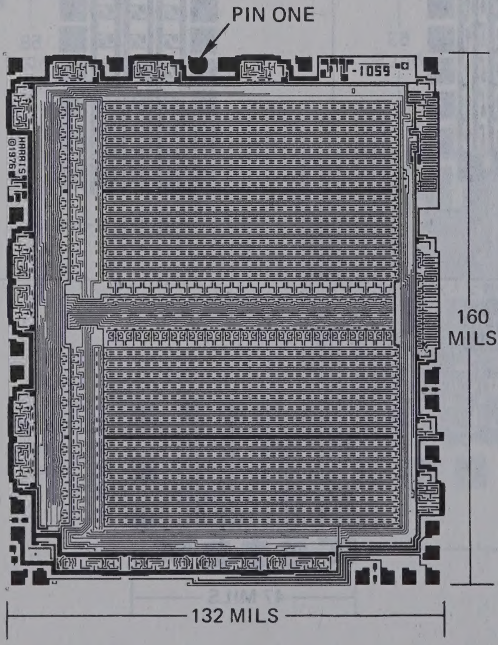
18 **HM-6100**


PIN ONE
200 MILS
219 MILS

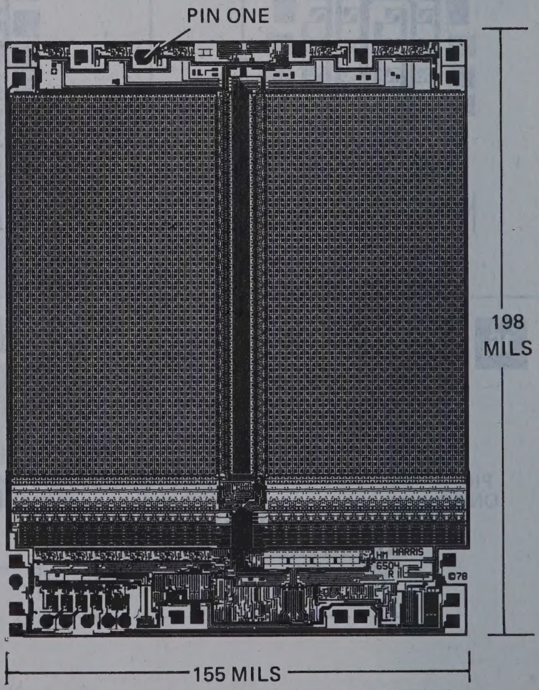
19 **HM-6322**


PIN ONE
HARRIS
151 MILS
137 MILS

20 **HM-6501**

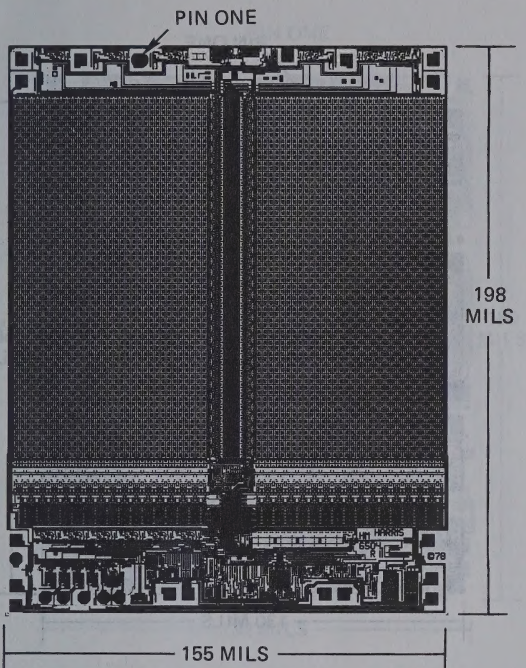

PIN ONE
6501-1059
HARRIS ©1976
160 MILS
132 MILS

21 **HM-6503, HM-6504**


PIN ONE
HM HARRIS 6504 R
©78
198 MILS
155 MILS

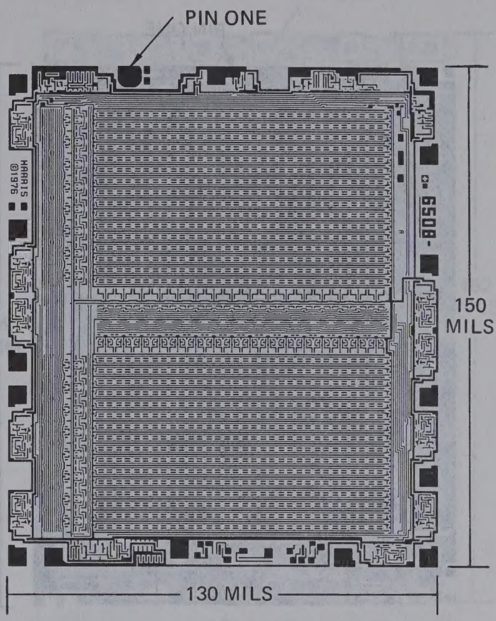
NOTE: OCTAGONAL PADS ARE NOT FOR BONDING.

22 HM-6505

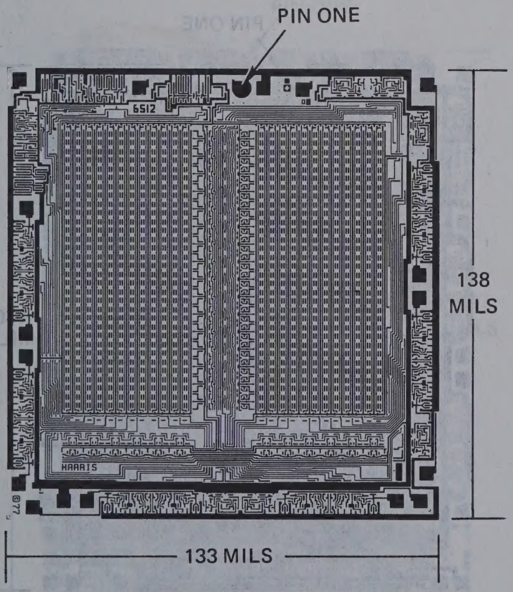

PIN ONE
198 MILS
155 MILS
HARRIS
650
R
©78

NOTE: OCTAGONAL PADS ARE NOT FOR BONDING.

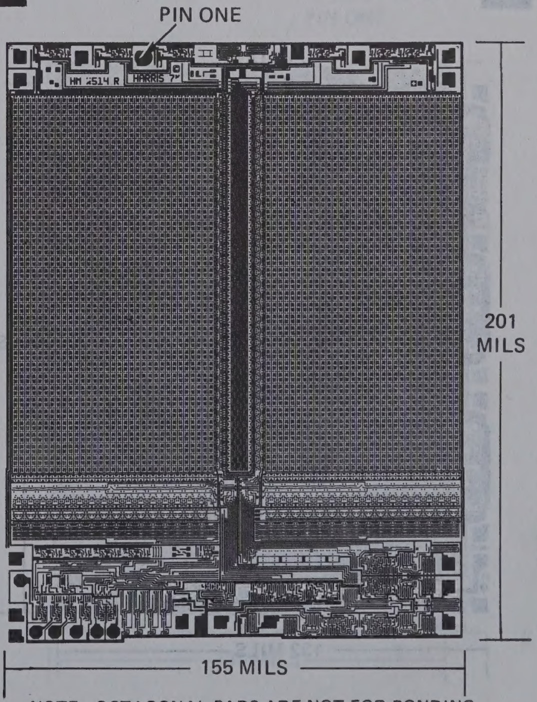
23 HM-6508


PIN ONE
HARRIS ©1976
6508-
150 MILS
130 MILS

24 HM-6512

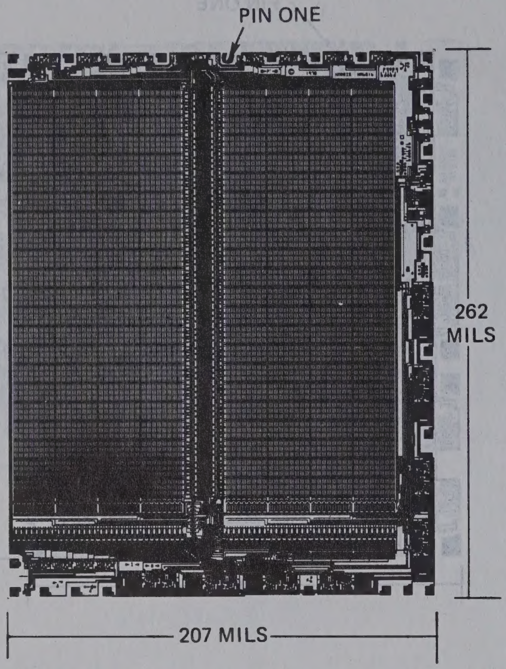

PIN ONE
6512
HARRIS
©77
138 MILS
133 MILS

25 HM-6513, HM-6514

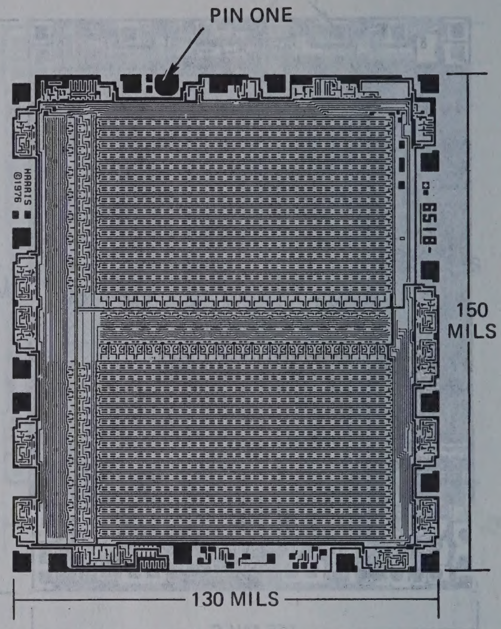

PIN ONE
HM 6514 R
HARRIS 7
201 MILS
155 MILS

NOTE: OCTAGONAL PADS ARE NOT FOR BONDING.

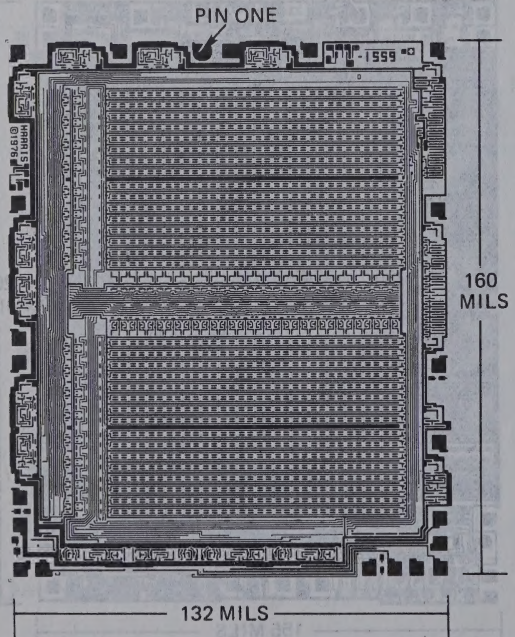
26 HM-6515, HM-6516


PIN ONE
262 MILS
207 MILS

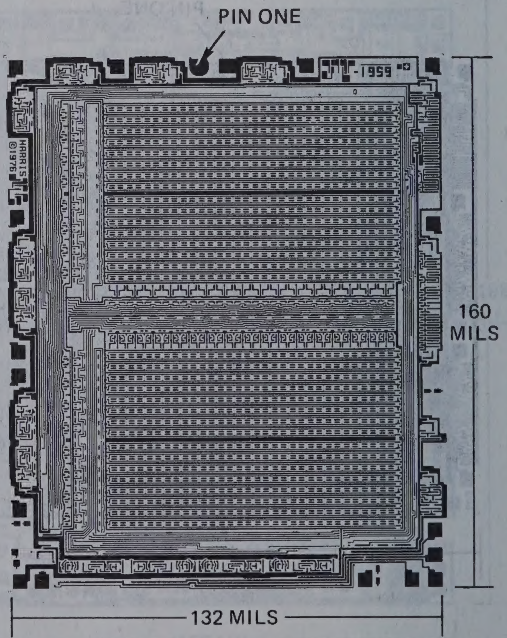
27 HM-6518


PIN ONE
HARRIS ©1976
6518-B
150 MILS
130 MILS

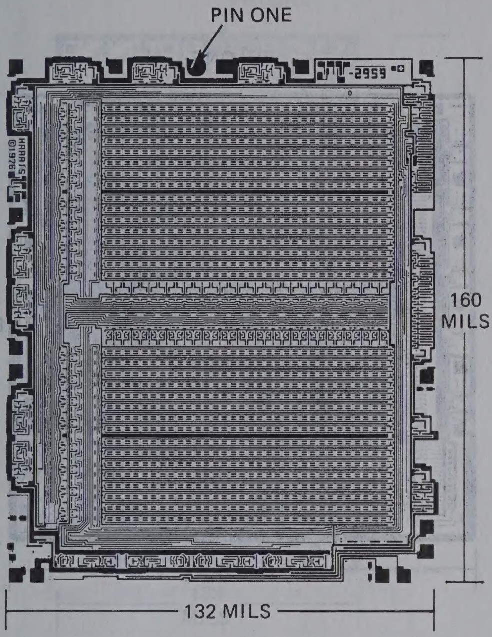
28 HM-6551


PIN ONE
HARRIS ©1976
160 MILS
132 MILS

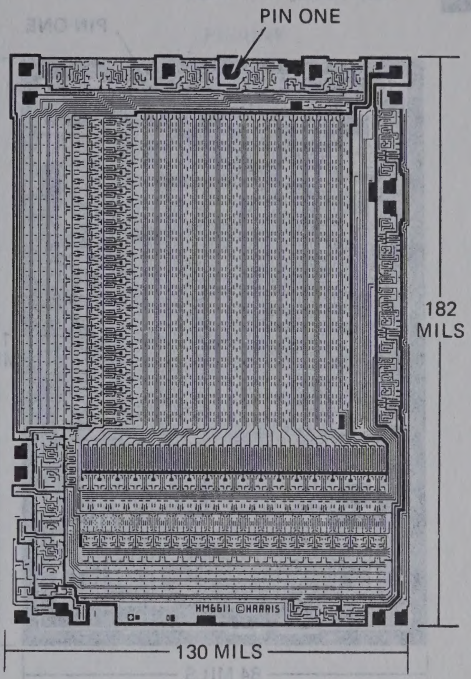
29 HM-6561


PIN ONE
HARRIS ©1976
160 MILS
132 MILS

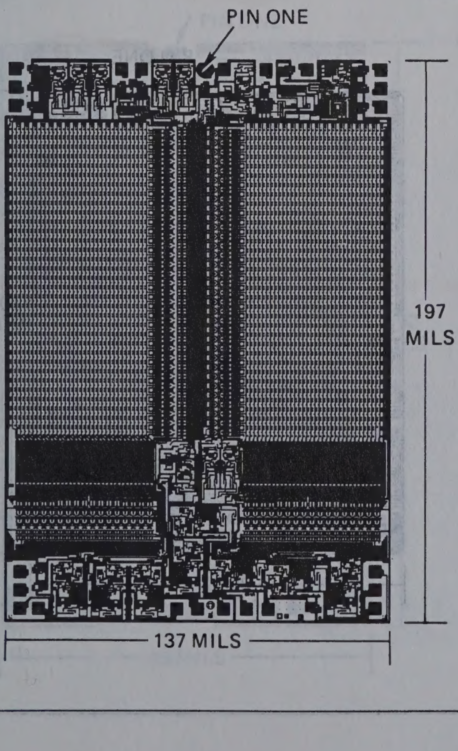
30 **HM-6562**


PIN ONE
2959
HARRIS ©1978
160 MILS
132 MILS

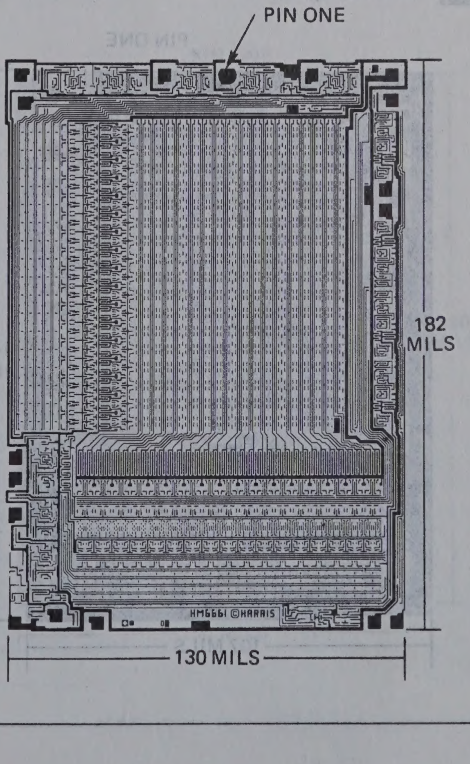
31 **HM-6611**


PIN ONE
182 MILS
HM6611 ©HARRIS
130 MILS

32 **HM-6641**

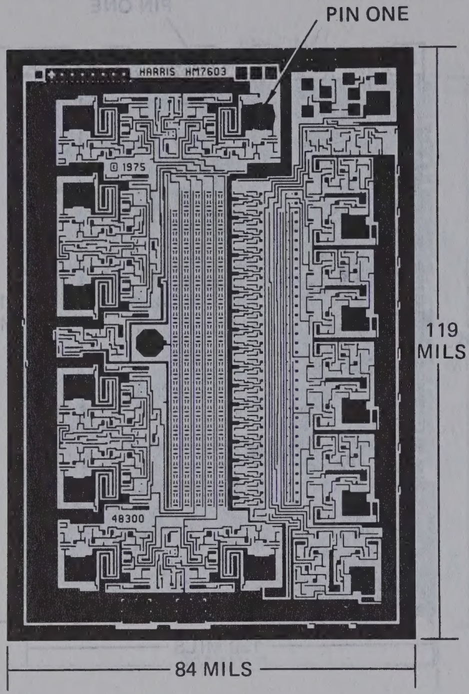

PIN ONE
197 MILS
137 MILS

33 **HM-6661**


PIN ONE
182 MILS
HM6661 ©HARRIS
130 MILS

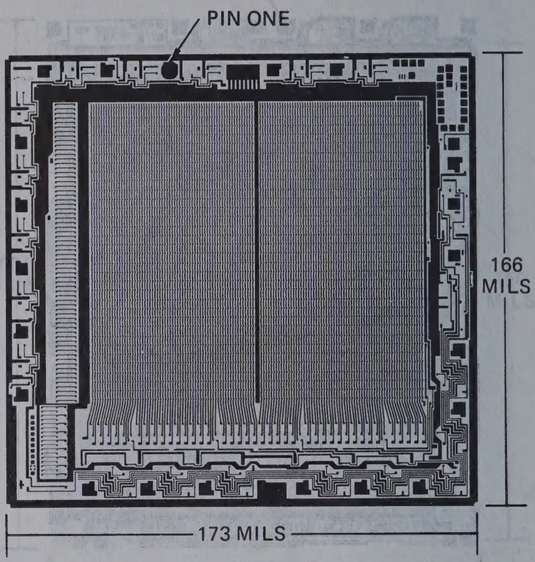
34

HM-7602, HM-7603


PIN ONE
HARRIS HM7603
© 1975
48300
119 MILS
84 MILS

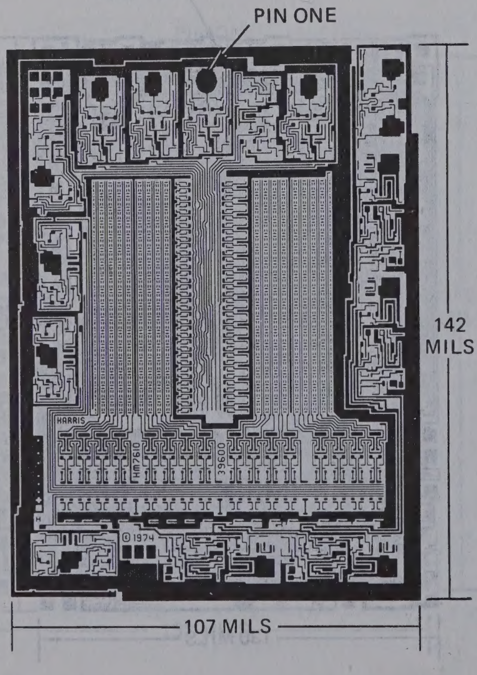
35

HM-7608, HM-7680/80A/80R/80P/80RP, HM-7681/81A/81R/81P/81RP


PIN ONE
166 MILS
173 MILS

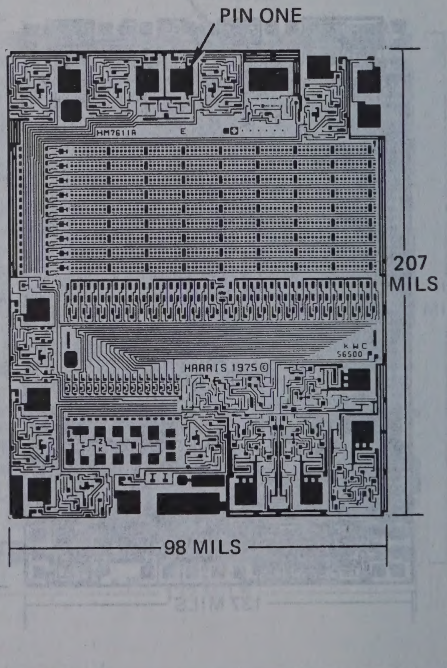
36

HM-7610, HM-7611

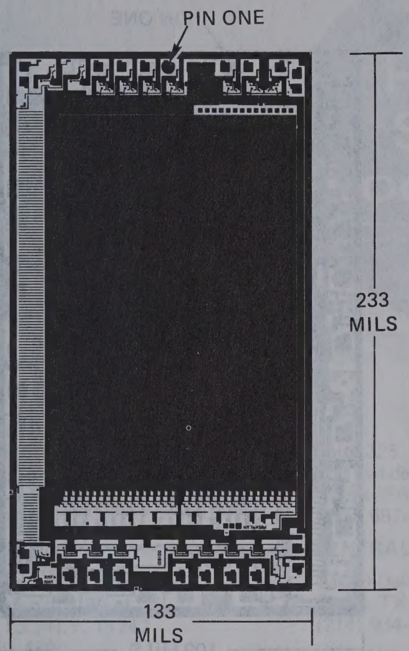

PIN ONE
HARRIS
HM7610
39600
© 1974
142 MILS
107 MILS

37

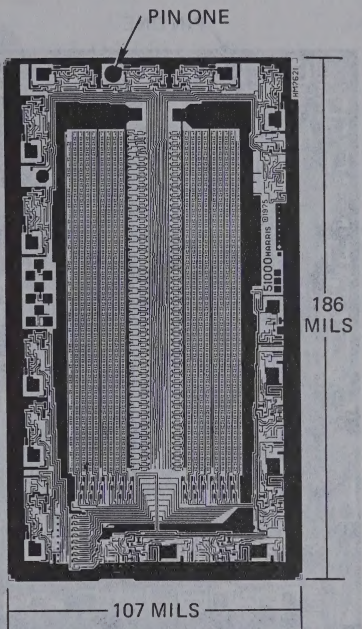
HM-7610A, HM-7611A


PIN ONE
HM7611A
E
HARRIS 1975 ©
KWC
56500
207 MILS
98 MILS

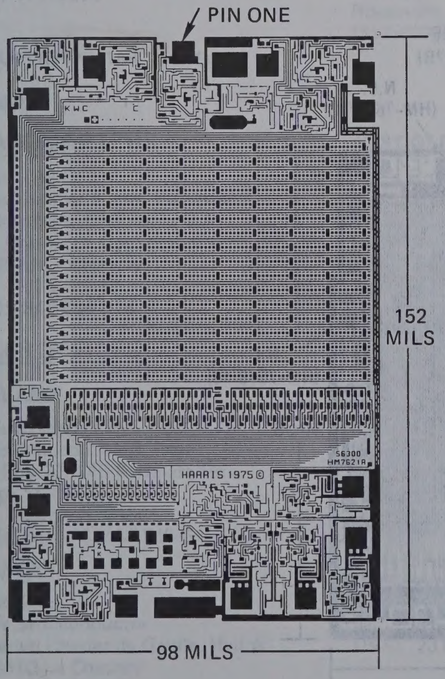
38 HM-76160, HM-76161


PIN ONE
233 MILS
133 MILS

39 HM-7620, HM-7621


PIN ONE
HM7621
51000 HARRIS ©1975
186 MILS
107 MILS

40 HM-7620A, HM-7621A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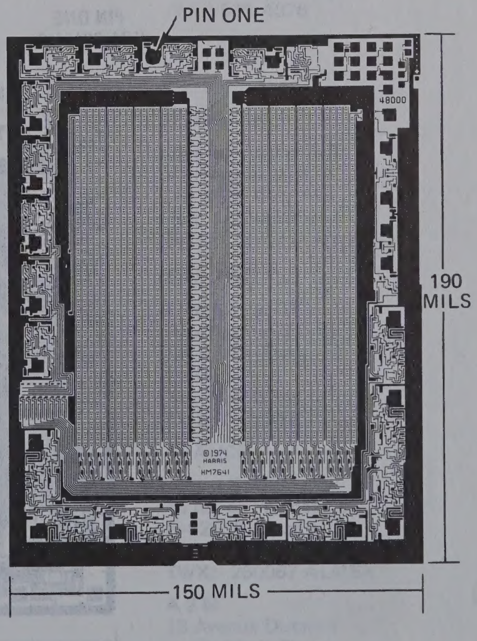
KWC
56300 HM7621A
HARRIS 1975 ©
152 MILS
98 MILS

41 HM-7640, HM-7641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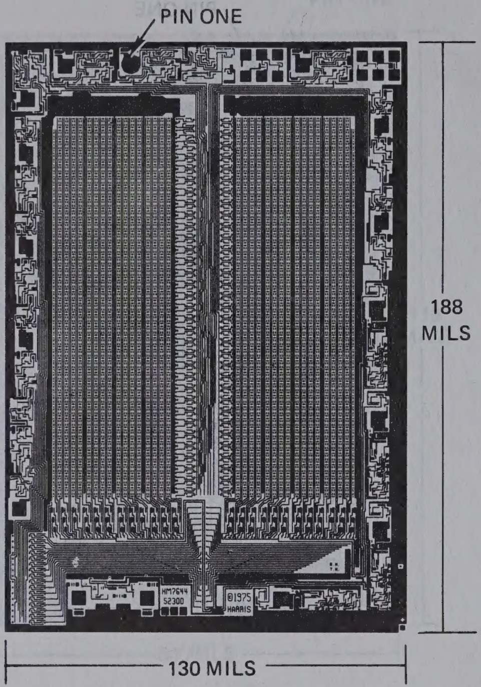
48000
©1974 HARRIS HM7641
190 MILS
150 MILS

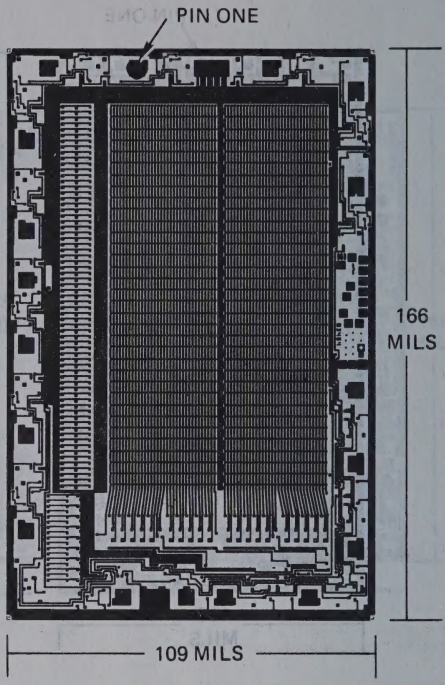
42

HM-7642, HM-7643, HM-7644


PIN ONE
HM7644
52300
©1975
HARRIS
188
MILS
130 MILS

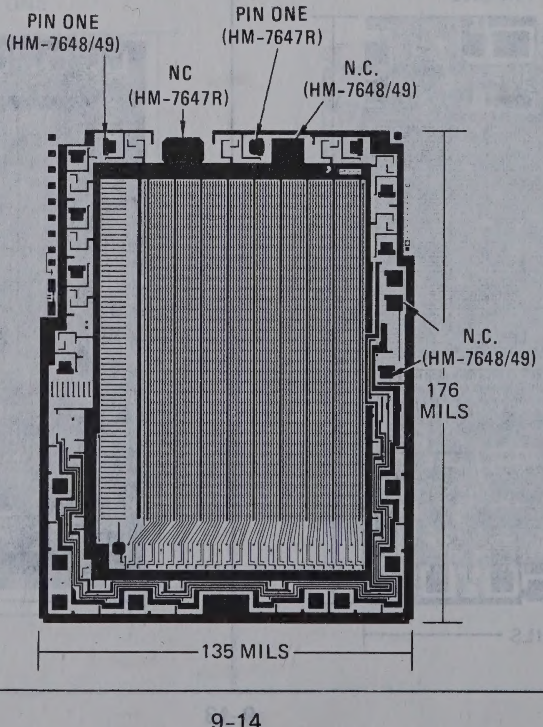
43

HM-7642A, HM-7642P, HM-7643A, HM-7643P


PIN ONE
166
MILS
109 MILS

44

HM-7647R, HM-7648, HM-7649


PIN ONE
(HM-7648/49)
NC
(HM-7647R)
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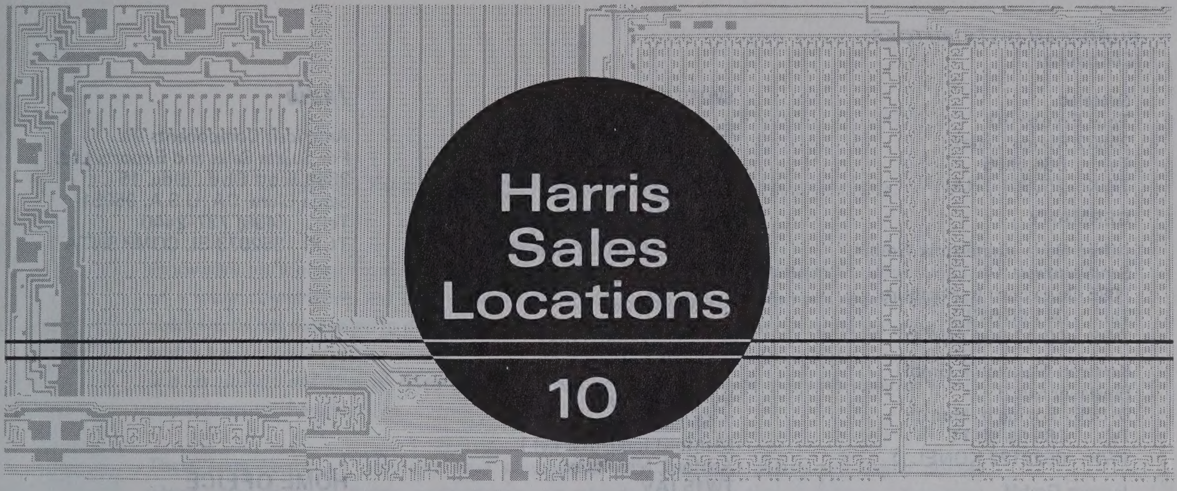
N.C.
(HM-7648/49)
N.C.
(HM-7648/49)
176
MILS
135 MILS



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10

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